SG733/733C

The SG733/733C are monolithic two-stage wideband amplifiers. These devices offer excellent gain stability at any gain setting and provide fixed gain options of 10, 100 and 400 without external components. All stages are current source biased to obtain high common mode and power supply rejection and emitter followers are used at the output to minimize the effects of capacitive loading. The devices are particularly well suited for applications requiring a fast linear function such as video and pulse amplifiers.

- **120MHz bandwidth**
- **Gain options of 10, 100, 400 without external components**
- **250kΩ input resistance**
- **No external frequency compensation necessary**

PARAMETERS*		733	733C	UNITS
Supply Voltage		±6V	±6V	V
Operating Temperature Range		−55 to +125	0 to +70	°C
Package Types		T, J	T, J, N	—
Differential Voltage Gain				
Gain 1[1]		300/500	250/600	V/V
Gain 2[2]		90/110	80/120	
Gain 3[3]		9/11	8/12	
Bandwidth				
Gain 1	$R_S = 50\Omega$	40 (typ)	40 (typ)	MHz
Gain 2		90 (typ)	90 (typ)	
Gain 3		120 (typ)	120 (typ)	
Risetime				
Gain 2, $R_s = 50\Omega$, $V_{out} = 1V_{p-p}$		10	12	nS
Propagation Delay				
Gain 2, $R_s = 50\Omega$, $V_{out} = 1V_{p-p}$		10	10	nS
Input Resistance				
Gain 2		20	10	kΩ
Input Capacitance				
Gain 2		2 (typ)	2 (typ)	pF
Input Offset Current		3	5	μA
Input Bias Current		20	30	μA
Input Voltage Range		±1	±1	V
Common Mode Rejection Ratio				
Gain 2 $V_{cm} \pm 1V$, $f \leq 100kHz$		60	60	dB
$V_{cm} \pm 1V$, $f = 5MHz$		60 (typ)	60 (typ)	
Supply Rejection Ratio				
Gain 2 $\Delta V_s = \pm 0.5V$		50	50	dB
Output Offset Voltage				
Gain 1		1.5	1.5	V
Gain 2, Gain 3		1.0	1.5	
Output Common Mode Voltage		2.4/3.4	2.4/3.4	V
Output Voltage Swing		3	3	V_{p-p}
Output Sink Current		2.5	2.5	mA
Output Resistance		20 (typ)	20 (typ)	Ω
Power Supply Current		24	24	mA

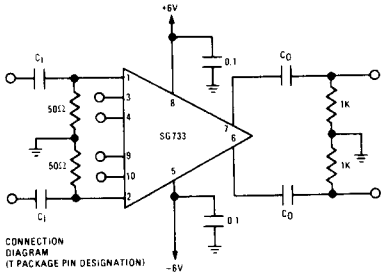
*Parameters apply for $V_S = \pm 6V$, at 25°C only and are min/max limits unless otherwise specified.

[1] Gain Select pins G_{1A} and G_{1B} connected together.

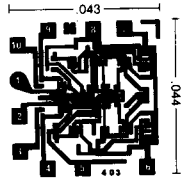
[2] Gain Select pins G_{2A} and G_{2B} connected together.

[3] All Gain Select pins open.

CONNECTION DIAGRAMS



CONNECTION DIAGRAM (T PACKAGE PIN DESIGNATION)



SG733/733C Chip (See T-package diagram for pad functions)