M52334FP

PLL-Split VIF/SIF IC

REJ03F0164-0201
Rev.2.01
Jan 25, 2008

Description

The M52334FP is IF signal-processing IC for VCRs and TVs. It enables the PLL detection system despite size as small as that of conventional quasi-synchronous VIF/SIF detector, IF/RF AGC, SIF limiter and FM detector.

Features

- Video detection output is 2 V_{P-P}. It has built-in EQ AMP.
- The package is a 20-pin flat package, suitable for space saving.
- The video detector uses PLL for full synchronous detection circuit. It produces excellent characteristics of DG, DP, 920 kHz beat, and cross color.
- Dynamic AGC realizes high-speed response with only single filter.
- Video IF and sound IF signal processing are separated from each other. VCO output is used to obtain intercarrier.
- As AFT output voltage uses the APC output voltage, VCO coil is not used.
- Audio FM demodulation uses PLL system, so it has wide frequency range with no external parts and no adjustment.
- This IC corresponds to only inter of NTSC system.

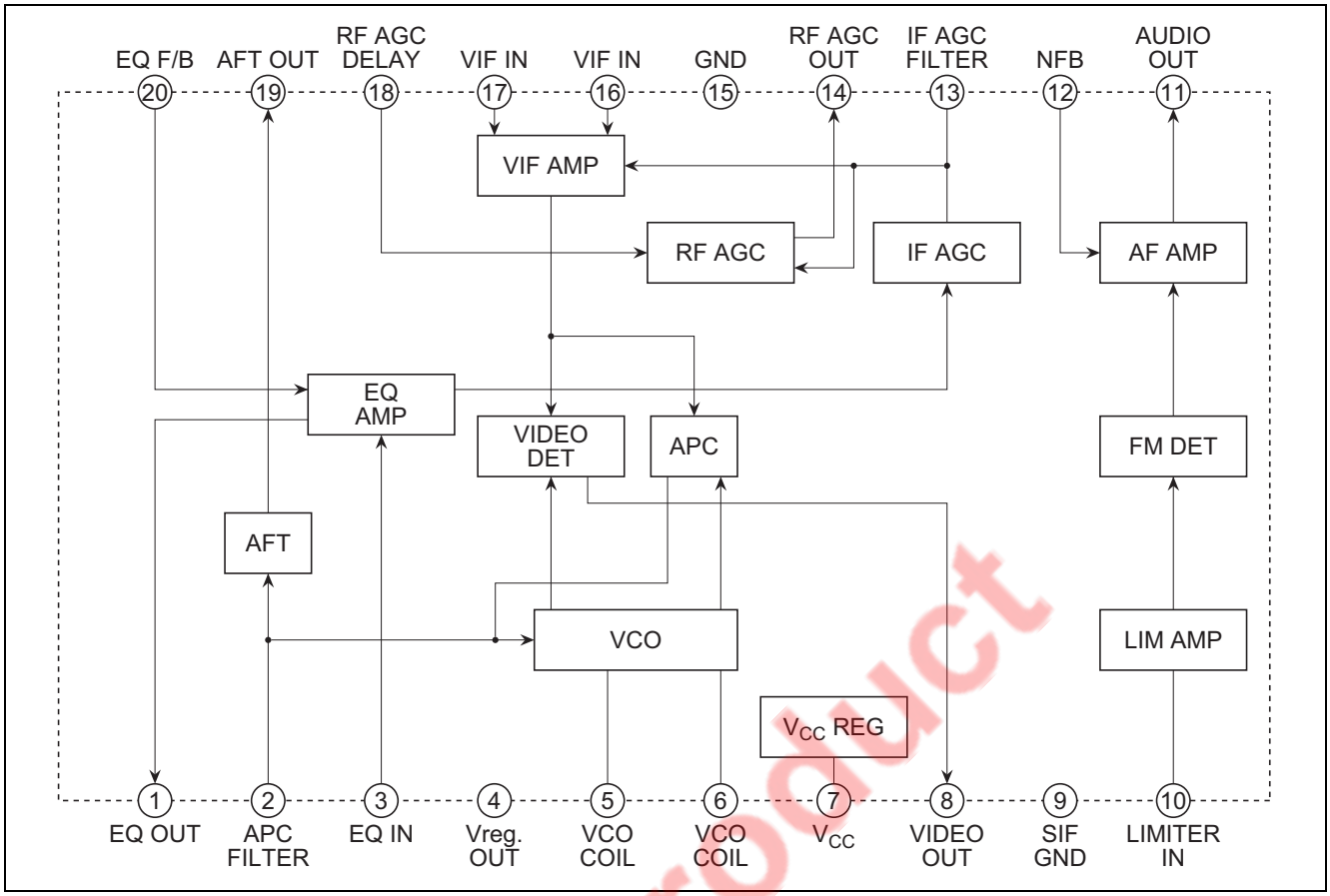
Application

TV sets, VCR tuners

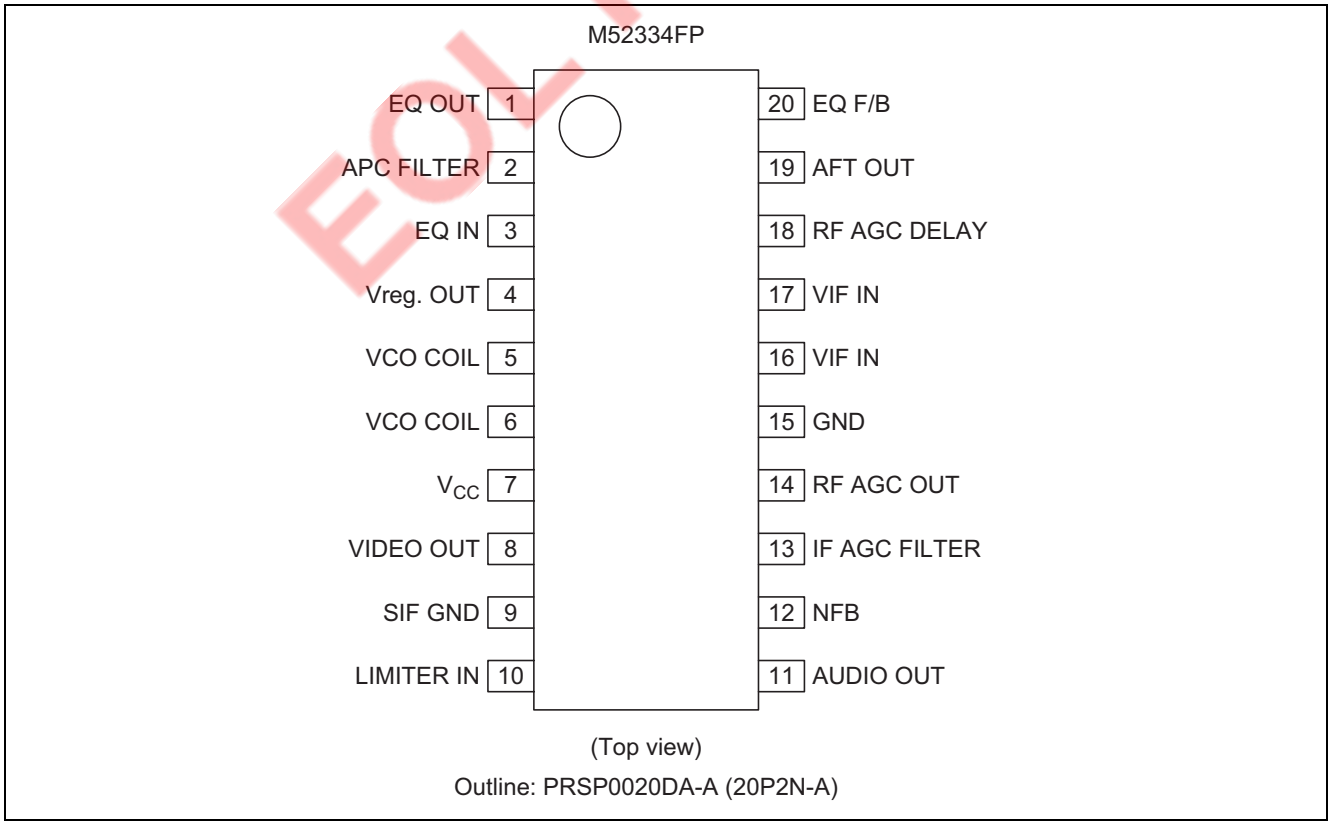
Recommended Operating Condition

- In case of V_{CC} and Vreg. OUT short
  - Supply voltage range: 4.75 to 5.25 V
  - Recommended supply voltage: 5.0 V
- Incase of Vreg. OUT open
  - Supply voltage range: 8.5 to 12.5 V

Block Diagram



Pin Arrangement



(Top view)

Outline: PRSP0020DA-A (20P2N-A)

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Condition
Supply voltage1	V_{CC}	13.2	V	V_{CC} and Vreg. out is not connected to each other.
Supply voltage Vreg. OUT	Vreg. OUT	6.0	V	V_{CC} and Vreg. out is not connected to each other.
Power dissipation	Pd	1225	mW	
Operating temperature	Topr	−20 to +85	°C	
Storage temperature	Tstg	−40 to +150	°C	
Surge voltage resistance	Surge	200	V	Surge protection capacitance 200 pF resistance 0

Electrical Characteristics

(V_{CC} = 9 V, Ta = 25°C, unless otherwise noted.)

Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Limits			Unit	Test Conditions
						Min	Typ	Max		Switches set to position 1 unless otherwise indicated
VIF section										
Circuit current1 V_{CC} = 5V	I_{CC1}	1	A	—	—	33	40.5	47	mA	V_{CC} = 5 V SW4 = 2, SW7 = 2
Circuit current2 V_{CC} = 12V	I_{CC2}	1	A	—	—	31	40.5	49	mA	V_{CC} = 12 V SW7 = 2
Vreg voltage2	V_{CC2}	1	TP4	—	—	4.7	5.00	5.3	V	V_{CC} = 12 V
Video output DC voltage1	V1	1	TP1A	—	—	3.45	3.9	4.35	V	SW13 = 2 V13 = 0 V
Video output voltage8	Vo det8	1	TP8	VIF IN	SG1	0.85	1.1	1.35	V_{P-P}	
Video output voltage1	Vo det	1	TP1A	VIF IN	SG1	1.85	2.2	2.55	V_{P-P}	
Video S/N	Video S/N	1	TP1B	VIF IN	SG2	51	56	—	dB	SW1 = 2
Video band width	BW	1	TP1A	VIF IN	SG3	5.0	7.0	—	MHz	SW13 = 2 V13 = variable
Input sensitivity	VIN MIN	1	TP1A	VIF IN	SG4	—	48	52	dBμ	
Maximum allowable input	VIN MAX	1	TP1A	VIF IN	SG5	101	105	—	dBμ	
AGC control range input	GR	—	—	—	—	50	57	—	dB	
IF AGD voltage	V13	1	TP13	VIF IN	SG6	2.85	3.15	3.45	V	
Maximum IF AGC voltage	V13H	1	TP13	—	—	4.0	4.4	—	V	
Minimum IF AGC voltage	V13L	1	TP13	VIF IN	SG7	2.2	2.4	2.6	V	
Maximum RF AGC voltage	V14H	1	TP14	VIF IN	SG2	8.0	8.7	—	V	SW13 = 2 V13 = 4 V
Minimum RF AGC voltage	V14L	1	TP14	VIF IN	SG2	—	0.1	0.5	V	SW13 = 2 V13 = 1 V

(V_{CC} = 9 V, Ta = 25°C, unless otherwise noted.)

Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Limits			Unit	Test Conditions
						Min	Typ	Max		Switches set to position 1 unless otherwise indicated
RF AGC operation voltage	V14	1	TP14	VIF IN	SG8	86	89	92	dBμ	
Capture range U	CL-U	1	TP1A	VIF IN	SG9	0.8	1.3	—	MHz	
Capture range L	CL-L	1	TP1A	VIF IN	SG9	1.4	2.0	—	MHz	
Capture range T	CL-T	1	—	—	—	2.5	3.3	—	MHz	
AFT sensitivity		1	TP19	VIF IN	SG10	20	30	70	mV/kHz	
AFT maximum voltage	V19H	1	TP19	VIF IN	SG10	7.7	8.2	—	V	
AFT minimum voltage	V19L	1	TP19	VIF IN	SG10	—	0.7	1.2	V	
AFT defeat 1	AFT def1	1	TP19	VIF IN	—	4.2	4.5	4.8	V	
Inter modulation	IM	1	TP3A	VIF IN	SG11	35	42	—	dB	SW13 = 2 V13 = variable
Differential gain	DG	1	TP3A	VIF IN	SG12	—	2	5	%	
Differential phase	DP	1	TP3A	VIF IN	SG12	—	2	5	deg	
Sync. tip level	V3 SYNC	1	TP3A	VIF IN	SG2	1.0	1.4	1.8	V	
VIF input resister	RINV	2	TP17	—	—	—	1.2	—	kΩ	
VIF input capacitance	CINV	2	TP17	—	—	—	5	—	pF	
SIF section										
AF output DC voltage	V1	1	TP11	—	—	3.5	4.4	5.3	V	
AF output	VoAF	1	TP11	SIF IN	SG16	565	790	1125	mVrms	
AF output distortion	THD AF	1	TP11	SIF IN	SG16	—	0.4	0.9	%	
Limiting sensitivity	LIM	1	TP11	SIF IN	SG17	—	42	55	dBμ	
AM rejection	AMR	1	TP11	SIF IN	SG18	55	65	—	dB	
AF S/N	AF S/N	1	TP11	SIF IN	SG19	55	65	—	dB	

Electrical Characteristics Test Method

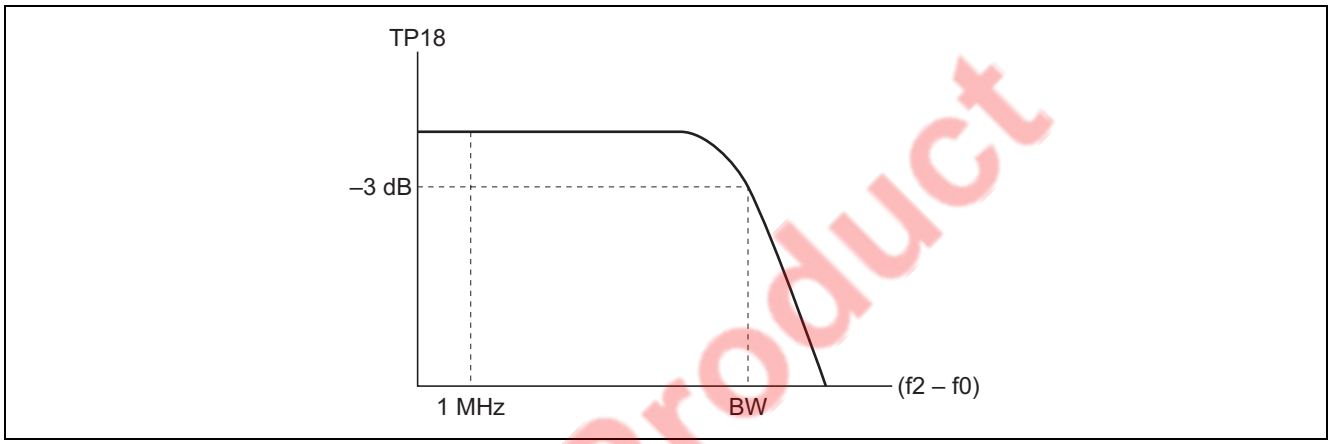
Video S/N

Input SG2 into VIF IN and measure the video out (Pin 3) noise in r.m.s at TP3-B through a 5 MHz (–3 dB) L.P.F.

$$S/N = 20 \log \left(\frac{0.7 \bullet Vo\ det}{NOISE} \right) \quad (dB)$$

BW Video Band Width

1. Measure the 1 MHz component level of EQ output TP3A with a spectrum analyzer when SG3 (f2 = 44.75 MHz) is input into VIF IN. At that time, measure the voltage at TP13 with SW13, set to position 2, and then fix V13 at that voltage.
2. Reduce f2 and measure the value of (f2 – f0) when the (f2 – f0) component level reaches –3 dB from the 1 MHz component level as shown below.



VIN MIN Input Sensitivity

Input SG4 (Vi = 90 dBμ) into VIF IN, and then gradually reduce Vi and measure the input level when the 20 kHz component of EQ output TP3A reaches –3 dB from Vo det level.

VIN MAX Maximum Allowable Input

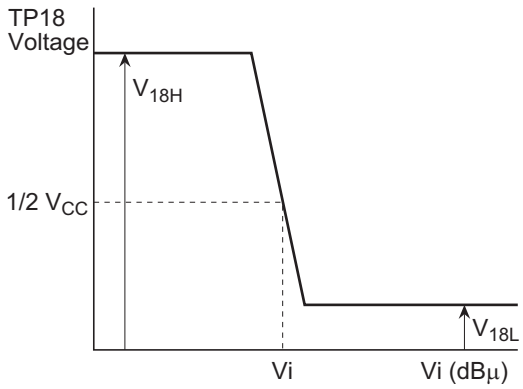
1. Input SG5 (Vi = 90 dBμ) into VIF IN, and measure the level of the 20 kHz components of EQ output.
2. Gradually increase the Vi of SG and measure the input level when the output reaches –3 dB.

GR AGC Control Range

$$GR = VIN\ MAX - VIN\ MIN\ (dB)$$

V18 RF AGC Operating Voltage

Input SG8 into VIF IN, and gradually reduce Vi and then measure the input level when RF AGC output TP14 reaches 1/2 V_{CC}, as shown below.



CL-U Capture Range

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks.

CL-U = fU – 45.75 (MHz)

CL-L Capture Range

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks.

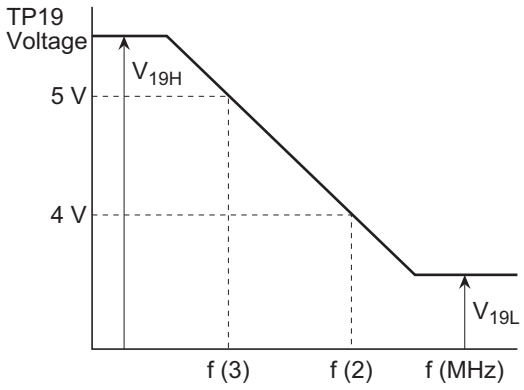
CL-L = 45.75 – fL (MHz)

CL-T Capture Range

CL-T = CL-U + CL-L (MHz)

μAFT Sensitivity, V_{19H} AFT Maximum Voltage, V_{19L} AFT Minimum Voltage

1. Input SG10 into VIF IN, and set the frequency of SG 10 so that the voltage of AFT output TP19 is 5 V. This frequency is named f (3).
2. Set the frequency of SG10 so that the AFT output voltage is 4 V. This frequency is named f (2).
3. In the graph, maximum and minimum DC voltage are V_{19H} and V_{19L}, respectively.



$$\mu = \frac{1000\ (mV)}{f\ (2) - f\ (3)\ (kHz)} \quad (mV/kHz)$$

IM Intermodulation

1. Input SG11 into VIF IN, and measure EQ output TP3A with an oscilloscope.
2. Adjust AGC filter voltage V13 so that the minimum DC level of the output waveform is 1.0 V.
3. At this time, measure, TP3A with a spectrum analyzer. The intermodulation is defined as a difference between 0.92 MHz and 3.58 MHz frequency components.

LIM Limiting Sensitivity

1. Input SG17 (Vi = 90 dBμ) into SIF input, and measure the 400 Hz component level of AF output TP11.
2. Lower the input level of SG17, and measure the level of SG17 when the VoAF level reaches –3 dB.

AMR AM Rejection

1. Input SG18 into SIF input, and measure the output level of AF output TP11. This level is named VAM.
2. AMR is;

$$AMR = 20 \log \left(\frac{VoAF\ (mVrms)}{VAM\ (mVrms)} \right) \quad (dB)$$

AF S/N

1. Input SG19 into SIF input, and measure the output noise level of AF output TP11. This level is named VN.
2. S/N is;

$$S/N = 20 \log \left(\frac{VoAF\ (mVrms)}{VN\ (mVrms)} \right) \quad (dB)$$

The Note in the System Setup

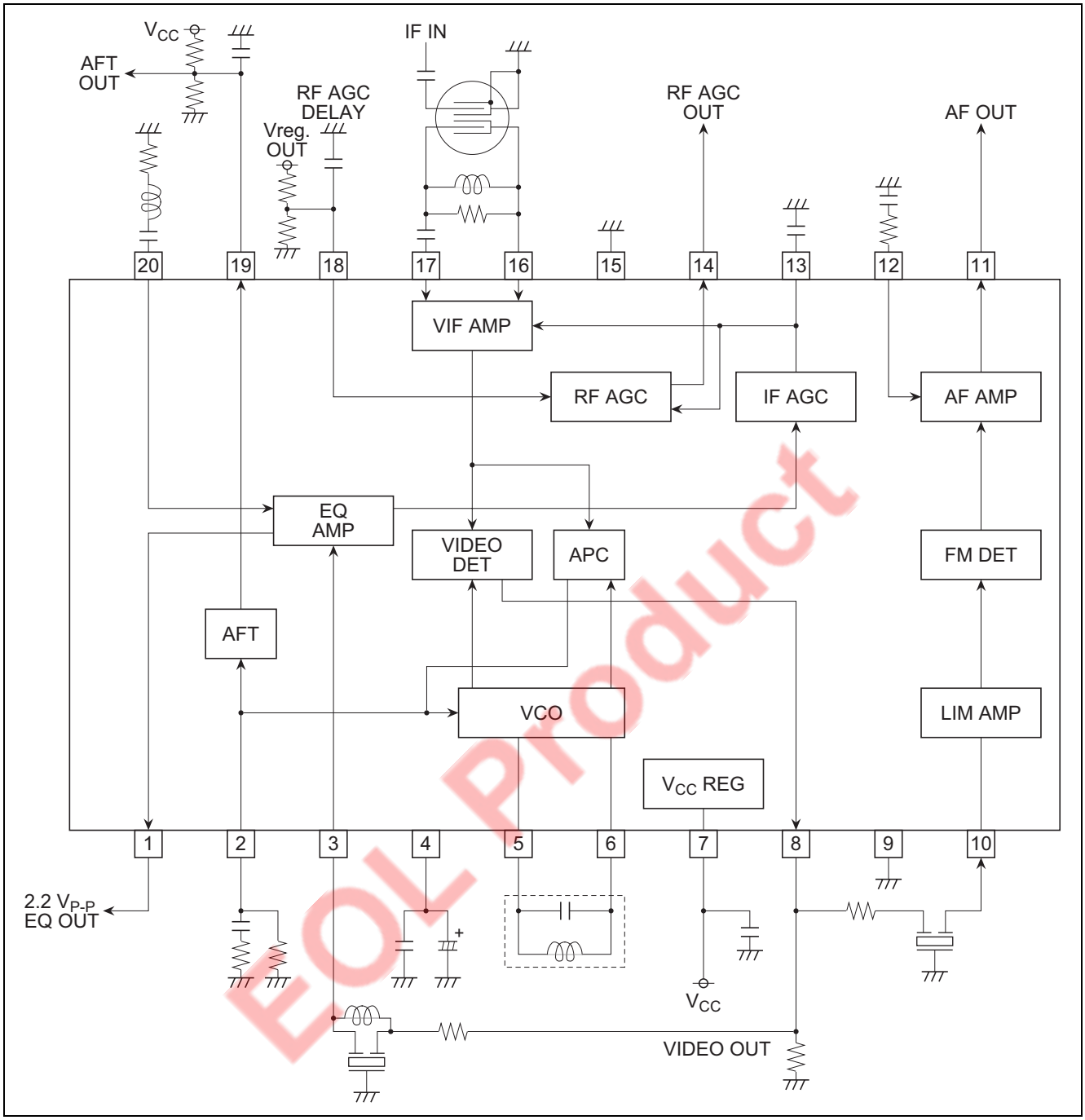
M52334FP has 2 power supply pins of V_{CC} (pin 7) and Vreg. OUT (pin 4). Pin 7 is for AFT output, RF AGC output circuits and 5 V regulated power supply circuit and pin 4 is for the other circuit blocks. In case M52334FP is used together with other ICs like VIF operating at more than 5 V, the same supply voltage as that of connected ICs is applied to V_{CC} and Vreg. OUT is opened. The other circuit blocks, connected to Vreg. OUT are powered by internal 5 V regulated power supply.

In case the connecting ICs are operated at 5 V, 5 V is supplied to both V_{CC} and Vreg. OUT.

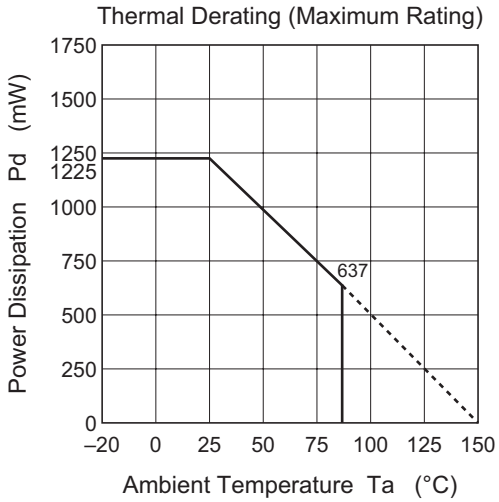
Input Signal

SG No.	Signals (50 Ω Termination)
1	f_0 = 45.75 MHz AM 20 kHz 77.8% 90 dBμ
2	f_0 = 45.75 MHz 90 dBμ CW
3	f_1 = 45.75 MHz 90 dBμ CW (Mixed signal) f_2 = Frequency variable 70 dBμ CW (Mixed signal)
4	f_0 = 45.75 MHz AM 20 kHz 77.8% level variable
5	f_0 = 45.75 MHz AM 20 kHz 14.0% level variable
6	f_0 = 45.75 MHz 80 dBμ CW
7	f_0 = 45.75 MHz 110 dBμ CW
8	f_0 = 45.75 MHz CW level variable
9	f_0 = Variable AM 20 kHz 77.8% 90dBμ
10	f_0 = Variable 90 dBμ CW
11	f_1 = 45.75 MHz 90 dBμ CW (Mixed signal) f_2 = 42.17 MHz 80 dBμ CW (Mixed signal) f_3 = 41.25 MHz 80 dBμ CW (Mixed signal)
12	f_0 = 45.75 MHz 87.5% TV modulation ten-step waveform Sync tip level 90 dBμ
13	f_1 = 41.25 MHz 103 dBμ CW
14	f_1 = 41.25 MHz 70 dBμ CW
15	f_1 = 45.75 MHz 90 dBμ CW (Mixed signal) f_2 = 41.25 MHz 70 dBμ CW (Mixed signal)
16	f_0 = 4.5 MHz 90 dBμ FM 400 Hz ± 25 kHz dev
17	f_0 = 4.5 MHz FM 400 Hz ± 25 kHz dev level variable
18	f_0 = 4.5 MHz 90 dBμ AM 400 Hz 30%
19	f_0 = 4.5 MHz 90 dBμ CW

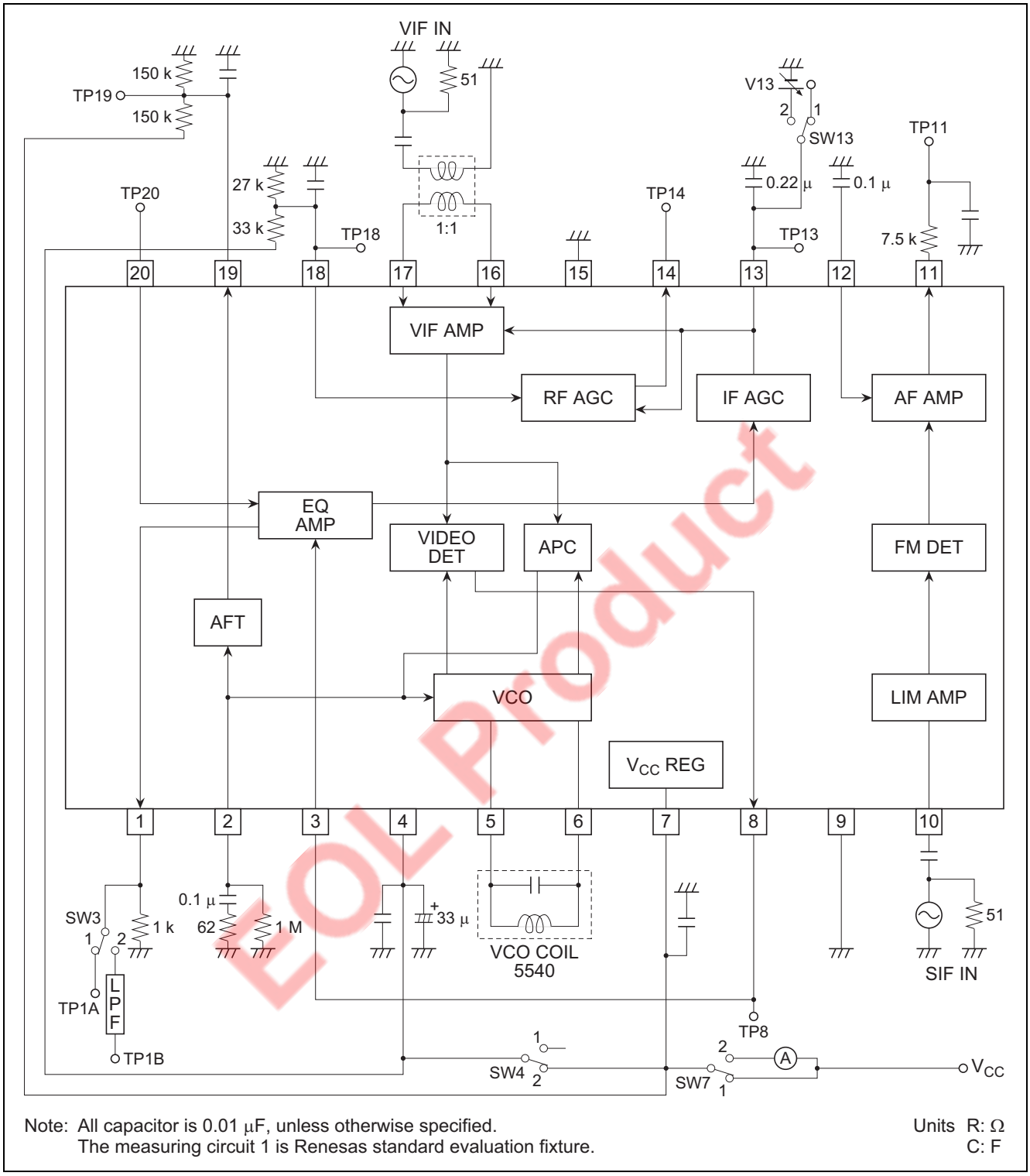
Test Circuit



Typical Characteristics



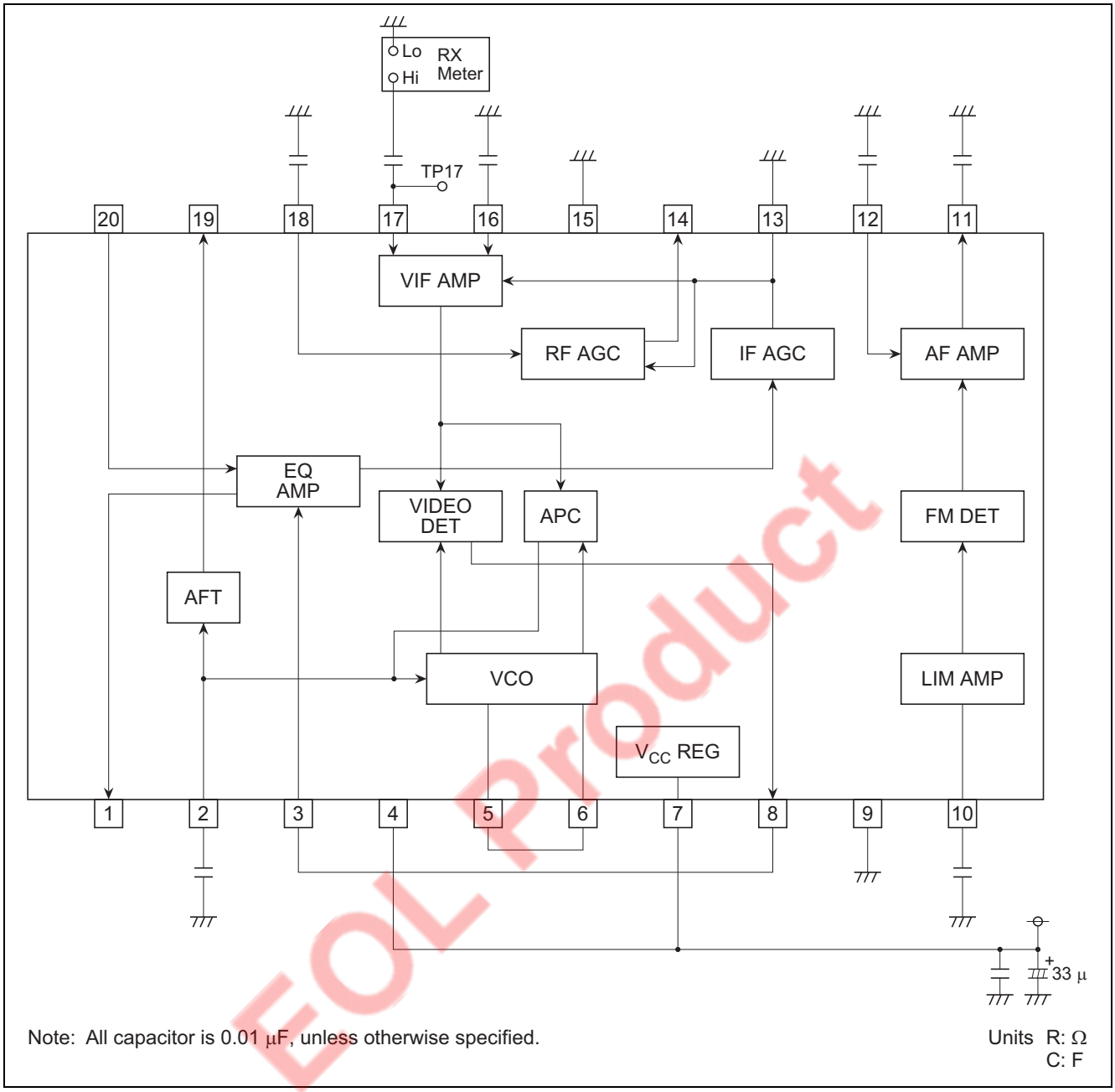
Application Example 1



Note: All capacitor is 0.01 µF, unless otherwise specified.
The measuring circuit 1 is Renesas standard evaluation fixture.

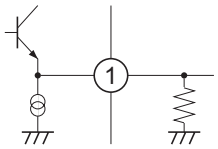
Units R: Ω
C: F

Application Example 2



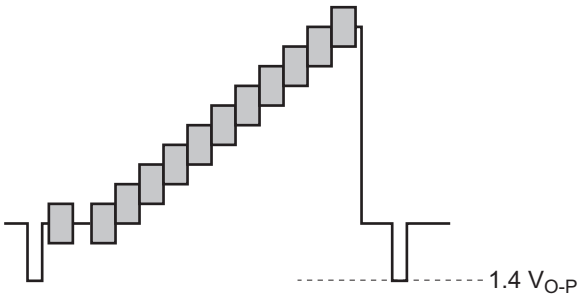
Pin Description

Pin 1 (EQ OUT)

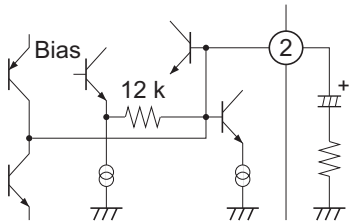


Internal driving current: 3 mA

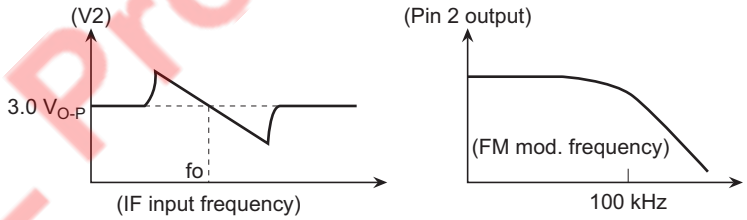
An output amplitude is positive 2.2 V_{P-P} in the case of 87.5% video modulation.



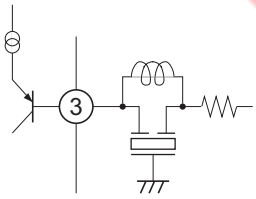
Pin 2 (APC FILTER)



In the locked state, the cut-off frequency of the filter is adjusted effectively by an external resistor so that it will be in the range of around 30 to 200 kHz.
In case the cut-off frequency is lower, the pull-in speed becomes slow. On the other hand, a higher cut-off frequency widen the pull-in range and band width, which results in a degradation in the S/N ratio. So, in the actual TV system design, the appropriate constant should be chosen for getting desirable performance considering above conditions.

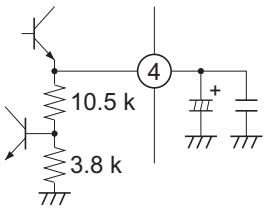


Pin 3 (EQ IN)



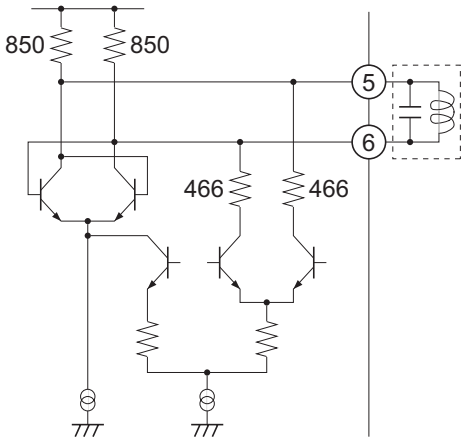
It is an open-base input.
The IF AGC does not work correctly, unless a DC element of pin 8 output is applied to it.

Pin 4 (Vreg. OUT)



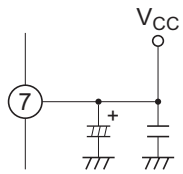
It is a regulated 5 V output which has current drive capability of approximately 10 mA.

Pin 5, Pin 6 (VCO COIL)



Connecting a tuning coil and capacitor to these pins enables an oscillation.
The tuning capacitor of about 30 pF is recommended.
The oscillation frequency is tuned in f0.
In the actual adjustment, the coil is tuned so that the AFT voltage is reached to $V_{CC}/2$ with f0 as an input.
The printed pattern around these pins should be designed carefully to prevent an pull-in error of VCO, caused by the laekage interference from the large signal level oscillator to adjacent pins.
The interconnection should be designed as short as possible.
In case the printed pattern has the interference problem, a capacitor of about 1 pF is connected between pin 5 or 6 and GND so as to cancel the interference and keep enough pull-in range even in a weak electric field.

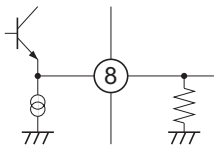
Pin 7 (V_{CC})



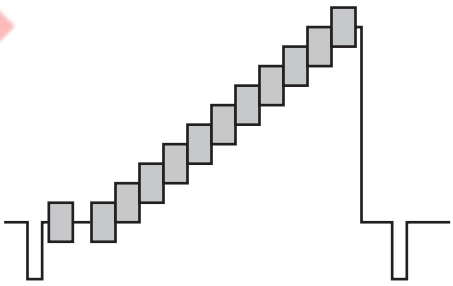
The recommended supply voltage is 5 V or 9 to 12 V.
In the case of 5 V supply, it should be tied to pin 17.
In the case of 9 to 12 V supply, a regulated output of 5 V are available in pin 17.

Pin 8 (VIDEO OUT)

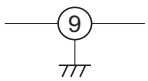
An output amplitude is positive 2 V_{P-P} in the case of 87.5% video modulation.



Internal driving current: 2 mA

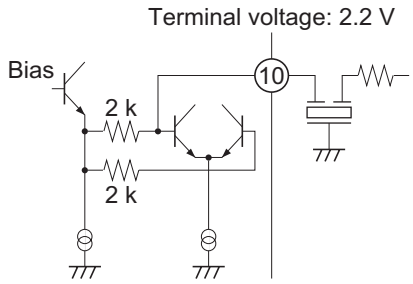


Pin 9 (SIF GND)



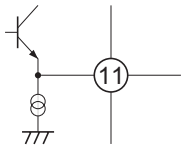
It is ground (GND) for the SIF.

Pin 10 (LIMITER IN)



The input impedance is 2 kΩ.

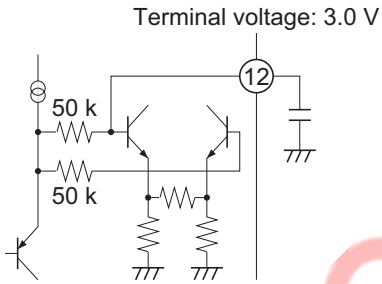
Pin 11 (AUDIO OUT)



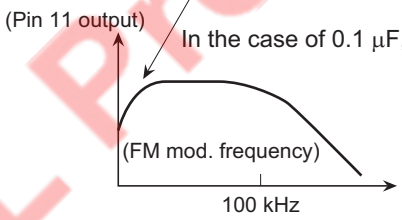
Internal driving current: 1 mA

The FM detector can respond to the 4.5 MHz intercarrier signal without an adjustment and external components by adopting the PLL technique.
The output DC voltages of 4.4 V_{O-P} and 2.4 V_{O-P} are in the V_{CC} of 9 V and 5 V, respectively.
Since its output frequency is more than 100 kHz in no loading condition, it can also respond to the multi audio broadcasting.

Pin 12 (NFB)

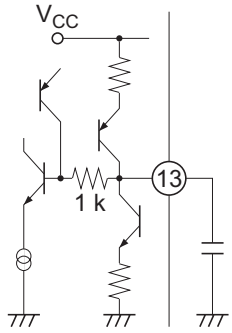


The frequency response of the audio output is set by the external capacitor of pin 12.

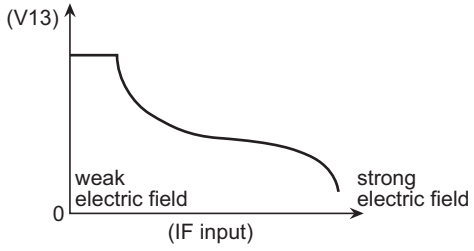


Connecting series resistor to the capacitor above, can reduce an audio output amplitude.

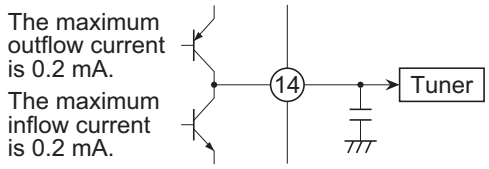
Pin 13 (IF AGC FILTER)



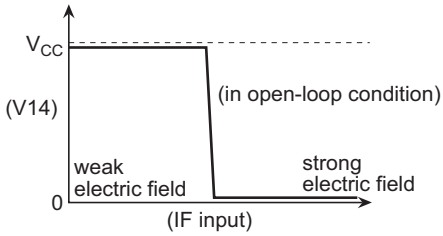
In spite of the 1-pin filter configuration, 2-pin filter characteristics are available by utilizing the dynamic AGC circuit.



Pin 14 (RF AGC OUT)

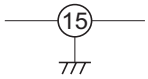


A current mode output is available in the reverse AGC operation.



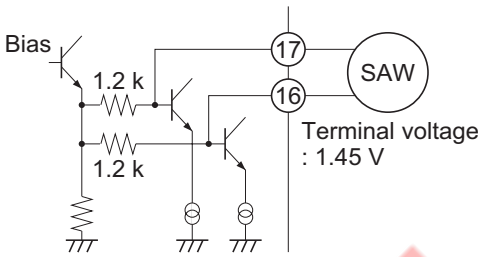
Note: Connecting a nonpolarity capacitor of 1 μF between pin 14 and pin 18 improves AGC operating speed.
In that case, the capacitors between pin 14/pin 18 and ground should be removed.

Pin 15 (GND)



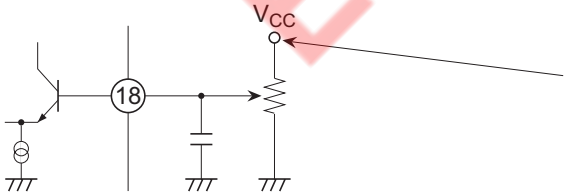
It is GND pin except for SIF.

Pin 16, Pin 17 (VIF IN)



It should be designed considering careful impedance matching with the SAW filter.

Pin 18 (RF AGC DELAY)

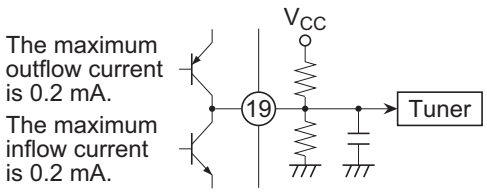


An applied voltage to the pin 18 is for changing a RF AGC delay point.

In the 3-in-1 type application, the regulated output from the regulator is suitable for a power supply (V_{CC}) to it, because there may be difference between the tuner and main board supply.

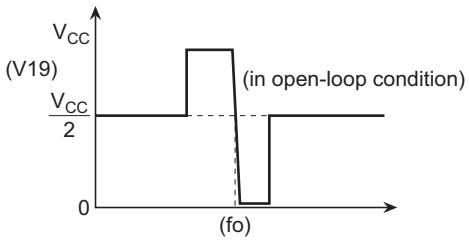
TV tuner, VIF demodulator and RF modulator are togetherin one package.

Pin 19 (AFT OUT)



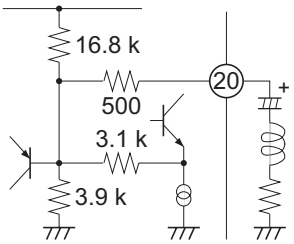
Since an AFT output is provided by a high impedance source, the detection sensitivity can be set by an external resistor.
The muting operation will be on in following two cases;

1) the APC is out of locking,
2) the video output becomes small enough in a weak electric field.

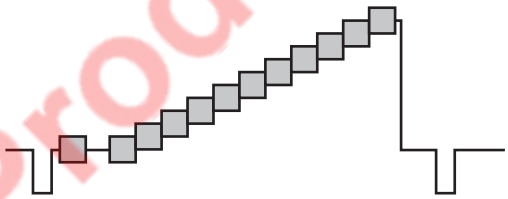


Note: In the case of 5 V supply, it should be considered that the maximum AFT and RF AGC output are less than 4.2 V and 4.7 V, respectively.

Pin 20 (EQ F/B)

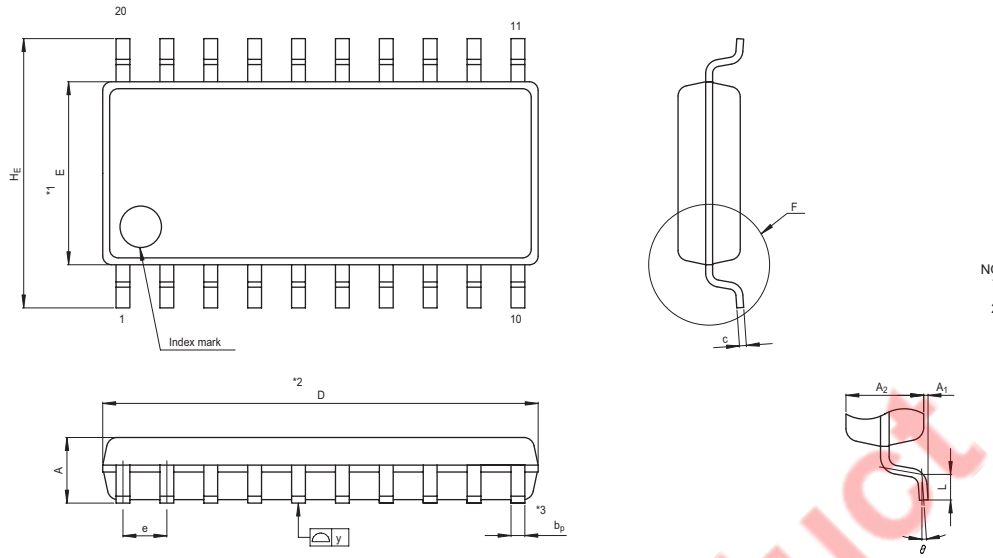


Both the external coil and capacitor determine the frequency response of EQ output.
The series connected resistor is for damping.



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

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Colophon .7.2