85 MHz Direct Digital Synthesizer

AD9955

FEATURES

85 MHz Minimum Clock Rate
32-Bit Phase Accumulator
12-Bit Sine Output
>90 dB Spurious Free Dynamic Range
Continuous Frequency Update
On-Board Data Ready Signal

APPLICATIONS

Frequency Synthesizers
DDS Tuning
Digital Demodulation
FM Modulators

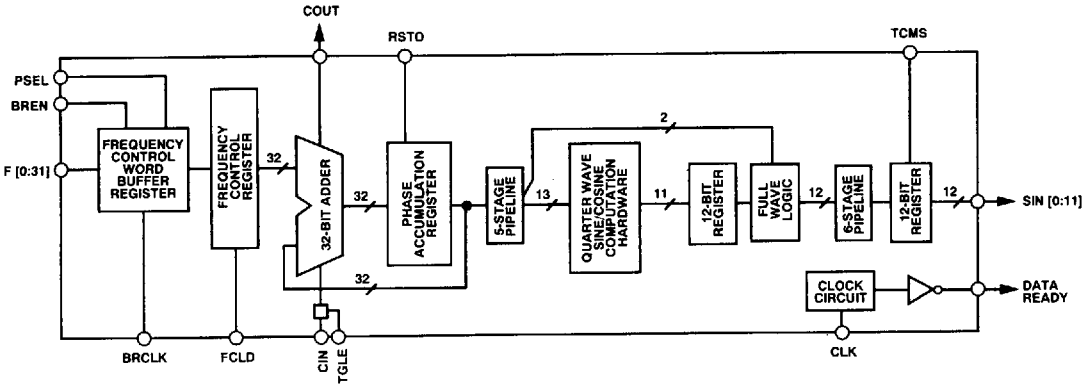
GENERAL DESCRIPTION

The AD9955 is a 85 MHz direct digital synthesizer for frequency synthesis applications. It comprises a 32-bit phase accumulator and a 15-bit phase-to-12-bit sine amplitude converter. The control logic is CMOS compatible, and the clock input is TTL. CMOS outputs are latched on board, and a data ready signal is provided.

Designed for applications in communications, instrumentation, and military systems, the AD9955 can be combined with a clock reference and a DAC such as the AD9713B or AD9721 to form a digitally-controlled analog frequency reference.

The AD9955 is available in an 80-lead plastic quad flatpack (PQFP) for commercial (0°C to +70°C) temperature range applications. Contact the factory for information concerning the availability of a military temperature range device.

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; f_{CLK} = 40 MHz; C_L = 20 pF, unless otherwise noted)

Parameter (Conditions)	Temperature	Test Level	AD9955 Min	AD9955 Typ	AD9955 Max	Units
CMOS INPUTS[1]						
Logic "1" Voltage	Full	II	3.5			V
Logic "0" Voltage	Full	II			1.5	V
Logic "1" Current	Full	II			1.0	μA
Logic "0" Current	Full	II			−1.0	μA
Input Capacitance	+25°C	V		10		pF
CMOS OUTPUTS						
Logic "1" Voltage (V_{IH})	Full	II	4.5			V
Logic "0" Voltage (V_{IL})	Full	II			0.4	V
Logic "1" Current	Full	II			12	mA
Logic "0" Current	Full	II			12	mA
Output Capacitance	+25°C	V		3		pF
TTL INPUTS[2]						
Logic "1" Voltage	Full	IV	2.0			V
Logic "0" Voltage	Full	II			0.8	V
Logic "1" Current	Full	II			1.0	μA
Logic "0" Current	Full	II			−1.0	μA
Input Capacitance	+25°C	V		4		pF
POWER SUPPLIES						
$+V_S$ Current[3]						
CLK = 50 MHz	Full	IV		120	160	mA
CLK = 100 MHz	+25°C	V		240		mA
Nominal Power Dissipation						
CLK = 50 MHz	+25°C	V		600		mW
CLK = 100 MHz	+25°C	V		1.2		W
Relative to Frequency	+25°C	V		11.5		mW/MHz
AC SPECIFICATIONS[4]						
Clock Update Rate (CLK)[5]	Full	IV	85	100		MHz
Frequency Update Rate (BRCLK)[6]	Full	II	40			MHz
Clock Pulse Width						
CLK Digital "1"	Full	IV	7.9	5.7		ns
CLK Digital "0"	Full	IV	3.8	2.2		ns
Frequency Update Pulse Width						
BRCLK Digital "1"	Full	II	10			ns
BRCLK Digital "0"	Full	II	10			ns
Input Rise/Fall Times						
CLK Rise Time	Full	IV			2	ns
CLK Fall Time	Full	IV			2	ns
BRCLK Rise Time	Full	IV			5	ns
BRCLK Fall Time	Full	IV			5	ns
BRCLK Input Timing						
Setup Time (t_{CS}, t_{ES})[7]	Full	II	5	2		ns
Hold Time (t_{CH}, t_{EH})[7]	Full	IV	5	1.8		ns
CLK Input Timing						
Setup Time (t_{LS})[8]	Full	IV	2.0	0.7		ns
Hold Time (t_{LH})[8]	Full	IV	2.0	0.7		ns
RESET 0 Timing						
Setup Time (t_{RS})[9]	Full	IV	6			ns
Hold Time (t_{RH})[9]	Full	IV	6			ns
Output Timing Characteristics						
Data Output Delay (t_{OD})[10]	Full	IV	3.4	6.1	8.7	ns
DRDY Output Delay (t_{DR})[10]	Full	IV	4.7	7.5	10	ns
Output Data Setup Time (t_{OS})[11]	Full	IV	0.8	1.9		ns
Carry Output Delay[12]	+25°C	V		7.7		ns
Spurious-Free Dynamic Range (SFDR)						
Worst Case Spur[13]	+25°C	V		>90		dBc
Latency of Initial Data[14]	+25°C	V		14		Clock Cycles

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NOTES
[1]Includes F[0:31], PSEL, BREN, FCLD, CIN, TGLE, BRCLK, TCMS, and RST0.
[2]Only the clock (CLK) is TTL compatible.
[3]f_{OUT} = 1/2 f_{CLK}. See performance curves.
[4]Nominal conditions (V_{IH} = 3.4 V; V_{IL} = 0.4 V).
[5]Based on minimum clock pulse width duty cycle (68% HIGH @ 85 MHz).
[6]This specification defines the maximum rate at which the output frequency tuning word (F[0:31]) can be updated.
[7]Referenced to 2.5 V point of rising edge of BRCLK, specified for F[0:31], BREN.
[8]Referred to rising edge of CLK, specified for FCLD. CIN setup time is typically 1.2 ns, specified for FCLD, CIN.
[9]Referred to 1.6 V point of the rising edge of CLK. See Timing Diagram.
[10]Referenced to 1.6 V point of the rising edge of CLK for 1.6 V point of the rising/falling edge of SIN [0:11]; or the falling edge of DRDY. Load is shown below.
[11]Referenced from 1.6 V point of the rising/falling edge of SIN[0:11] to 1.6 V point of the falling edge of DATA READY. Specified driving AD9713B; no additional capacitive load.
[12]Referenced from 1.6 V point of rising edge of CLK to 1.6 V point of the rising/falling edge of COUT.
[13]Based on proprietary phase-to-sine algorithm, TGLE HIGH.
[14]Referred to CLK for FCLD high. See Timing Diagram.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C; parameter is guaranteed by design and characterization at temperature extremes.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.

Parameters based on characterization testing have limits based on 6 sigma of a normal distribution; typical values are the mean of the distribution.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$) . . . . . −0.5 V to +7 V
Input Voltage . . . . . −0.5 V to $+V_S$ +0.5 V
Output Voltage Swing . . . . . −0.5 V to $+V_S$ +0.5 V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Maximum Junction Temperature[2] . . . . . +150°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +250°C

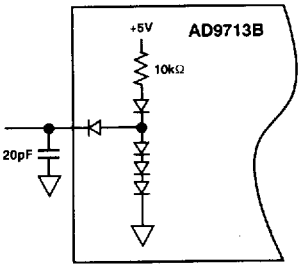
NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedance; part soldered in place:
θ_{JA} = 62°C/W
θ_{JC} = 7°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD9955KS-66[2]	0°C to +70°C	80-Terminal Plastic Quad Flatpack	S-80
AD9955KS-6[3]	0°C to +70°C	80-Terminal Plastic Quad Flatpack	S-80
AD9955/PCB	N/A	DDS Evaluation Board	

NOTES
[1]For outline information see Package Information section.
[2]Model AD9955KS-66 units are shipped in a standard JEDEC tray; minimum order quantity is 66 units (1 full tray).
[3]AD9955KS-6 units are shipped in a nonstandard tray; minimum order quantity is 6 units (1 full tray). Three nonstandard trays will fit in a standard JEDEC tray outline, allowing use with standard assembly equipment. Contact factory for details.

NOTE: All units are dry packed to inhibit moisture absorption. Units which are exposed to air for more than 48 hours should be baked for 24 hours at +125°C prior to assembly.

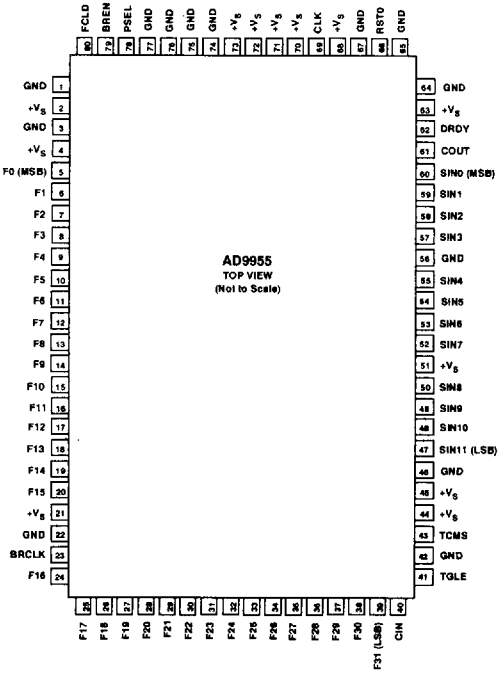


AD9955 Load Circuit

AD9955 PIN DESCRIPTIONS

Name	Description
GND	Ground Reference Voltage Connection.
$+V_S$	Positive voltage power connection, nominally +5 V.
BRCLK	Buffer Register Clock. Data inputs are loaded into the Frequency Control Word Buffer Register on the rising edge of BRCLK when register is enabled (BREN input at Logic "1").
CLK	System Clock. Continuous TTL signal for synchronizing all internal operations, except loading of Frequency Control Word Buffer Register; rising edge initiates synchronization.
F[0:31]	32 parallel data inputs for loading frequency tuning word.
BREN	Buffer Load Enable Signal. Enables loading of data into the Frequency Control Word Buffer Register. If BREN is logic "0," register retains its contents. If BREN is Logic "1," theFrequency Control Word Buffer Register either (1) parallel loads the data present at F[0:31] inputs (PSEL = HIGH) or (2) serially shifts data present at F[31] input (PSEL = LOW).
FCLD	Frequency Control Load Enable Signal. FCLD = HIGH enables loading of data from Frequency Control Word Buffer Register into Frequency Control Register. Loading takes place on next rising edge of CLK signal. FCLD = LOW disables loading of data.
DRDY	Data Ready Signal. Output data (SIN [0:11]) is valid on the rising edge of DRDY, which tracks propagation delay variations of the output data vs. temperature. The duty cycle of DRDY is dependent on the duty cycle of the CLK input. The DRDY signal should be used only for applications which have a very high clock rate (85 Msps) and require operation over a wide temperature range. Normally allowed to float.
CIN	Carry-In signal is provided as the carry input to the least significant bit (LSB) of the 32-bit adder in the phase accumulator. This signal is used as the carry input only if the TGLE signal is a logic zero; carry has 1 LSB weight, and is used for stacking units for 64-bit DDS. Normally tied to ground.
TGLE	Carry Toggle Enable. When HIGH, the CIN signal is disabled, and the Carry-In toggles internally between HIGH and LOW on each clock (CLK) cycle to reduce the worst case spurious response of the digital output signal by 3.92 dB. Normally tied to ground.
TCMS	Twos Complement/Magnitude Mode Select. Selects binary output format of data on SIN[0:11] outputs. If TCMS is a Logic "1," format of output data at SIN[0:11] is in twos complement format. If TCMS is a Logic "0," data is binary unsigned magnitude format. Normally tied to ground.
SIN[0:11]	12 parallel data bits comprising the sine data output. Frequency of the sine data outputs is defined by the Frequency Control Register (Δ phase) as $f_{OUT} = f_{CLK}\left(\frac{\Delta\ phase}{2^{32}}\right)$ Binary data format of 12-bit samples is either twos complement or unsigned magnitude, determined by TCMS signal.
RST0	Reset Phase to Zero Signal. Activates synchronous reset of the Phase Accumulation Register to a binary value of "0," or zero radians. Reset is enabled when RST0 is a Logic "1" and takes place on rising edge of system clock (CLK). Normally low.
COUT	Carry-Out signal output of the 32-bit adder in the phase accumulator; used for stacking two AD9955 units for 64-bit DDS. Normally allowed to float.
PSEL	Parallel/Serial Frequency Control Word Buffer Input Selector. Selects mode for loading the Buffer Register. If a load is enabled (BREN = "1"), and PSEL is a Logic "1," data is parallel loaded into the Frequency Control Word Buffer Register from the F0:31] inputs on the next rising edge of BRCLK. If a load is enabled and PSEL is a Logic "0," data is serially shifted into the Frequency Control Word Buffer Register from the F[31] input on rising edge of BRCLK.

PIN DESIGNATIONS



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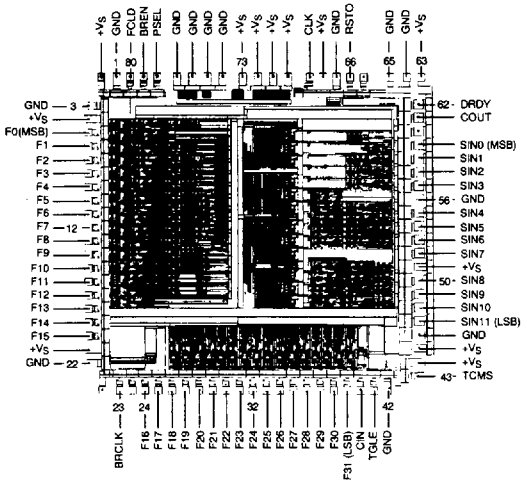
DIE INFORMATION

Die Dimensions	.215 × 199 × 20.7 (±1) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	Ground
Passivation	Oxynitride
Die Attach	Epoxy
Bond Wire	Gold



AD9955 Chip Layout

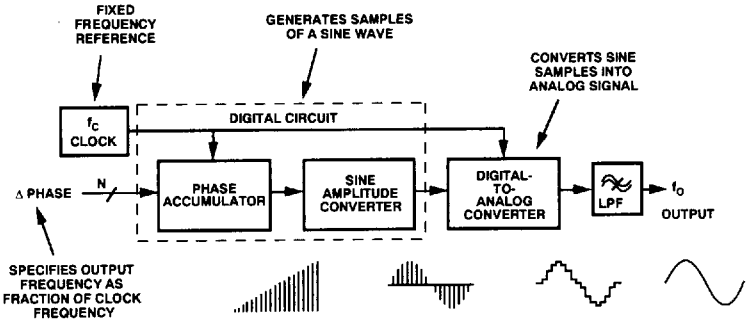


Figure 1. Block Diagram of DDS Generator

DDS

Direct digital synthesis (DDS) is a method of deriving a wide-band, digitally controlled frequency (sine wave) synthesizer from a single reference frequency (system clock).

The circuit has three major components:

1. Phase accumulator
2. Phase-to-amplitude converter
3. Digital-to-analog converter

These major stages and their relationships to one another are illustrated in the block diagram shown above.

The phase accumulator is a digital device which generates the phase increment of the output waveform. Its input is a digital word which (with the reference oscillator) determines the frequency of the output waveform. The output of the phase accumulator stage represents the current phase of the generated waveform. In effect, the accumulator serves as a variable-frequency oscillator generating a digital ramp. The frequency of the signal is defined by Δphase as

$$f_{OUT} = \frac{\Delta phase}{\Delta phase_{MAX}} f_{CLOCK} = \frac{\Delta phase}{2^N} f_{CLOCK}$$

Translating phase information from the phase accumulator into amplitude data takes place in the phase-to-amplitude converter. This is most commonly accomplished by means of a look-up table (LUT) stored in memory, but may be calculated instead using a digital algorithm to minimize circuit complexity and/or increase the update rate.

In the final step of frequency synthesis, amplitude data is converted into an analog signal. This is done by a digital-to-analog (D/A) converter which must have good linearity; low glitch impulse; and fast, symmetrical rise and fall times. When it does, the frequency synthesizer is able to produce a spectrally pure waveform.

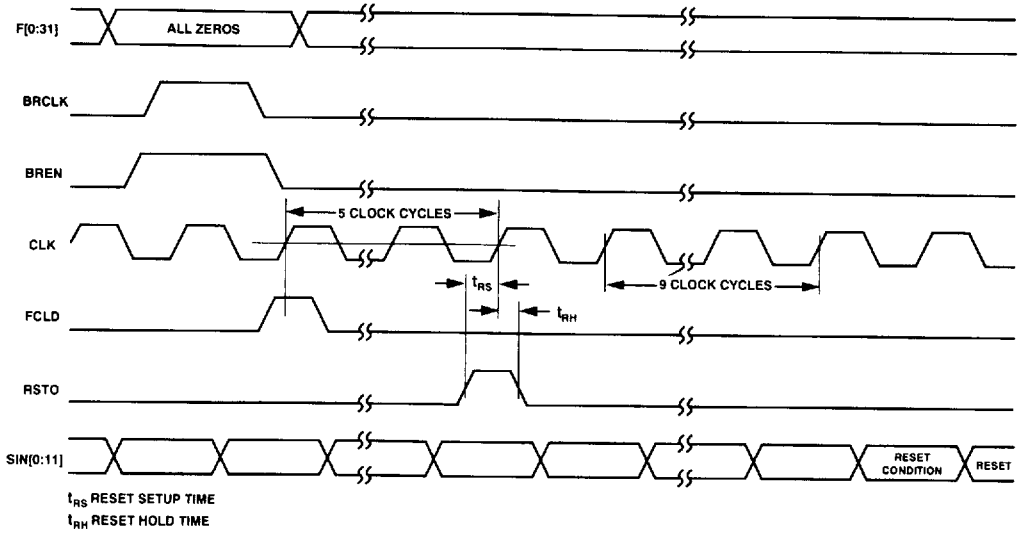


Figure 2. Reset Timing

AD9955 DIRECT DIGITAL SYNTHESIZER

The AD9955 is a digital device which integrates a 32-bit phase accumulator and 15-bit phase to 12-bit sine amplitude converter (see block diagram). The circuit is fabricated in a CMOS process technology, and designed to minimize the number of external devices necessary to implement a high speed DDS system.

Phase Accumulator Architecture

The phase accumulator is comprised of 8 pipelined, 4-bit adder cells to achieve the typical 100 MHz operation. The pipelined accumulator requires the use of input data alignment registers between the frequency control register and the accumulator to maintain the phase-coherent switching characteristics of the DDS. The alignment registers on the 16 least significant bits of the accumulator were eliminated to save power and reduce the number of pipeline delays; this results in a maximum phase discontinuity of 0.005°.

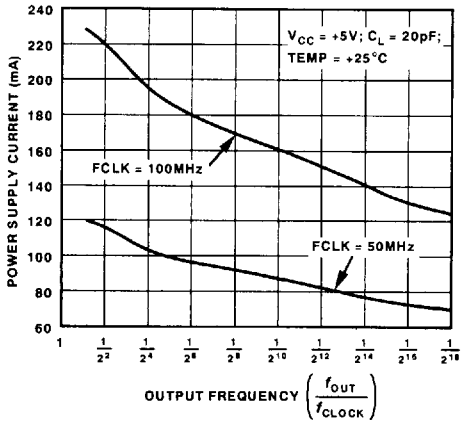


Figure 3. Power Supply Current vs. Output Frequency

The accumulator incorporates carry input and output pins (CIN and COUT) to enable stacking of devices to achieve greater than 32-bit resolution. In normal operation, CIN will be connected to ground, and COUT allowed to float.

An additional feature of the AD9955 accumulator is controlled by the TGLE pin. With this pin tied HIGH, the CIN pin is disabled and the carry input is internally toggled on successive clock cycles. The toggling of the carry input has two major benefits. The theoretical worst case spur is reduced by 3.92 dB, making the worst case spurious free dynamic range of the SIN[0:11] outputs 90.3 dBc. In addition, the DDS spur performance is made more consistent versus frequency due to the randomizing of the errors introduced by possible DAC nonlinearities.

Resetting the AD9955

The synchronous reset function (RST0) resets the output of the phase accumulator to zero radians, allowing the user to initialize the AD9955 from a known state. A reminder: the RSTO signal does not affect the contents of the alignment registers on either side of the adders. To properly reset the AD9955 to zero radians (SIN[0:11] = 1000 0000 0000), perform the following steps in the order listed:

1. Frequency input should be preloaded to zero (F[0:31] = 0; see loading the AD9955).
2. Four clock cycles must pass to clear the prealignment registers.
3. The RSTO signal should go HIGH for at least 12 ns, and meet required setup (t_{RS}) and hold (t_{RH}) times.
4. Nine additional clock cycles must pass to clear the post-alignment registers and allow the new tuning word (0 radians) to propagate through the phase to sine amplitude conversion circuitry.

Critical timing and pipeline delays required for resetting the AD9955 are illustrated in the reset timing diagram. After the RSTO signal is returned to LOW, a new frequency can be

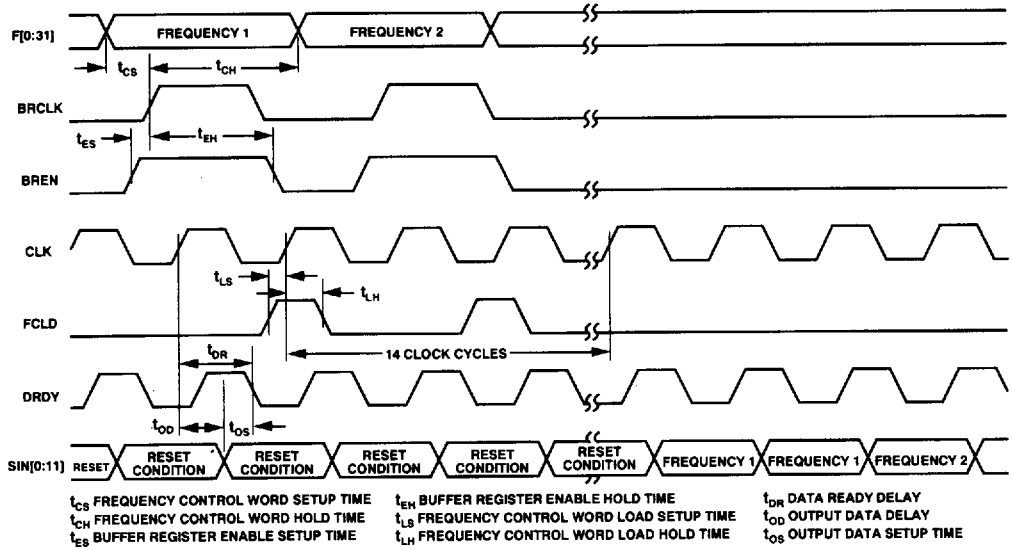


Figure 4. Parallel Mode Timing

loaded into the frequency control register; the SIN[0:11] outputs will remain at the midscale value for 14 clock cycles while the new tuning word propagates through the AD9955.

Loading the Frequency Control Word

For convenience, the frequency control register is double buffered at the inputs to allow asynchronous loading of a new frequency control word. The frequency control word buffer register can be loaded in either parallel (PSEL = HIGH) or serial (PSEL = LOW) mode. The data is clocked on the rising edge of the BRCLK signal when the BREN pin is held HIGH. In serial mode, the data is fed through the LSB (F[31]) and requires multiple clock edges to shift in data.

Once new frequency data is loaded into the frequency control word buffer, it is passed into the frequency control register on the next rising edge of the CLK signal following a HIGH signal on the FCLD pin. The new frequency control word is then used as the input to the phase accumulator and it begins to accumulate at the new rate. The Parallel Mode Timing diagram illustrates the critical timing relationships for loading new frequency data into the AD9955 from the reset condition; these relationships remain the same for any arbitrary condition.

Phase to Sine Architecture

The phase to sine amplitude converter calculates the sine amplitude using a proprietary algorithm for the first 90° of the sine cycle, and takes advantage of the symmetry of the waveform to calculate the remaining quadrants. Only the 15 most significant bits of the phase accumulator output are needed to achieve the 12-bit accuracy of the SIN[0:11] outputs.

In normal operation (TGLE = LOW), the frequency tuning word may take on both odd and even values. Odd frequency input words will result in a spurious free dynamic range (SFDR) of 90.3 dBc, while even frequency words may have spurious frequency content as high as 86.4 dBc. The carry toggle feature discussed above guarantees a worst case SFDR of the frequency tuning words of 90.3 dBc.

The architecture and implementation of the phase to sine algorithm uses several compression techniques to reduce the amount of internal memory required, and to guarantee a minimum throughput rate of 85 MHz, a new benchmark for CMOS DDS circuits. Accordingly, the CLK input is TTL logic compatible, and buffered internally to minimize input capacitance. Although most devices will operate with a 50% duty cycle on CLK input, guaranteed operation at 85 MHz will require adjustment of clock duty cycle (see specification table). All other inputs and outputs are CMOS logic compatible.

SIN Outputs

The SIN[0:11] outputs of the phase to sine conversion circuitry are latched at the output to minimize data skew. The TCMS control signal specifies the format of the output data as either binary unsigned magnitude or two's complement format. The output data is valid on the rising edge of the data ready signal (DRDY), and is designed to track the temperature variation of the output data. The DRDY signal is not recommended for clocking the DAC because of phase uncertainty (jitter). The parallel mode timing diagram also illustrates the timing relationships relevant to capturing the output data, and also the pipeline delays associated with loading a new frequency word. The curves below show the typical propagation delays of SIN[0:11] and DRDY vs. temperature.

SERIAL MODE OPERATION

Serial data is shifted into Pin F31 on the rising edge of the BRCLK. The setup and hold times shown in Figure 4 (Parallel Mode Timing) apply to loading serial data as well. Thirty-two cycles of the BRCLK are needed to shift the entire frequency control word into the Frequency Control Word Buffer Register. Bits are clocked in ascending order, F[31], F[30], F[29] . . . with the MSB clocked in last. A HIGH signal on the FCLD pin allows all 32 bits to pass to the Frequency Control Register on the next rising edge of the CLK.

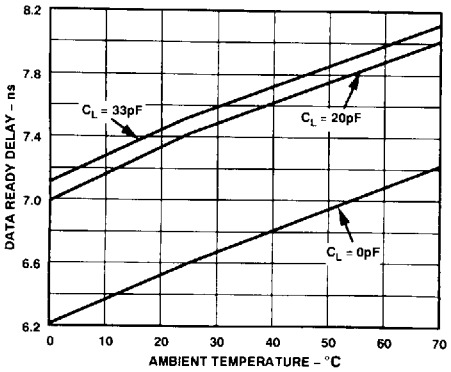


Figure 5. Data Ready Delay vs. Ambient Temperature

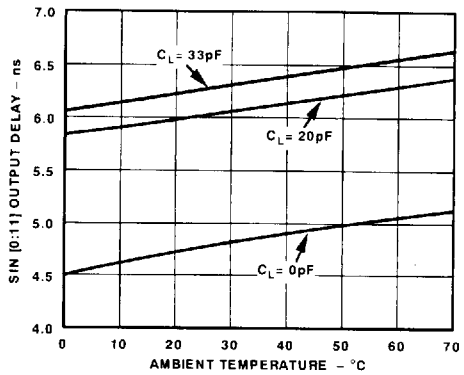


Figure 6. Output Delay vs. Ambient Temperature

Applications Information

The AD9955 can be used in digital demodulation applications to provide a digital frequency reference, or combined with a DAC to provide an analog frequency reference. In the latter application, a DAC with exceptional ac performance is required. The diagram below gives a recommended hookup for a complete direct digital synthesizer employing the AD9955 and the AD9721, a 10-bit 100 Msps DAC.

As in all high speed applications, proper layout is critical; it is particularly important when both analog and digital signals are involved. Analog signal paths should be kept as short as possible, and properly terminated to avoid reflections.

Digital signal paths should also be kept short, and run lengths matched to avoid propagation delay mismatch. In the diagram, series resistors (130 ohms) are inserted in the connections between the SIN[0:9] outputs of the AD9955 and the data inputs of the AD9721 (D_1–D_{10}) to reduce data feedthrough effects and to insure that the setup and hold times of the AD9721's input register are met over the commercial temperature range (0°C to +70°C).

Layout of the ground circuit is a critical factor. A single, low impedance ground plane will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance power planes.

Evaluation Board

An evaluation board is available which combines the AD9955 and either the AD9713B, an 80 Msps 12-bit DAC, or the AD9721, a 10- bit 100 Msps DAC, both of which are supplied with the board. This simplifies the task of evaluating and characterizing the DDS synthesizer. The block diagram shown in Figure 9 illustrates its operation. For more information, please consult the AD9955/PCB data sheet.

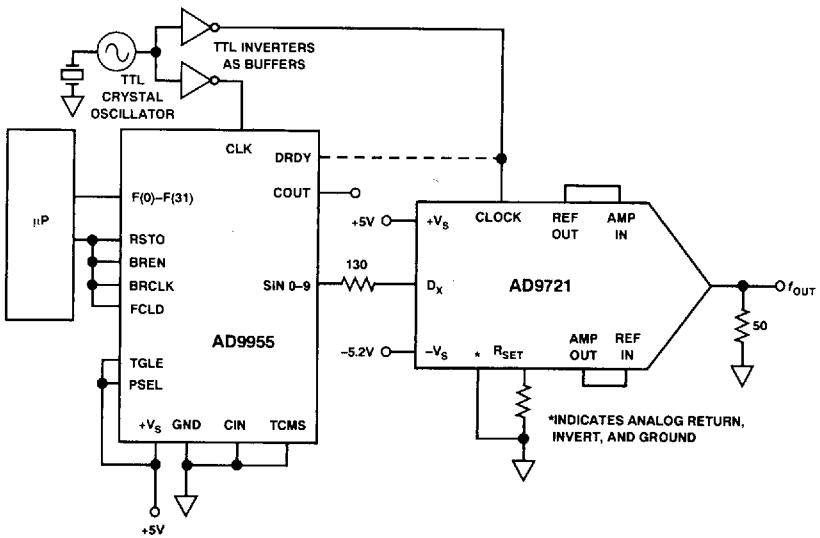


Figure 7. AD9955/AD9721 DDS Synthesizer

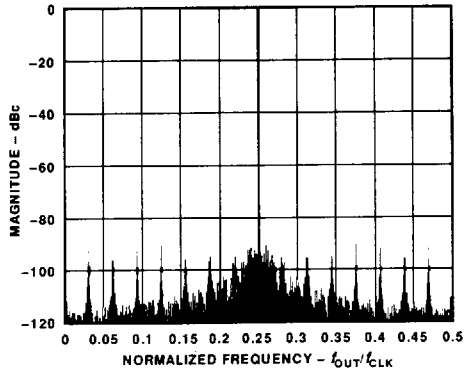


Figure 8. AD9955 Output Spectrum

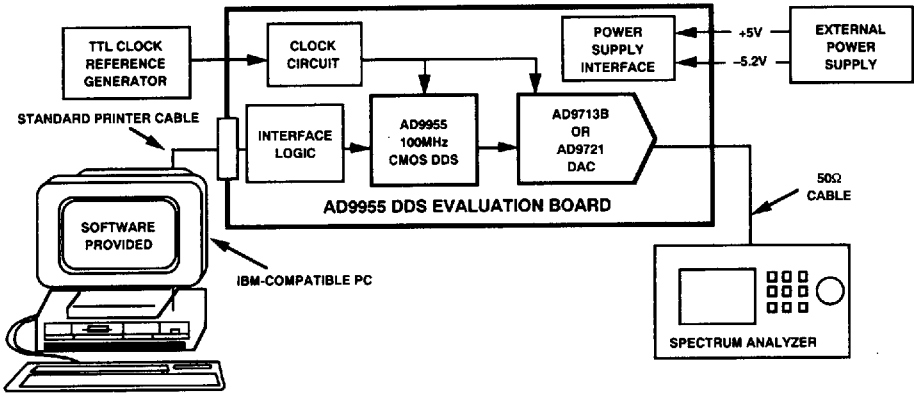


Figure 9. AD9955 DDS Evaluation Board Setup

Table I. Recommended Operation

	Input Voltage		
Parameter	**Min**	**Nominal**	**Max**
$+V_S$	4.75	5.0	5.25
CLK·	0	TTL	$+V_S$
BRCLK, PSEL, BREN, FCLD, CIN, TGLE, TCMS, RSTO, F[0:31]	0	CMOS	$+V_S$

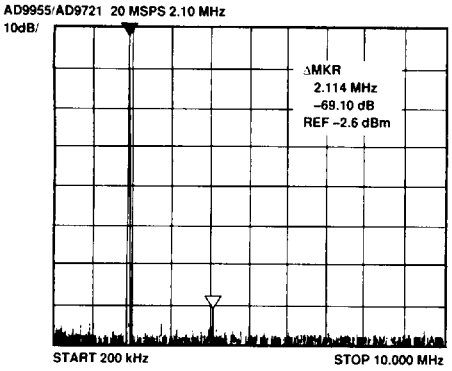


Figure 10. AD9955/AD9721 Output Spectrum

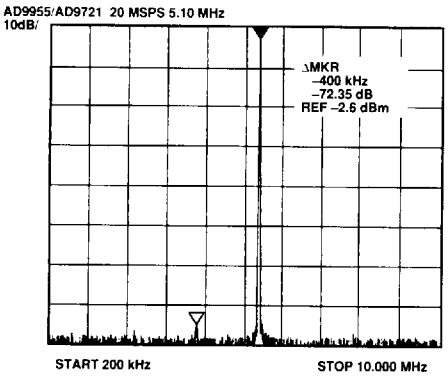


Figure 11. AD9955/AD9721 Output Spectrum

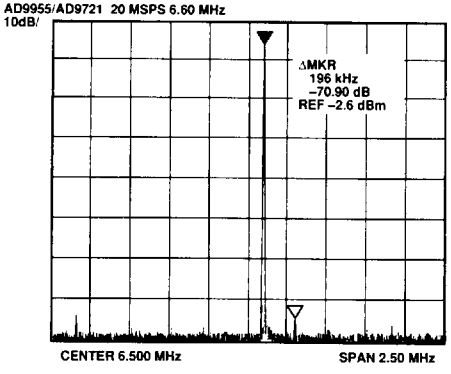


Figure 12. AD9955/AD9721 Output Spectrum

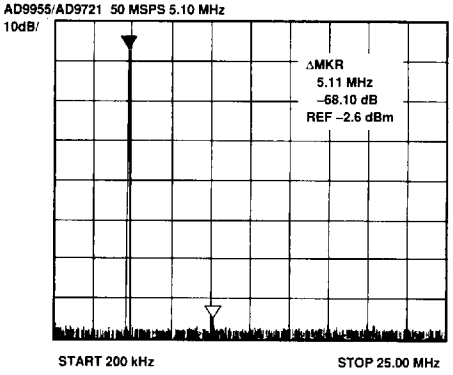


Figure 13. AD9955/AD9721 Output Spectrum

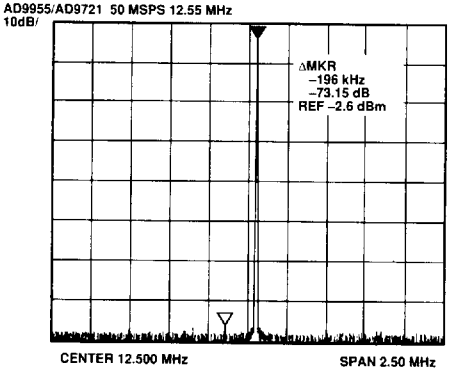


Figure 14. AD9955/AD9721 Output Spectrum

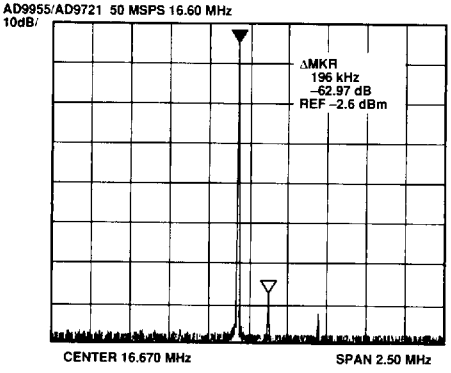


Figure 15. AD9955/AD9721 Output Spectrum

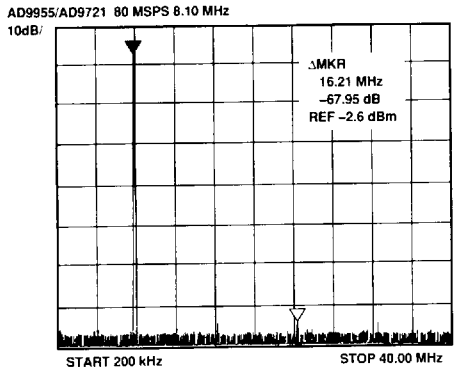


Figure 16. AD9955/AD9721 Output Spectrum

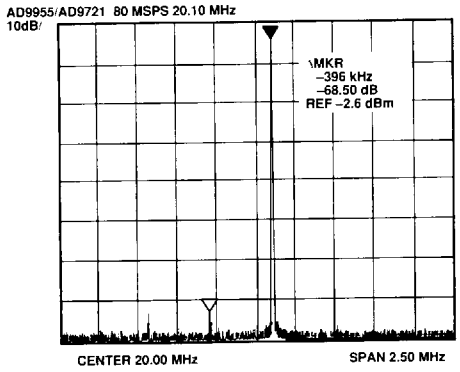


Figure 17. AD9955/AD9721 Output Spectrum

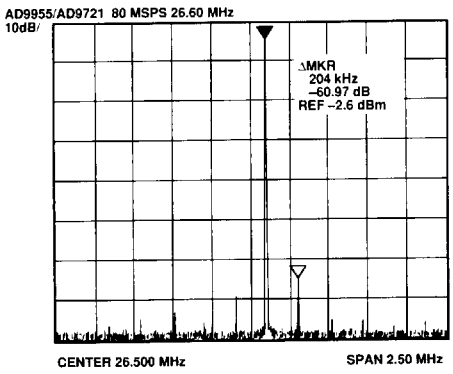


Figure 18. AD9955/AD9721 Output Spectrum

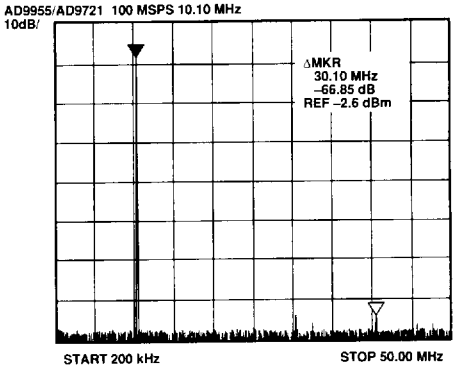


Figure 19. AD9955/AD9721 Output Spectrum

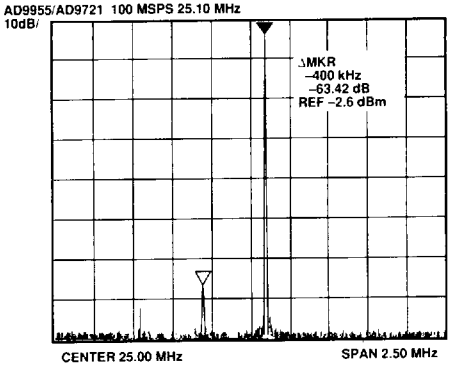


Figure 20. AD9955/AD9721 Output Spectrum

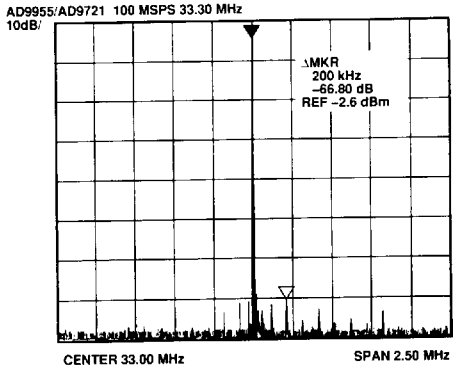


Figure 21. AD9955/AD9721 Output Spectrum