

2x512Kx32bit DRAM Card

MF14M1-J57ATXX

Connector Type

Two-piece 88-pin

DESCRIPTION

These DRAM CARDS have been developed based on JEIDA DRAM CARD GUIDELINE Ver. 2.1. These cards are made using industry standard 512K × 8 Dynamic RAM and interface IC's in TSOP.

FEATURES

- Operating Voltage : $V_{CC}=3.3V \pm 5\%$
- All inputs except \overline{RAS} inputs are buffered.
- Standard card size : 54mm (W) × 85.6mm (L) × 3.3mm (T)
- 88pin 2 piece connector type.
- \overline{RAS} only refresh mode, \overline{CAS} before \overline{RAS} refresh mode and Page mode functions are available.
- Self refresh mode is available. (128ms/1024cycle)

APPLICATIONS

Main/expansion memory unit for Personal Computer, Laser-Printer, FAX etc.

PRODUCT LIST

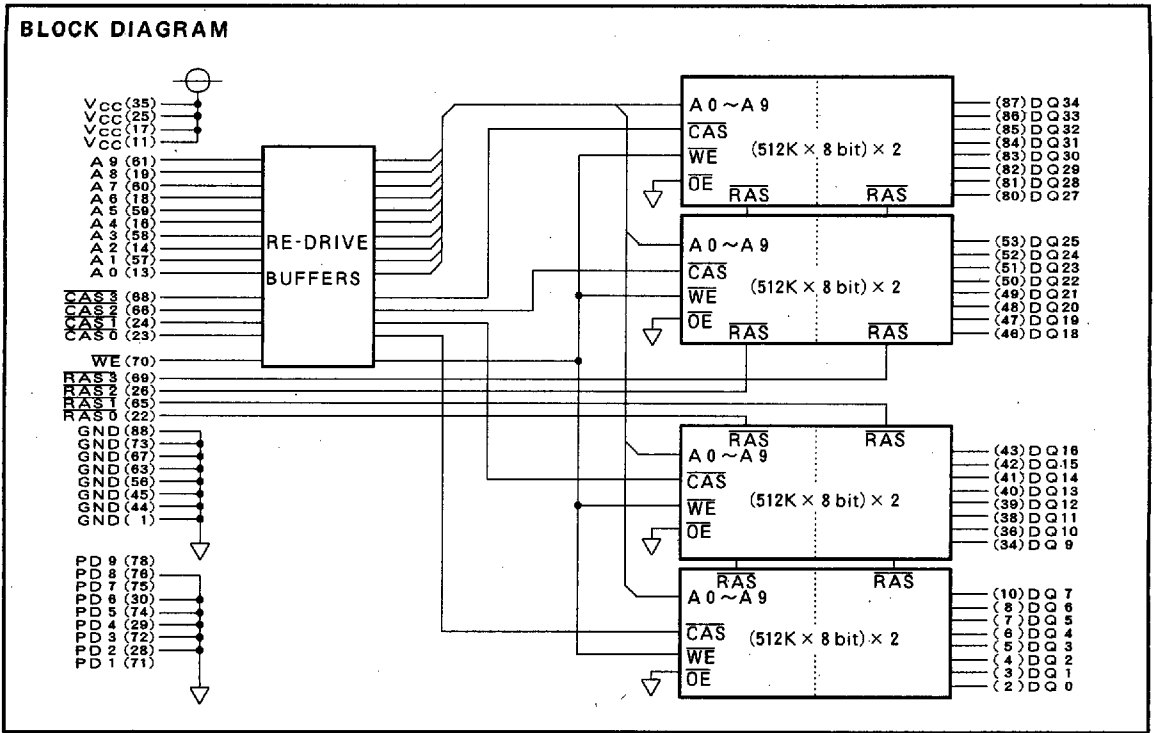
Type name	Item	Memory capacity	Data bus width (bits)	Access time (t _{RAC}) (ns)	Connector type	Number of pins	Outline drawing
MF14M1-J57ATXX		4 MB	32	70	Two-piece	88	88P-002

DYNAMIC RAM CARDS

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	Data I/O	46	DQ18	Data I/O
3	DQ 1		47	DQ19	
4	DQ 2		48	DQ20	
5	DQ 3		49	DQ21	
6	DQ 4		50	DQ22	
7	DQ 5		51	DQ23	
8	DQ 6		52	DQ24	
9	N.C.		No connection	53	
10	DQ 7	Data I/O	54	N.C.	
11	Vcc	Power supply voltage	55	N.C.	Ground
12	N.C.	No connection	56	GND	
13	A 0	Address input	57	A 1	Address input
14	A 2		58	A 3	
15	N.C.	No connection	59	A 5	
16	A 4	Address input	60	A 7	
17	Vcc	Power supply voltage	61	A 9	No connection
18	A 6	Address input	62	N.C.	
19	A 8		Address input	63	GND
20	N.C.	No connection	64	N.C.	No connection
21	N.C.	No connection	65	RAS 1	Row address strobe 1
22	RAS 0	Row address strobe 0	66	CAS 2	Column address strobe 2
23	CAS 0	Column address strobe 0	67	GND	Ground
24	CAS 1	Column address strobe 1	68	CAS 3	Column address strobe 3
25	Vcc	Power supply voltage	69	RAS 3	Row address strobe 3
26	RAS 2	Row address strobe 2	70	WE	Write enable
27	N.C.	No connection	71	PD 1 (N.C.)	Presence detect 1
28	PD 2 (GND)	Presence detect 2	72	PD 3 (GND)	Presence detect 3
29	PD 4 (GND)	Presence detect 4	73	GND	Ground
30	PD 6 (GND)	Presence detect 6	74	PD 5 (GND)	Presence detect 5
31	N.C.	No connection	75	PD 7 (N.C.)	Presence detect 7
32	N.C.		76	PD 8 (GND)	Presence detect 8
33	N.C.	Data I/O	77	N.C.	No connection
34	DQ 9		Data I/O	78	PD 9 (N.C.)
35	Vcc	Power supply voltage	79	N.C.	Data I/O
36	DQ10	Data I/O	80	DQ27	
37	N.C.	No connection	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND	Ground	88	GND	Ground

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FUNCTION TABLE

Operation	input					input/output		Refresh	Note
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Row address	Column address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
RAS-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
CAS before RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
 Odd numbered RAS signals (RAS1, RAS3) and even numbered RAS signals (RAS0, RAS2) should not be active at the same time during Read and Early write cycles.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	-0.5~4.6	V
V _I	Input voltage		-0.5~4.6	V
V _O	Output voltage		-0.5~4.6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	8	W
T _{opr}	Operating temperature		0~55	°C
T _{stg}	Storage temperature		-40~80	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 55°C, unless otherwise noted) : (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage	3.135	3.3	3.465	V
GND	Supply voltage	0	0	0	V
V _{IL}	High input voltage	2.0		V _{CC}	V
V _{IH}	Low input voltage	0		0.8	V

Note 2 : With respect to GND

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ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$, $\text{GND} = 0\text{V}$) : (Note 3)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage	$I_{OH} = -2\text{mA}$	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{mA}$	0		0.4	V
I_{OZ}	Off-state output current	$0\text{V} \leq V_{out} \leq V_{CC}$	-20		20	μA
I_I	Input current	$0\text{V} \leq V_{in} \leq V_{CC}$ other input pins = 0V	-20		20	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} , operating (Note 4, 5, 6)	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{RC} = t_{WC} = \text{min}$, output open			330	mA
$I_{CC2(AV)}$	Supply current from V_{CC} , Standby (Note 7)	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ other input pins $\geq V_{CC} - 0.2\text{V}$ or 0.2V output open			0.7	mA
$I_{CC3(AV)}$	Average supply current from V_{CC} , refreshing (Note 4, 6)	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ $t_{RC} = \text{min}$, output open			590	mA
$I_{CC4(AV)}$	Average supply current from V_{CC} , Page-mode (Note 4, 5, 6)	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling $t_{RC} = \text{min}$, output open			370	mA
$I_{CC6(AV)}$	Average supply current from V_{CC} , $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode (Note 4, 6)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling $t_{RC} = \text{min}$, output open			540	mA
$I_{CC8(AV)}$	Average supply current from V_{CC} , Extended refresh mode (Note 7)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling $\overline{\text{WE}} \geq V_{CC} - 0.2\text{V}$, other input pins = $V_{CC} - 0.2\text{V}$ or 0.2V, output open $t_{RC} = 125\mu\text{s}$, $t_{RAS}(\text{min}) \sim 1\mu\text{s}$			1	mA
$I_{CC9(AV)}$	Average supply current from V_{CC} , Self refresh mode (Note 7)	$\overline{\text{RAS}} = \overline{\text{CAS}} \leq 0.2\text{V}$ output open			1	mA

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate.

Specified values are obtained at the fastest cycle rate.

5 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading.

Specified values are obtained with the outputs open.

6 : Column Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$ and $\overline{\text{CAS}} = V_{IH}$.

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SWITCHING CHARACTERISTICS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$, $GND = 0\text{V}$): (Note 7)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 8, 9)		27	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 8, 10)		70	ns
tAA	Column address access time (Note 8, 11)		42	ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	27	ns

Note 7 : An initial pause of 500 μsec is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged period of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

8 : Measured with a load circuit equivalent to 100pF and $V_{OH} = 2.4\text{V}$ ($I_{OH} = -2\text{mA}$), $V_{OL} = 0.4\text{V}$ ($I_{OL} = 2\text{mA}$).

The reference levels for measuring of output signals are 2.0V (V_{OH}) and 0.8V (V_{OL}).

9 : Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{ASC} \geq t_{ASC}(\text{max})$.

10 : Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.

11 : Assumes that $t_{RAD} \geq t_{RAD}(\text{max})$ and $t_{ASC} \leq t_{ASC}(\text{max})$.

12 : tOFF(max) define the time at which the output achieves the high impedance state ($|I_{OUT}| \leq 20\ \mu\text{A}$) and are not reference to $V_{OH}(\text{min})$ or $V_{OL}(\text{max})$.

TIMING REQUIREMENTS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$, $GND = 0\text{V}$): (Note 13, 14)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tREF	Refresh cycle time		128	ms
tRP	$\overline{\text{RAS}}$ high pulse width	50		ns
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note 15)	20	43	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low (Note 16)	17		ns
tRPC	Precharge to $\overline{\text{CAS}}$ active time.	0		ns
tCPN	$\overline{\text{CAS}}$ high pulse width	10		ns
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note 17)	17	28	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low	10		ns
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note 18)	5	10	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low	10		ns
tCAH	Column address hold time after $\overline{\text{CAS}}$ low	15		ns
tT	Transition time (Note 19)	3	50	ns

Note 13 : The timing requirements are assumed $t_T = 5\text{ns}$.

14 : $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.

15 : $t_{RCD}(\text{max})$ is specified as a reference point only. If $t_{RCD} \leq t_{RCD}(\text{max})$, access time is tRAC. If $t_{RCD} \geq t_{RCD}(\text{max})$, access time is defined as tCAC and tAA.

16 : tCRP requirement is applicable for all $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.

17 : tRAD(max) is specified as a reference point only.

If $t_{RAD} \geq t_{RAD}(\text{max})$ and $t_{ASC} \leq t_{ASC}(\text{max})$, access time is controlled exclusively by tAA.

18 : tASC(max) is specified as a reference point only.

19 : tT is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

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Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{RC}	Read cycle time	130		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width	70	10000	ns
t _{CAS}	$\overline{\text{CAS}}$ low pulse width	20	10000	ns
t _{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	70		ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	27		ns
t _{RCS}	Read setup time before $\overline{\text{CAS}}$ low	5		ns
t _{RCH}	Read hold time after $\overline{\text{CAS}}$ high	0		ns
t _{RRH}	Read hold time after $\overline{\text{RAS}}$ high	10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{WC}	Write cycle time	130		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width	70	10000	ns
t _{CAS}	$\overline{\text{CAS}}$ low pulse width	20	10000	ns
t _{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	70		ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	27		ns
t _{WCS}	Write setup time before $\overline{\text{CAS}}$ low	5		ns
t _{WCH}	Write hold time after $\overline{\text{CAS}}$ low	15		ns
t _{DS}	Data setup time	10		ns
t _{DH}	Data hold time after $\overline{\text{CAS}}$ low	22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{PC}	Read, Write cycle time	55		ns
t _{CP}	$\overline{\text{CAS}}$ high pulse width	10		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width (Note 20)	125	100000	ns

Note 20 : t_{RAS}(min) is specified the following formula as two cycles of $\overline{\text{CAS}}$ input are executed.
 $t_{\text{RAS}}(\text{min}) = t_{\text{CSH}}(\text{min}) + t_{\text{PC}}(\text{min})$.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 21)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{CSR}	$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	20		ns
t _{CHR}	$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	15		ns

Note 21 : Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

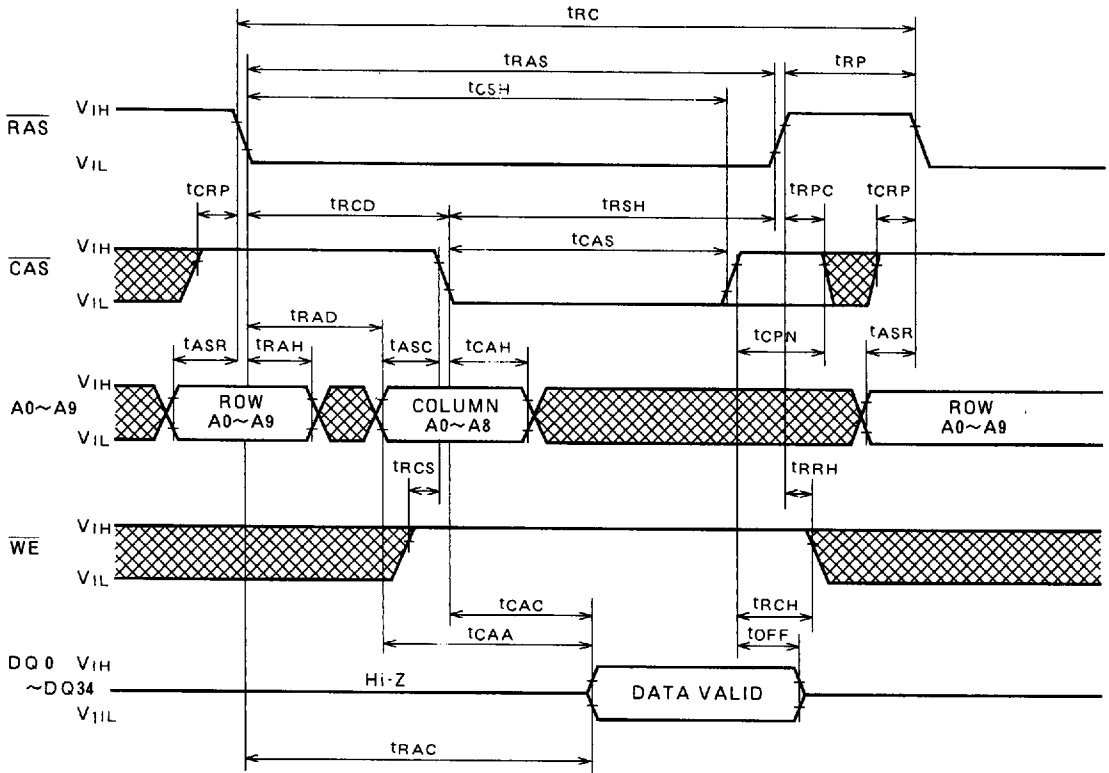
Self Refresh Cycle


Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{RASS}	$\overline{\text{RAS}}$ low pulse width	100		μs
t _{RPS}	$\overline{\text{RAS}}$ high pulse width	130		ns
t _{CHS}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ high	-50		ns



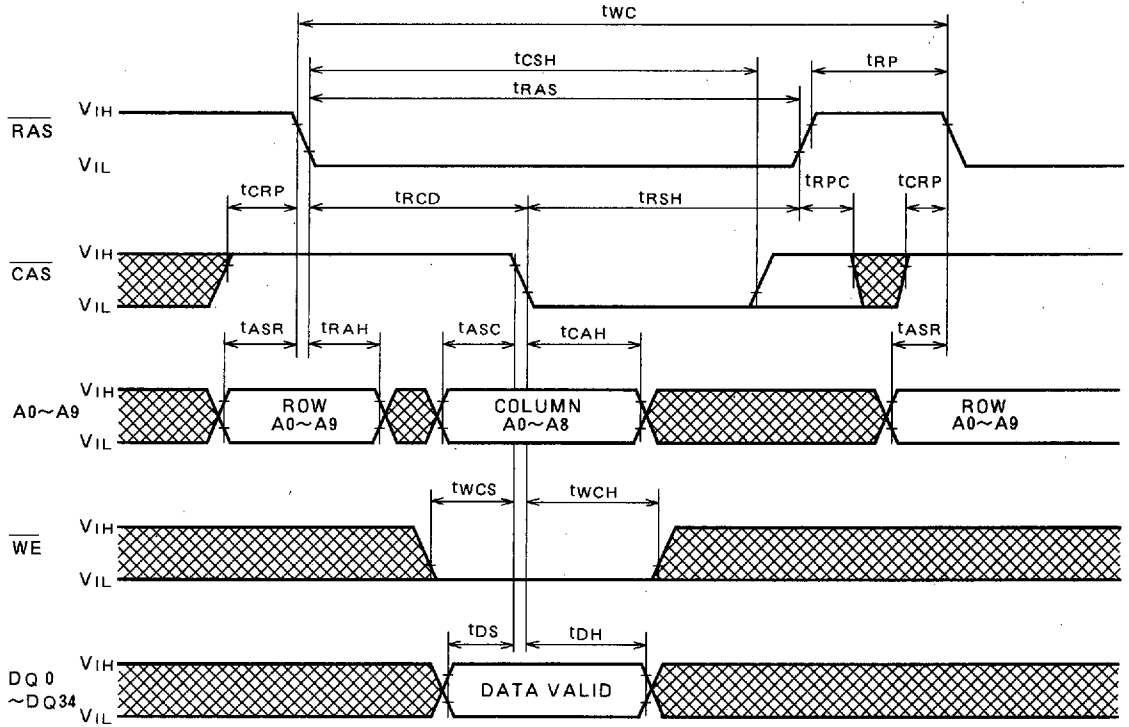
TIMING DIAGRAMS (Note 22)

Read Cycle



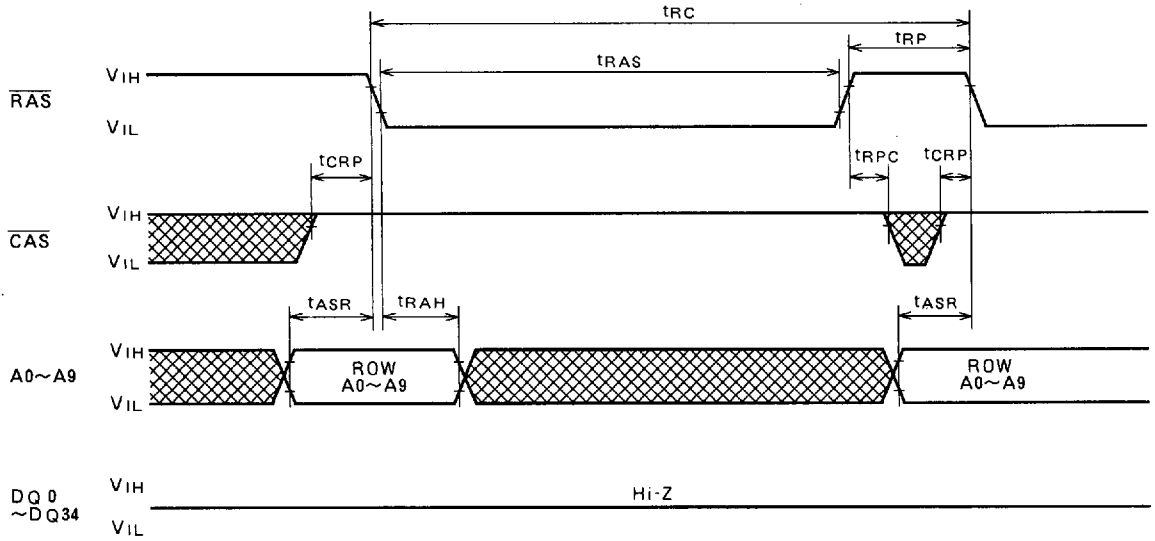
Note 22 :  indicates the don't care input

Early Write Cycle

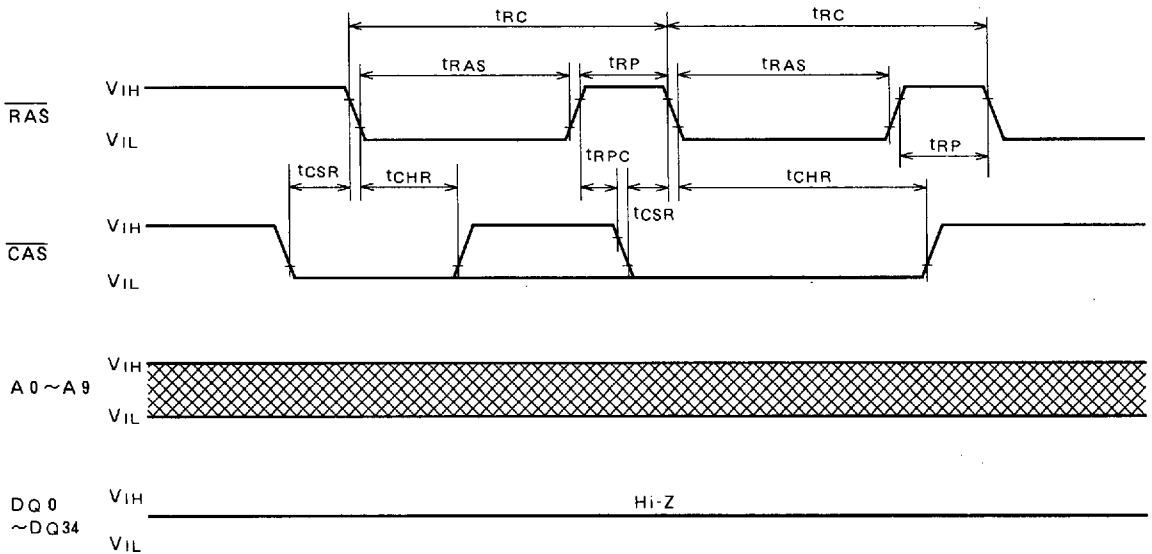


DYNAMIC RAM CARDS

RAS only Refresh Cycle (Note 23)

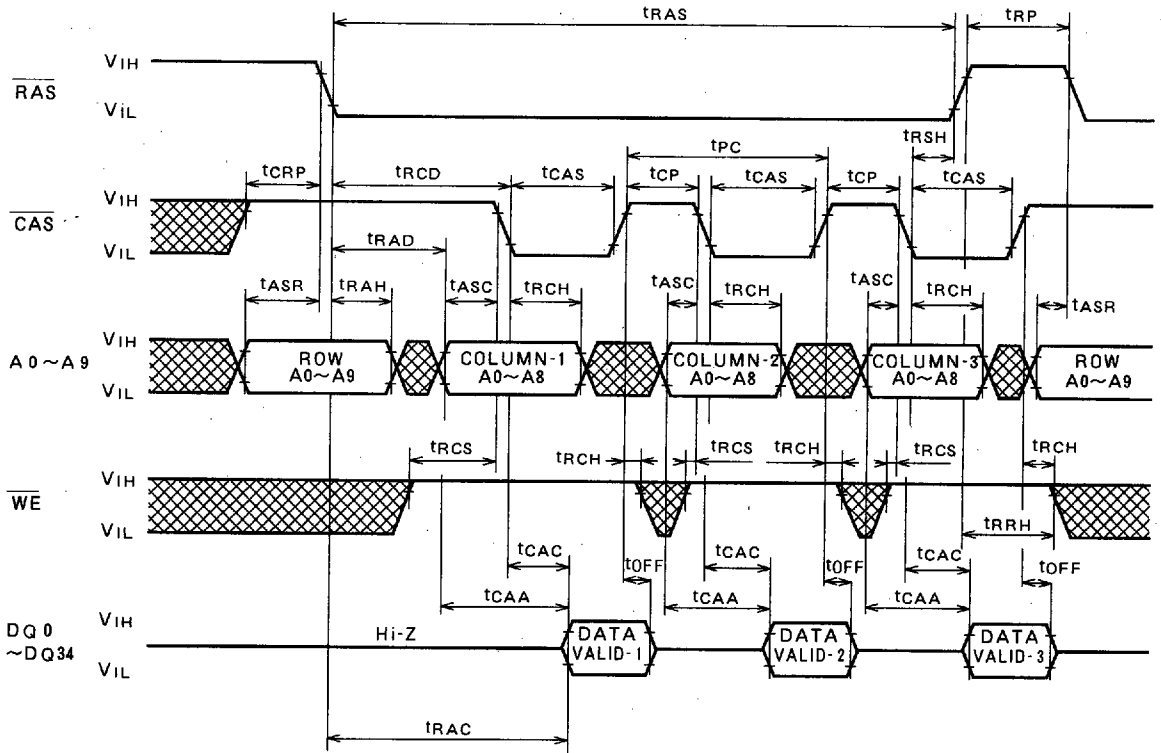


CAS before RAS Refresh Cycle (Note 24)



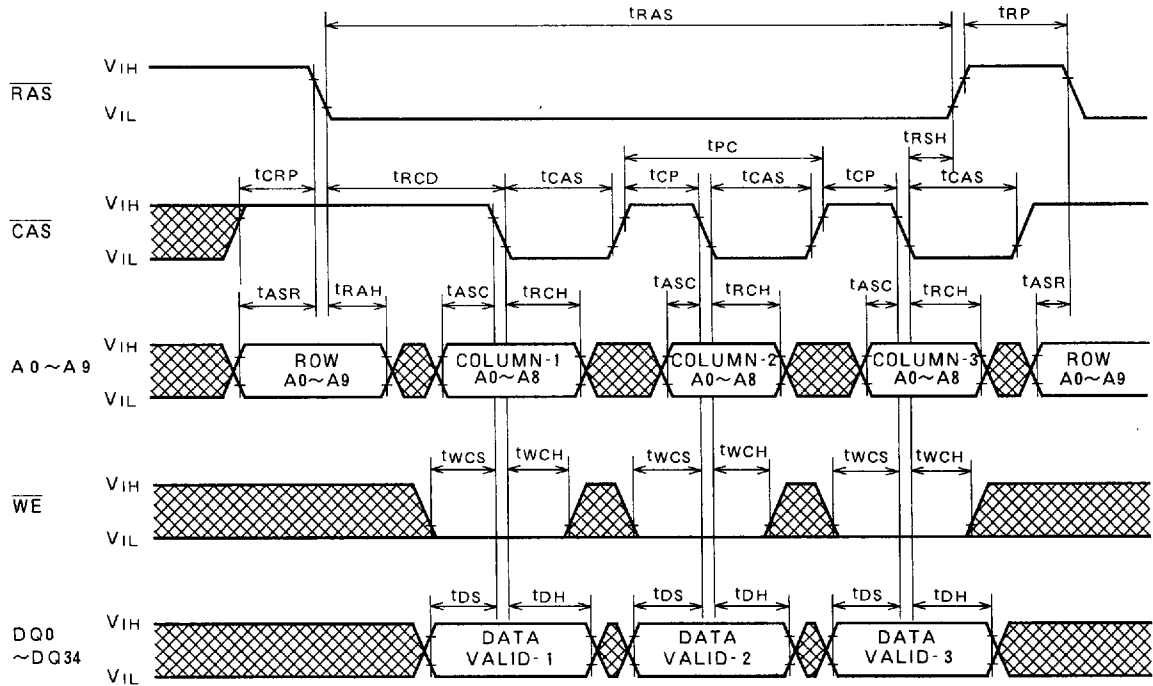
DYNAMIC RAM CARDS

Page-Mode Read Cycle



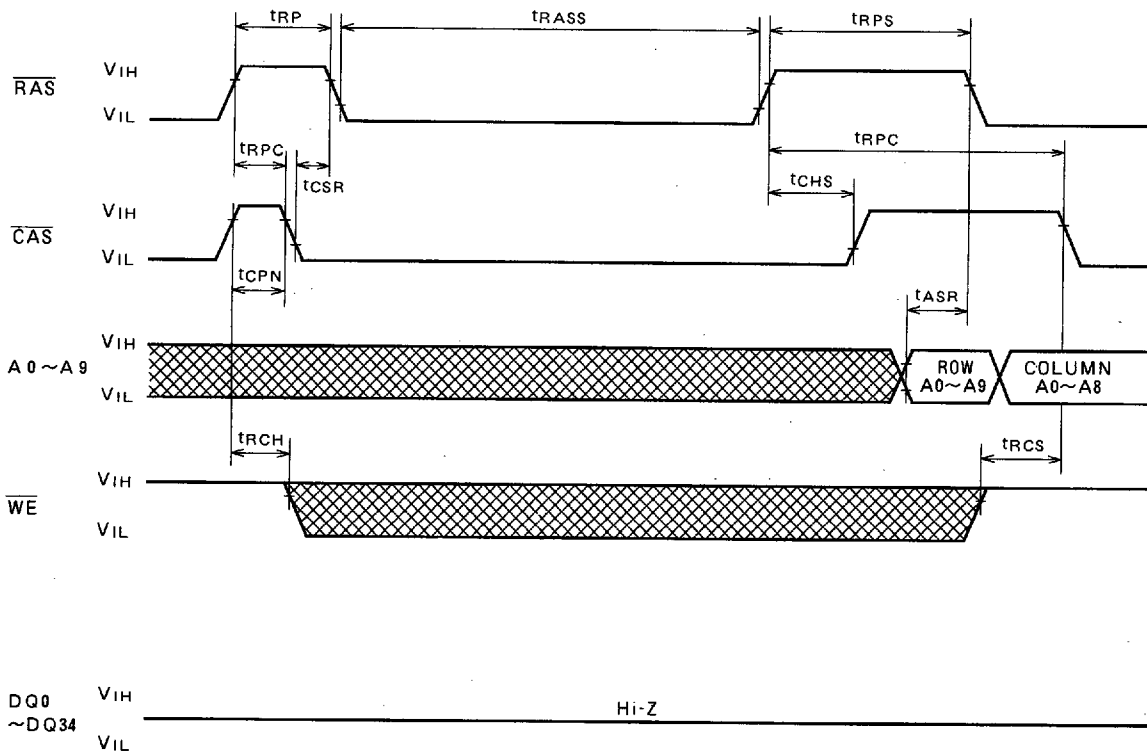
DYNAMIC RAM CARDS

Page-Mode Early Write Cycle



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Self Refresh Cycle (Note 25)



Note 25. Self refresh sequence

Two refreshing methods can be selected depending on the low pulse width (t_{RASS}) of \overline{RAS} signal during the self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing diagram

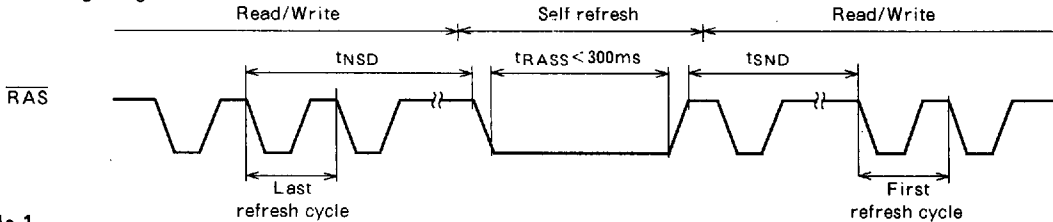
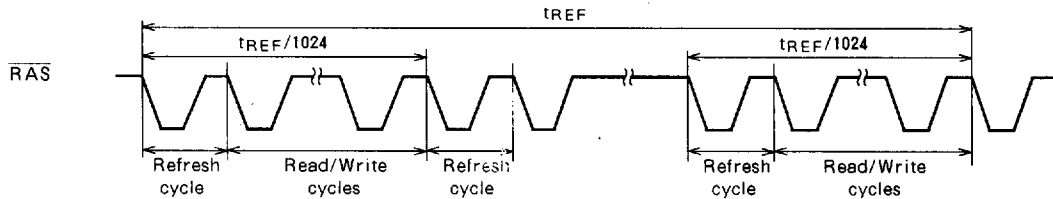


Table 1

Read/Write	Read/Write → Self refresh	Self refresh → Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leq 16.4ms$	
RAS only distributed refresh	$t_{NSD} \leq 16 \mu s$	$t_{SND} \leq 16 \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh

The CBR distributed refresh performs more than 1024 constant period ($125 \mu s$ max) CBR cycles within 128ms.

Definition of RAS only distributed refresh

All combinations of ten row address signals ($A_0 \sim A_9$) are selected during 1024 constant period ($16 \mu s$ max) RAS only refresh cycles within 16.4ms.

Note :

$\overline{RAS}/\overline{CAS}$ refresh may be used instead of RAS only refresh.

1.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
The time interval from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSD} (shown in table 1).

- Switching from self refresh operation to read/write operation.

The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 1).

1.1.2 \overline{RAS} only distributed refresh

- Switching from read/write operation to self refresh operation.
The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last RAS only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within $16 \mu s$.
- Switching from self refresh operation to read/write operation.
The time interval t_{SND} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within $16 \mu s$.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

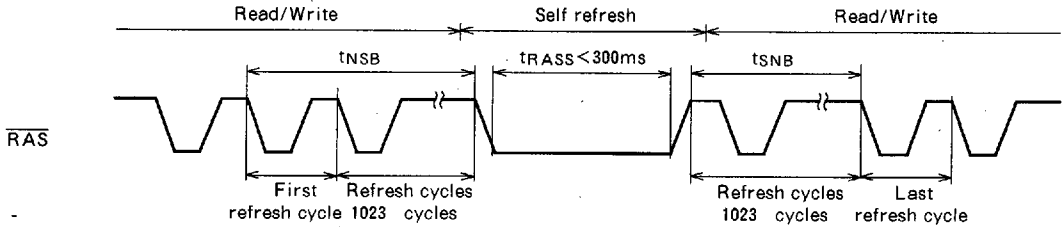
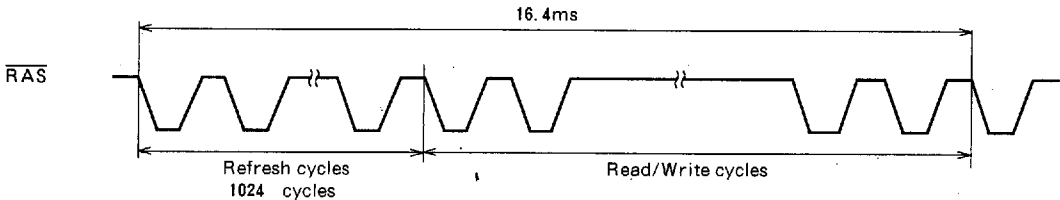


Table 2

Read/Write	Read/Write → Self refresh	Self refresh → Read/Write
CBR burst refresh	$t_{NSB} \leq 16.4ms$	$t_{SNB} \leq 16.4ms$
\overline{RAS} only burst refresh	$t_{NSB} + t_{SNB} \leq 16.4ms$	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4 ms.

Definition of \overline{RAS} only burst refresh

All combinations of ten row address signals ($A_0 \sim A_9$) are selected during 1024 continuous \overline{RAS} only refresh cycles within 16.4ms.

1.2.1 CBR burst refresh

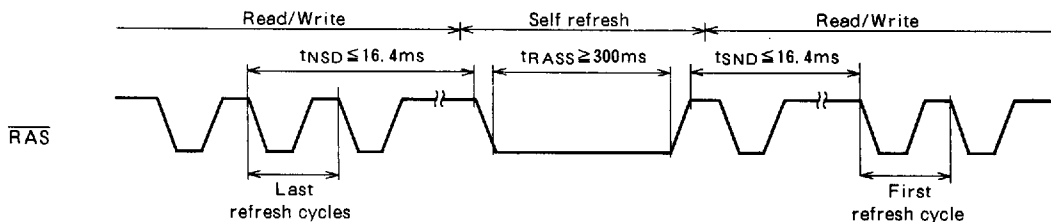
- Switching from read/write operation to self refresh operation.
The time interval t_{NSB} from the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation.
The time interval t_{SNB} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

1.2.2 \overline{RAS} only burst refresh

- Switching from read/write operation to self refresh operation.
The time interval from the falling edge of \overline{RAS} signal in the first \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSB} (shown in table 2).
- Switching from self refresh operation to read/write operation.
The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edges of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 2).

2. In case of $t_{RASS} \geq 300ms$

(A) Timing diagram-A



Timing diagram-B

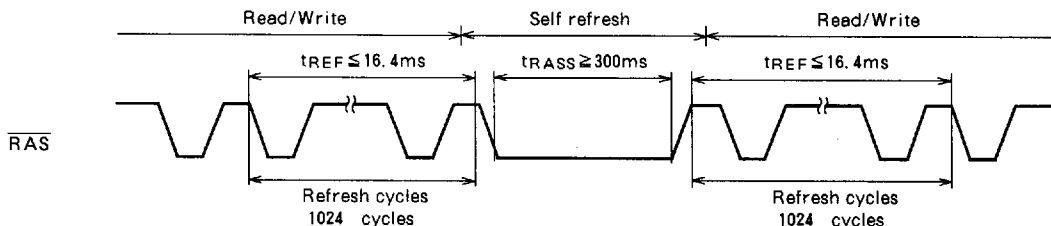


Table 3

Read/Write	Read/Write→Self refresh	Self refresh→Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
RAS only distributed refresh CBR burst refresh RAS only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh

The same as 1.1-(B) and 1.2-(B)

2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16.4ms.

- Switching from self refresh operation to read/write operation.

The time interval t_{SND} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.1.2 \overline{RAS} only distributed, CBR burst, \overline{RAS} only burst refresh.

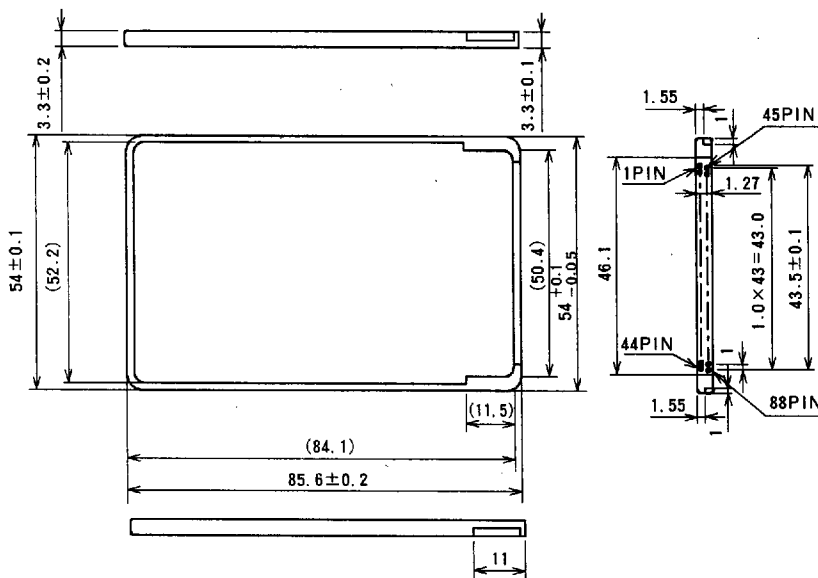
- Before and after the self refresh, 1024 refresh cycles should be executed within 16.4ms for each refresh operation.

MITSUBISHI MEMORY CARD CARD DIMENSIONS

88P-001

TWO - PIECE 88 pin (5V connector keying)

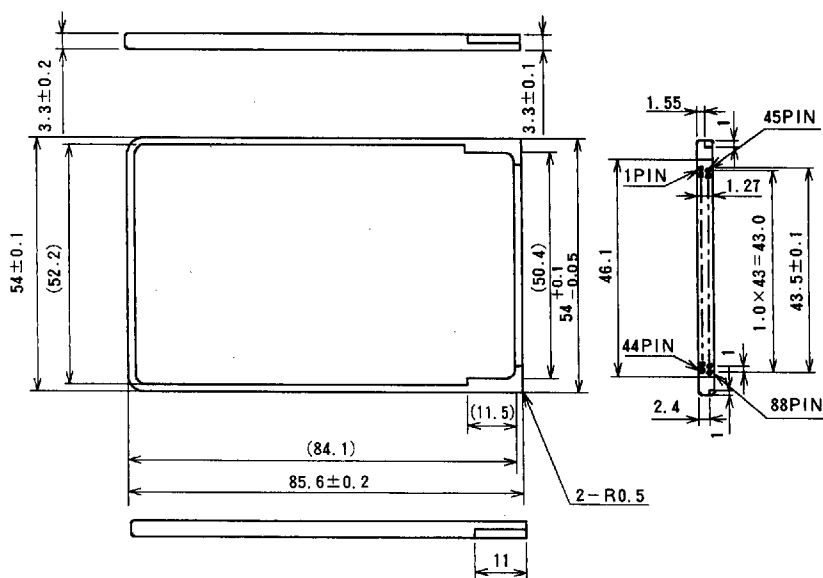
Dimensions in mm



88P-002

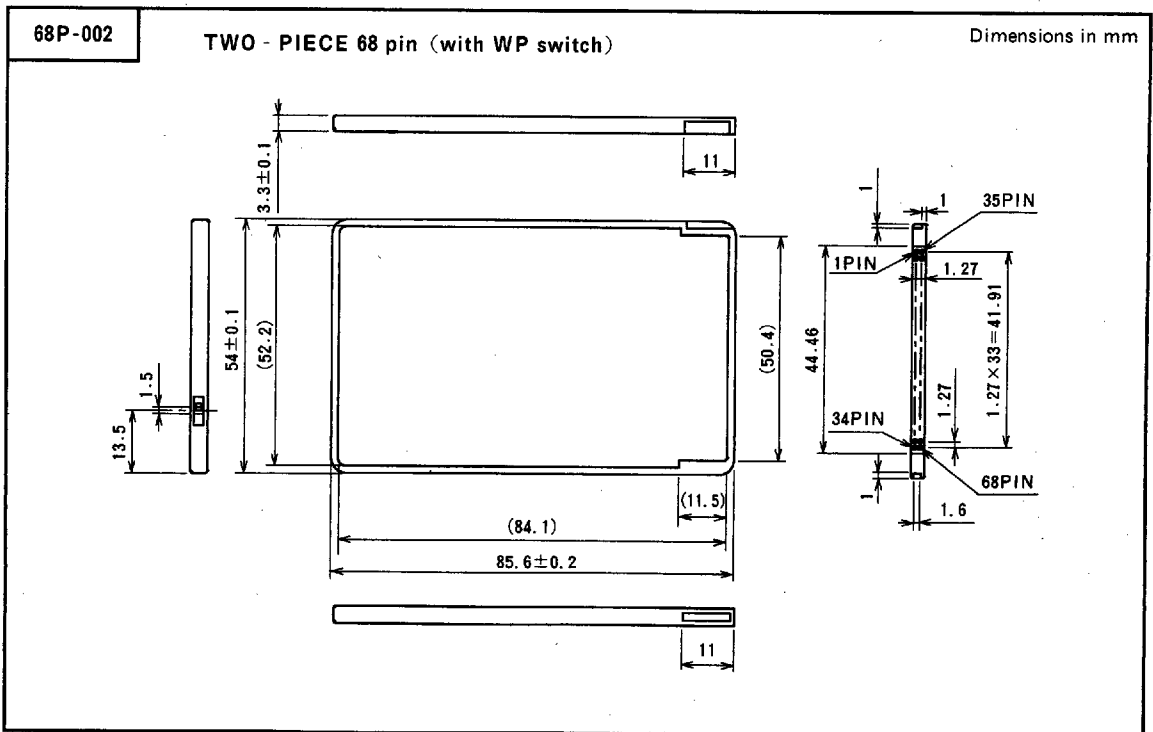
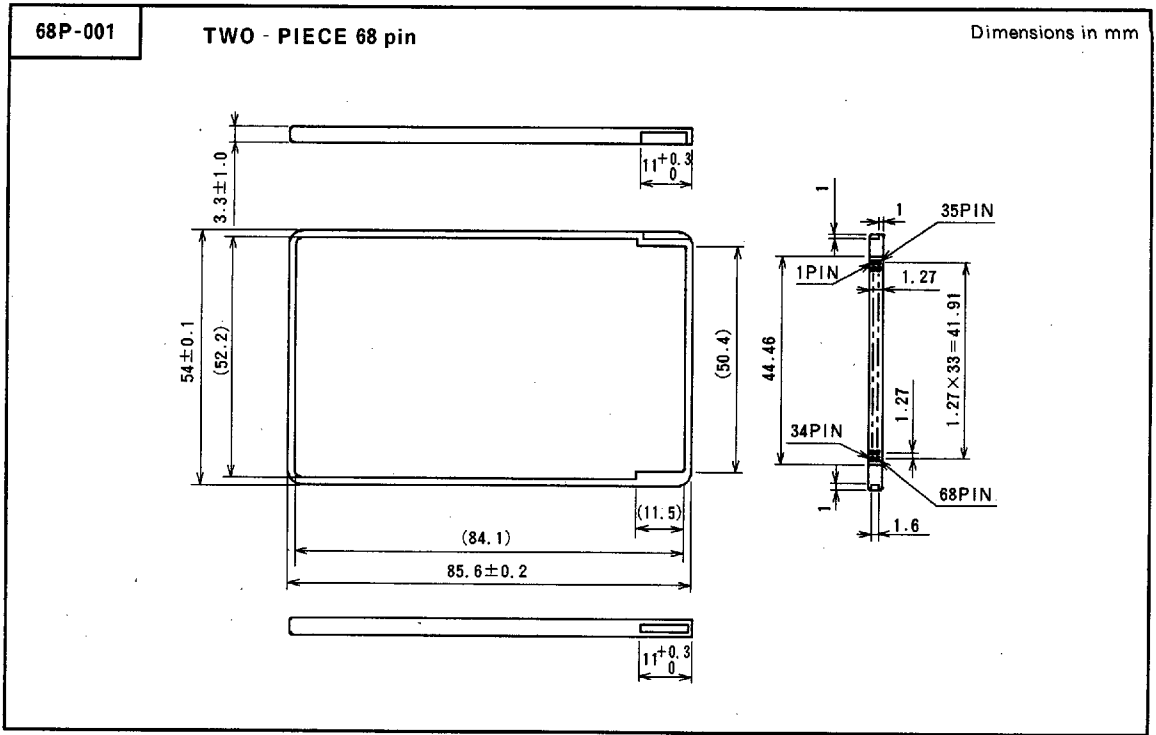
TWO - PIECE 88 pin (3.3V connector keying)

Dimensions in mm



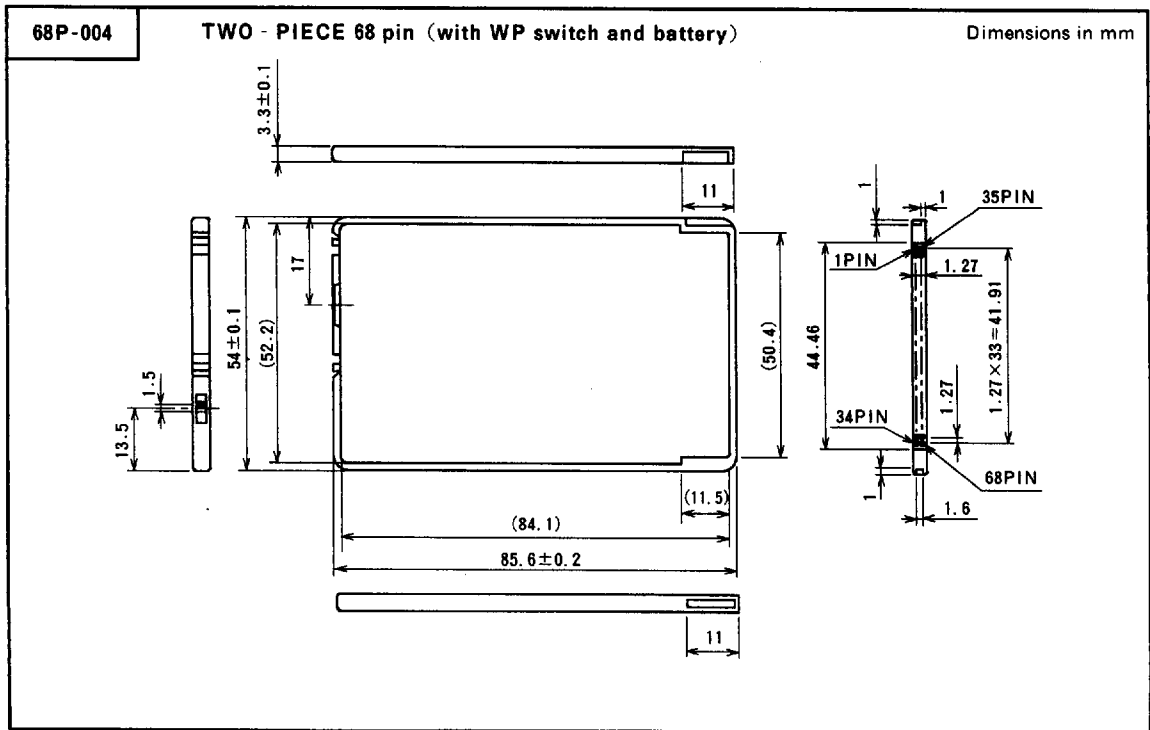
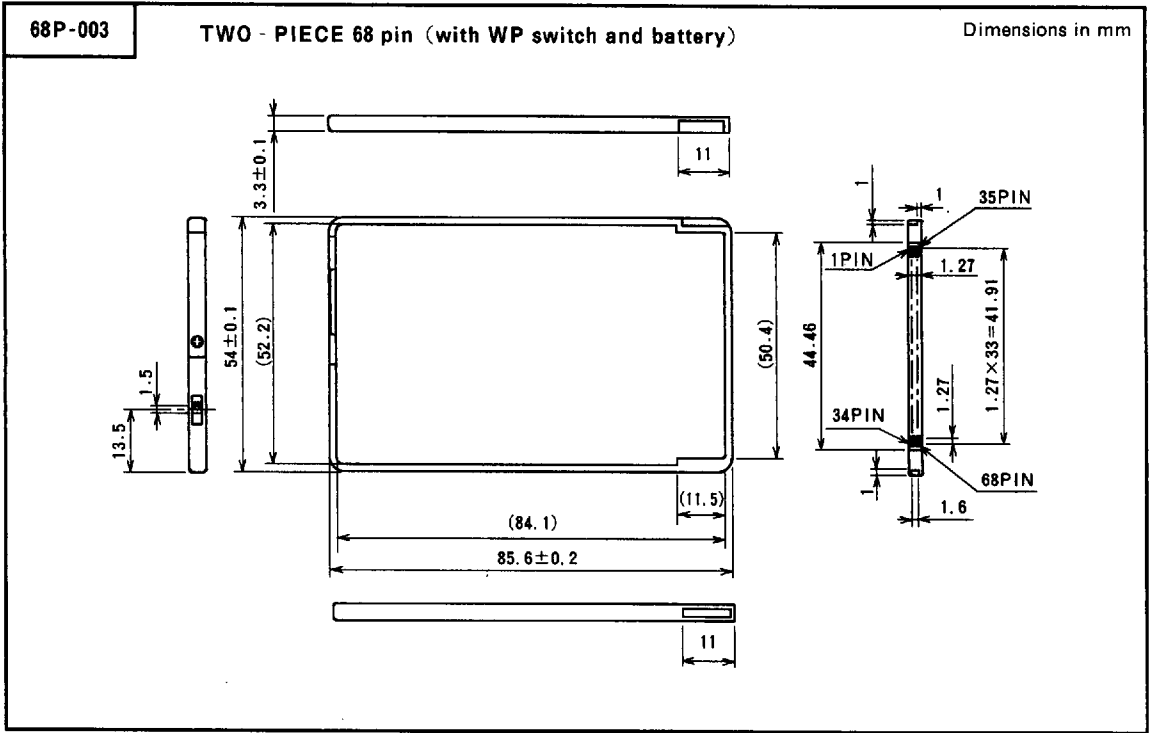
6249825 0029949 809

MITSUBISHI MEMORY CARD CARD DIMENSIONS



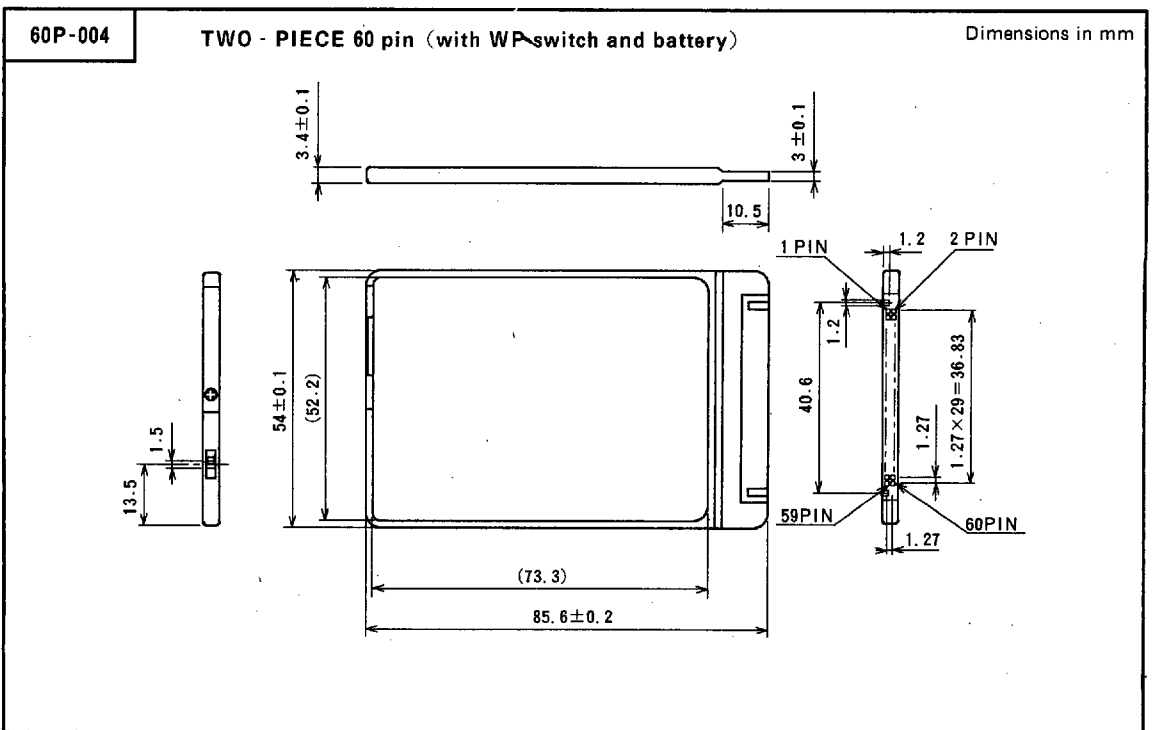
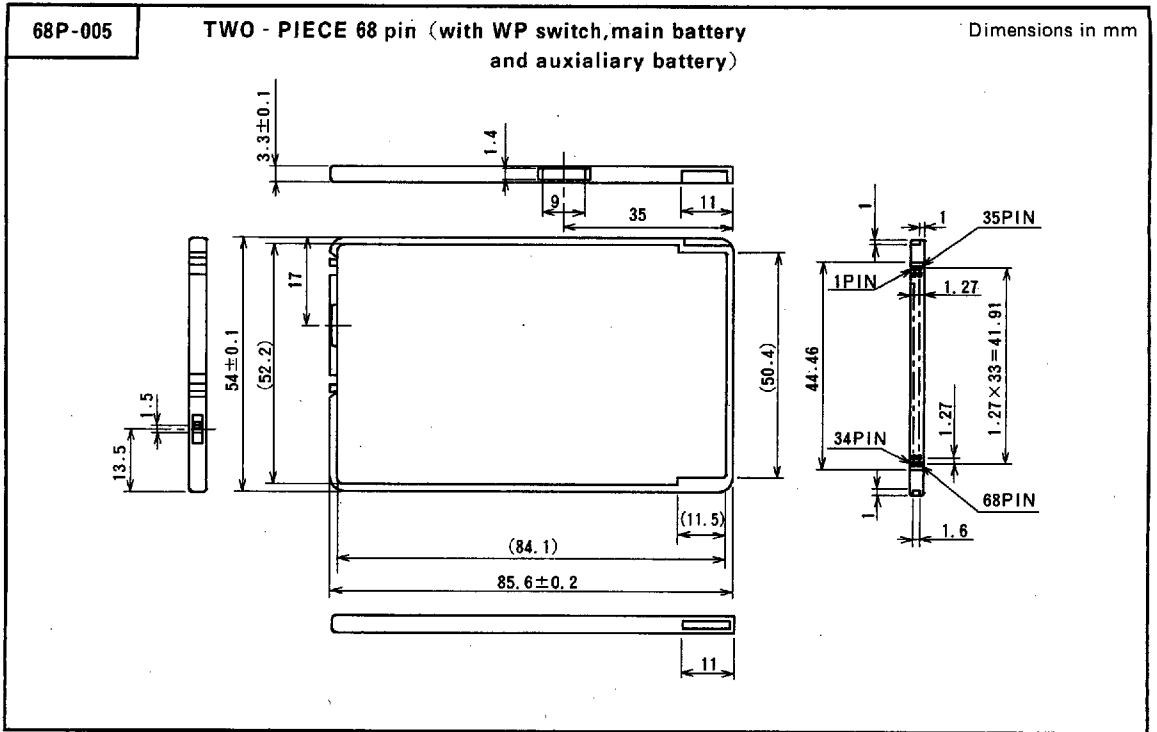
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MITSUBISHI MEMORY CARD CARD DIMENSIONS



6249825 0029951 467

MITSUBISHI MEMORY CARD CARD DIMENSIONS



6249825 0029952 3T3