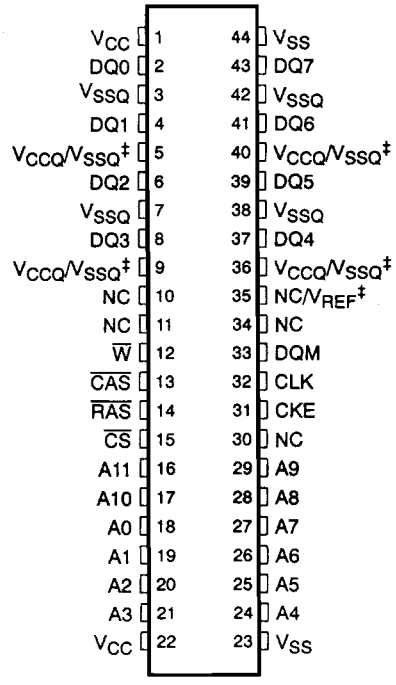
# 16 777 216 BIT SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY

SMOS682–JANUARY 1993

- **Organization . . . 1M × 8 × 2 Banks**
- **3.3 V-Power Supply (10% Tolerance)**
- **Two Banks For On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 100-MHz Data Rates**
- **Burst Length Programmable to 1, 2, 4, or 8**
- **Programmable Output Sequence – Serial or Interleave**
- **Chip Select and Clock Enable For Enhanced System Interfacing**
- **Cycle-By-Cycle DQ Bus Mask Capability**
- **Programmable Read Latency From Column Address**
- **Self-Refresh Capability**
- **High-Speed, Low-Noise LVTTL and GTL Interfaces (SPICE Models Available)**
- **Interface Type (LVTTL or GTL) Automatically Sensed and Provided**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **4K Refresh (Total For Both Banks)**
- **Performance Ranges:**

| | SYNCHRONOUS CLOCK CYCLE TIME $t_{CK}$ (MIN) | ACTV COMMAND TO READ OR WRT COMMAND $t_{RCD}$ (MIN) | REFRESH TIME INTERVAL $t_{REF}$ (MAX) |
|---|---|---|---|
| SDRAM-10 | 10 ns | 30 ns | 64 ms |
| SDRAM-12 | 12.5 ns | 35 ns | 64 ms |
| SDRAM-15 | 15 ns | 40 ns | 64 ms |

DGE PACKAGE†
(TOP VIEW)




† Package is shown for pinout reference only.

‡ Pins 5, 9, 36, and 40 must be connected to $V_{CCQ}$ and pin 35 must remain open (unconnected) for LVTTL Interface Operation. Pins 5, 9, 36, and 40 must be connected to $V_{SSQ}$ and pin 35 must be connected to $V_{REF}$ for GTL Interface Operation.

| PIN NOMENCLATURE | |
|---|---|
| CLK | System Clock |
| $\overline{CS}$ | Chip Select |
| CKE | Clock Enable |
| DQM | Data/Output Enable |
| A11 | Bank Select |
| A0–A10 | Address Inputs<br>A0–A10 Row Addresses<br>A0–A8 Column Addresses<br>A10 Automatic Precharge Select |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{W}$ | Write Enable |
| DQ0–DQ7 | SDRAM Data Inputs/Outputs |
| $V_{CC}$ | Power Supply (3.3 V Typ) |
| $V_{SS}$ | Ground |
| $V_{CCQ}$ | Power Supply for Output Drivers (3.3 V Typ) |
| $V_{SSQ}$ | Ground for Output Drivers |
| $V_{REF}$ | GTL Reference Voltage |
| NC | No External Connect |

## description

The Texas Instruments synchronous DRAM devices are high-speed 16 777 216-bit synchronous dynamic random-access memories, each organized as 2 banks of 1 048 576-words with 8-bits per word. The synchronous DRAM employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches. The synchronous DRAM series is

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compatible with both Low Voltage TTL (LVTTL) and Gunning Tranceiver Logic (GTL) input/output levels, by automatically sensing the interface arrangement and internally enabling the corresponding set of I/O drivers. These synchronous DRAMs are available in a variety of frequency performance ranges.

The synchronous DRAMs are available in a 400-mil, 44-pin surface mount TSOP II package (DGE suffix).

## operation

All inputs of the synchronous DRAM are latched on the rising edge of the system (synchronous) clock. The synchronous DRAM outputs, DQ0–DQ7, are also referenced to the rising edge of CLK. The synchronous DRAM has two banks which are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles will refresh both banks alternately.

Five basic commands or functions control most operations of the synchronous DRAM:

- Bank activate/row address entry
- Column address entry/write operation
- Column address entry/read operation
- Bank deactivate
- $\overline{\text{CAS}}$-before $\overline{\text{RAS}}$ / self-refresh entry

Additionally, operation of the synchronous DRAM may be controlled by three methods: using chip select ($\overline{\text{CS}}$) to select/deselect the device; using DQM to enable/mask the DQ signals on a cycle-by-cycle basis; or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation. Refer to the following truth tables (Tables 1 through 3).

**Table 1. Basic Command Truth Table†**

| COMMAND | STATE OF BANK(S) | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | A11 | A10 | A9–A0 | MNEMONIC |
|---|---|---|---|---|---|---|---|---|---|
| Mode register set | t = deac<br>b = deac | L | L | L | L | X | X | A9=X<br>A8=0<br>A7=0<br>A6=A5=X | MRS |
| Mode register read | t = deac<br>b = deac | L | L | L | L | X | X | A9=X<br>A8=1<br>A7=0<br>A6=A5=X | MRR |
| Bank deactivate (precharge) | X | L | L | H | L | BS | L | X | DEAC |
| Deactivate all banks | X | L | L | H | L | X | H | X | DCAB |
| Bank activate/row address entry | SB = deac | L | L | H | H | BS | V | V | ACTV |
| Column address entry/write operation | SB = actv | L | H | L | L | BS | L | V | WRT |
| Column address entry/write operation with auto-deactivate | SB = actv | L | H | L | L | BS | H | V | WRT-P |
| Column address entry/read operation | SB = actv | L | H | L | H | BS | L | V | READ |
| Column address entry/read operation with auto-deactivate | SB = actv | L | H | L | H | BS | H | V | READ-P |
| Burst stop | – | L | H | H | L | X | X | X | STOP |
| No operation | X | L | H | H | H | X | X | X | NOOP |
| Control input inhibit/No operation | X | H | X | X | X | X | X | X | DESL |

† For execution of these commands on cycle n, CKE (n–1) must be high and CKE (n) and DQM (n) are don't cares.
L = Logic low
H = Logic high
X = Don't care
V = Valid
t = Bank t
b = Bank b
actv = Activated
deac = Deactivated
BS = Logic high to select bank t; logic low to select bank b
SB = Bank selected by A11 at cycle n

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**Table 2. CKE-Use Command Truth Table†**

| COMMAND | STATE OF BANK(S) | CKE (n–1) | CKE (n) | $\overline{CS}$ (n) | $\overline{RAS}$ (n) | $\overline{CAS}$ (n) | $\overline{W}$ (n) | MNEMONIC |
|---|---|---|---|---|---|---|---|---|
| Continue current operation | X | L | L | X | X | X | X | – |
| Self-refresh entry‡ | t = b = deac | H | L | L | L | L | H | SLFR |
| Power-down entry | t =b = no access§ operation | H | L | L | H | H | H | PDE |
| | | H | L | H | X | X | X | PDE |
| Self-refresh/power-down exit | t =b = self-refresh/ power-down | L | H | L | H | H | H | – |
| | | L | H | H | X | X | X | – |
| CLK suspend at n+1 | t or b = access§ operation | H | L | X | X | X | X | HOLD |
| CLK suspend exit at n+1 | t or b = access§ operation | L | H | X | X | X | X | – |
| CBR refresh‡ | t = b = deac | H | H | L | L | L | H | REFR |

† For execution of these commands, A0–A11 (n) and DQM (n) are don't cares.
‡ CBR or self refresh entry requires that all banks be deactivated, or in an idle state prior to the command entry.
n = CLK cycle number
L = Logic low
H = logic high
X = Don't care
V = Valid
t = Bank t
b = Bank b
actv = Activated
deac = Deactivated
burst = Data-in or data out cycle in progress at cycle n+1
§ An access operation refers to any READ (–P) or WRT (–P) command in progress at cycle n. Access operations include the cycle upon which the READ (–P) or WRT (–P) command is entered and all subsequent cycles through the completion of the access burst.

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**Table 3. DQM-Use Command Truth Table†**

| COMMAND | STATE OF BANK(S) | DQM (n) | D0–D7 (n) | $\overline{Q0}$–$\overline{Q7}$ (n+2) | MNEMONIC |
|---|---|---|---|---|---|
| – | t = deac and b = deac | X | N/A | HI-Z | – |
| – | t = actv and b = actv (no bursts) | X | N/A | HI-Z | – |
| Data-in enable | t = write or b = write | L | V | N/A | ENBL |
| Data-in mask | t = write or b = write | H | M | N/A | MASK |
| Data-out enable | t = read or b = read | L | N/A | V | ENBL |
| Data-out mask | t = read or b = read | H | N/A | HI-Z | MASK |

† For execution of these commands, CKE (n–1) must be high and CKE (n) must be high. $\overline{CS}$ (n), $\overline{RAS}$ (n), $\overline{CAS}$ (n), $\overline{W}$ (n), and A0–A11 (n) are don't cares.
n = CLK cycle number
L = Logic low
H = logic high
X = Don't care
V = Valid
M = Masked input data
N/A = Not applicable
t = Bank t
b = Bank b
actv = Activated with no read or write operation in progress.
deac = Deactivated
write = Activated and accepting data-in on cycle n
read = activated and delivering data-out on cycle n+2

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## burst sequence

All data for the SDRAM is written or read in a *burst* fashion. That is, a single starting address is entered into the device and then the SDRAM internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first may be at preceding as well as succeeding column addresses depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst. Refer to the following tables. The length of the burst sequence can be user-programmed to be either 1, 2, 4, or 8 accesses. After a read burst is completed (as determined by the programmed burst length) the outputs will be placed in a high-impedance state (see note below) until the next read access is initiated. Refer to the examples following the timing requirements and characteristics description (Figures 9 through 15).

NOTE: When using terminated DQ buses for GTL interfacing, turning off the output buffers at the device will result in the DQ lines pulling up to the terminating voltage, $V_{TT}$.

**Table 4. 2-Bit Burst Sequences**

| | INTERNAL COLUMN ADDRESS A0 | | | |
|---|---|---|---|---|
| | DECIMAL | | BINARY | |
| | START | 2ND | START | 2ND |
| Serial | 0 | 1 | 0 | 1 |
| | 1 | 0 | 1 | 0 |
| Interleave | 0 | 1 | 0 | 1 |
| | 1 | 0 | 1 | 0 |

**Table 5. 4-Bit Burst Sequences**

| | INTERNAL COLUMN ADDRESS A1 A0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | DECIMAL | | | | BINARY | | | |
| | START | 2ND | 3RD | 4TH | START | 2ND | 3RD | 4TH |
| Serial | 0 | 1 | 2 | 3 | 00 | 01 | 10 | 11 |
| | 1 | 2 | 3 | 0 | 01 | 10 | 11 | 00 |
| | 2 | 3 | 0 | 1 | 10 | 11 | 00 | 01 |
| | 3 | 0 | 1 | 2 | 11 | 00 | 01 | 10 |
| Interleave | 0 | 1 | 2 | 3 | 00 | 01 | 10 | 11 |
| | 1 | 0 | 3 | 2 | 01 | 00 | 11 | 10 |
| | 2 | 3 | 0 | 1 | 10 | 11 | 00 | 01 |
| | 3 | 2 | 1 | 0 | 11 | 10 | 01 | 00 |

**Table 6. 8-Bit Burst Sequences**

| | INTERNAL COLUMN ADDRESS A2 A1 A0 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DECIMAL | | | | | | | | BINARY | | | | | | | |
| | START | 2ND | 3RD | 4TH | 5TH | 6TH | 7TH | 8TH | START | 2ND | 3RD | 4TH | 5TH | 6TH | 7TH | 8TH |
| Serial | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | 000 |
| | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 010 | 011 | 100 | 101 | 110 | 111 | 000 | 001 |
| | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 011 | 100 | 101 | 110 | 111 | 000 | 001 | 010 |
| | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 100 | 101 | 110 | 111 | 000 | 001 | 010 | 011 |
| | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 101 | 110 | 111 | 000 | 001 | 010 | 011 | 100 |
| | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 110 | 111 | 000 | 001 | 010 | 011 | 100 | 101 |
| | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 111 | 000 | 001 | 010 | 011 | 100 | 101 | 110 |
| Interleave | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 | 001 | 000 | 011 | 010 | 101 | 100 | 111 | 110 |
| | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 | 010 | 011 | 000 | 001 | 110 | 111 | 100 | 101 |
| | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 011 | 010 | 001 | 000 | 111 | 110 | 101 | 100 |
| | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 100 | 101 | 110 | 111 | 000 | 001 | 010 | 011 |
| | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 | 101 | 100 | 111 | 110 | 001 | 000 | 011 | 010 |
| | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 | 110 | 111 | 100 | 101 | 010 | 011 | 000 | 001 |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 111 | 110 | 101 | 100 | 011 | 010 | 001 | 000 |

## latency

The beginning data output cycle of a read burst may be be programmed to occur 1, 2, or 3 CLK cycles after the read command. Refer to the set mode register description. This feature allows the user to adjust the synchronous DRAM to operate in accordance with the system's capability to latch the data output from the synchronous DRAM. The delay between the READ command and the beginning of the output burst is known as *read latency* (also known as $\overline{CAS}$ latency). As described previously, after the initial output cycle has commenced, the data burst will occur at the CLK frequency without any intervening gaps. Use of minimum read latencies are restricted based on the particular maximum frequency rating of the synchronous DRAM.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. Note that the write latency is fixed and not determined by the mode register contents.

## two-bank operation

The synchronous DRAM contains two independent banks, which can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank activate/row address entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank may be deactivated either automatically during a READ or a WRT command (READ-P or WRT-P) or by use of the deactivate banks (DEAC) command. Both banks may be deactivated at once by use of the DCAB command. Refer to Table 1 and the following bank deactivation description.

The availability of two banks allows enhanced performance and a wider variety of possible combinations and methods of data access for the user to choose from, based on the system needs.

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### two-bank row access operation

The two-bank feature allows the user to access information on random rows at a higher rate of operation than is possible with a standard DRAM. This may be accomplished by activating one bank with a row address as described previously. Then, while the data stream is being accessed to/from that bank, the second bank can be activated with another row address. When the data stream to/from the first bank is complete, the data stream to/from the second bank can commence without interruption. After the second bank is activated, the first bank could be deactivated to allow the entry of of new row address for the next round of accesses. In this manner, operation could continue on in an interleaved "ping-pong" fashion. Refer to the examples following the timing requirements and characteristics description. (Refer Figures 9 through 15.)

### two-bank column access operation

The availability of two banks also allows the user to access data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), the user can use A11 to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Refer to the examples following the timing requirements and characteristics description. (Refer Figures 9 through 15.)

### bank deactivation (precharge)

Both banks may be simultaneously deactivated (placed in precharge) by use of the DCAB command. The DCAB command is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ low, and A10 high on the rising edge of CLK. A single bank may be deactivated by use of the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 will select the bank to be precharged. A bank may also be deactivated automatically by use of A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, then the accessed bank (selected by A11) will automatically be deactivated upon completion of the access burst. If A10 is held low during READ or WRT command entry then that bank will remain active following the burst. The READ and WRT commands with automatic deactivation are denoted READ-P and WRT-P. Refer to Table 1.

### chip select

$\overline{CS}$, or chip select, can be used to select or deselect the synchronous DRAM for command entry, such as might be required for multiple memory device decoding. If $\overline{CS}$ is held high on the rising edge of CLK, (DESL command) the device will not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ input until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command may be entered simultaneously on the same rising CLK edge of the select operation. The device may be selected/deselected on a cycle-by-cycle basis. (Refer to Table 1 and Table 2.) Note that use of $\overline{CS}$ will not affect an access burst that is in progress; the DESL command can only restrict $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the SDRAM.

### data/output mask

Masking of individual data cycles within a burst sequence may be accomplished by use of the MASK command (see Table 3). During a write burst, if DQM is held high on the rising edge of CLK, then the incident (referenced to the same rising edge of CLK) data word on DQ0–DQ7 will be ignored. For a read burst, if DQM is held high on the rising edge of CLK, then DQ0–DQ7 referenced to the second next rising edge of CLK will be placed in HI-Z (see note below). Therefore, the application of DQM to data output cycles (READ burst) involves a latency of 2 CLK cycles, while the application of DQM to data-in cycles (WRITE burst) has no latency. Also note that the MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read or a write burst sequence. Refer to Figure 11 and the examples following the timing requirements and characteristics description.

NOTE: When using terminated DQ buses for GTL interfacing, turning off the output buffers at the device will result in the DQ lines pulling up to the terminating voltage, $V_{TT}$.

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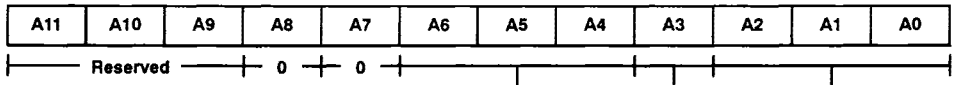
## CLK suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE is made low during the execution of a READ (or READ-P) or WRT (or WRT-P) operation, then the state of the DQ bus occurring at the immediate next rising edge of CLK will be "frozen" at its current state and no further inputs will be accepted until CKE is returned high. This is known as a CLK suspend operation and its execution is denoted as a HOLD command. The device will resume operation from the point at which it was placed in suspension beginning with the second rising edge of CLK after CKE is returned high.

If CKE is brought low when no READ (or READ-P) or WRT (or WRT-P) command is in progress, then the device will enter power-down mode. If both banks are deactivated when power-down mode is entered, then power consumption will be reduced to the minimum. Power-down mode may be used during row active or CBR refresh periods to reduce input buffer power. After power-down mode has been entered, no further inputs will be accepted until CKE is returned high. When exiting power-down mode, new commands may be entered on the first CLK edge after CKE is returned high, provided that $t_{CESP}$ is satisfied. If $t_{CESP} > t_{CK}$, then NOOP or DESL commands must be entered until $t_{CESP}$ is met. Note that CLK must be active and stable (if CLK was turned off for power-down) before CKE is returned high. Refer to Table 2 and Figure 14. Also see the self-refresh description.

## mode register set

The synchronous DRAM contains a mode register, which should be programmed by the user with the read latency length, the burst type, and the burst length. This is accomplished by executing a MRS command with the information being entered on the address lines A0–A8. Bits A9–A11 are reserved for later, or manufacturer's use. A logic 0 should always be entered on A7 and A8, but A9–A11 are don't care entries for the synchronous DRAM. (Refer to Figure 1.)




0 = Serial
1 = Interleave
(Burst Type)

| REGISTER BITS† | | | READ LATENCY‡ |
|---|---|---|---|
| A6 | A5 | A4 | |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |

† All other combinations are reserved.

‡ Refer to timing requirements for minimum valid Read Latencies based on maximum frequency rating.

| REGISTER BITS§ | | | BURST LATENCY‡ |
|---|---|---|---|
| A2 | A1 | A0 | |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |

§ All other combinations are reserved.

**Figure 1. Mode Register Programming**

The MRS command is executed by holding $\overline{RAS}$ low, $\overline{CAS}$ low, $\overline{W}$ low, and the input mode word valid on A0–A8 on the rising edge of CLK (refer to Table 1). The MRS command can be executed only following the deactivation of both banks.

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### mode register read

To read back the contents of the mode register, a MRR command can be entered, which is identical to the MRS command described previously, except that A8 should be held high instead of low. The DQ bus will enter the low impedance state on the first CLK edge after the MRR command is entered (refer to parameter $t_{LZ}$). The lower nibble of the mode register, bits 0, 1, 2, 3, will be available on the DQ1, DQ3, DQ4, and DQ6 outputs, correspondingly, at the fourth CLK edge after the MRR command is entered. The output data will be held for the time specified by $t_{OH}$ after the fourth CLK edge. Bits 4, 5, 6 of the mode register will be available on the DQ1, DQ3, and DQ4 outputs, correspondingly, at the sixth CLK edge after the MRR command is entered. The output data will be held for the time specified by $t_{OH}$ after the sixth CLK edge. A new command can be entered on or after the eighth CLK edge occurring after entry of the MRR command. Refer to Figure 2.

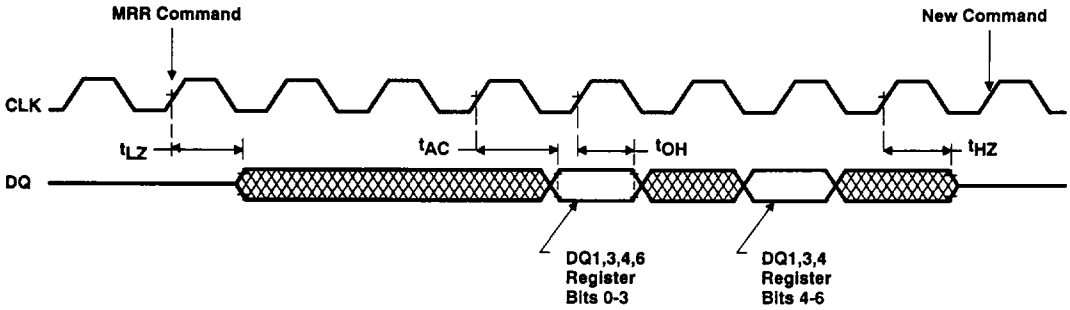



**Figure 2. Mode Register Read**

### refresh

The synchronous DRAM must be refreshed at intervals not exceeding $t_{REF}$ (refer to the parameter timing requirements), or data may not be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, or by performing 4096 $\overline{CAS}$-before-$\overline{RAS}$ (REFR) commands, or by placing the device in self-refresh. Regardless of the method used, refresh must be accomplished before $t_{REF}$ has expired.

#### $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

Before performing a $\overline{CAS}$-before-$\overline{RAS}$ refresh, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ must be low, $\overline{CAS}$ must be low, and $\overline{W}$ must be high upon the rising edge of CLK (refer to Table 2). The refresh address is generated internally such that after 4096 REFR commands, both banks of the SDRAM will have been refreshed. The external address and bank select (A11) are ignored. Note that execution of a REFR command will automatically deactivate both banks upon completion of the internal CBR cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before $t_{REF}$ expires.

#### self-refresh

To enter self-refresh, both banks of the synchronous DRAM must first be deactivated. Following this, a SLFR command should be executed (refer to Table 2). The SLFR command is identical to the REFR command decribed previously, except that CKE is low. Note that for proper entry of the SLFR command, CKE should be brought low only for the same rising edge of CLK that $\overline{RAS}$ and $\overline{CAS}$ are brought low and $\overline{W}$ is brought high. (Otherwise the device would enter power-down mode.) In the self-refresh mode, all refreshing signals are generated internally for both banks, with all external signals (except CKE) being ignored. Data can be retained by the device automatically for an indefinite period as long as power is maintained (consumption is reduced to a minimum). To exit self-refresh mode, CKE should be returned high. Following this, new commands can then

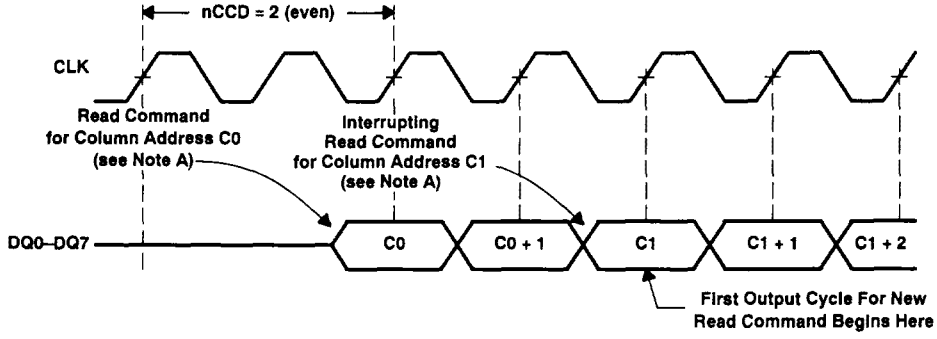
be issued after $t_{RC}$ has expired. Note that if CLK is made inactive during self-refresh, it must be returned to an active and stable condition before CKE is brought high to exit self-refresh. Refer to Figure 15 following the timing requirements and electrical characteristics description.

### Interrupted bursts

A read or write may be interrupted before the burst sequence has been completed with no adverse performance, by entering certain superseding commands and providing that all timing requirements are met (refer to timing requirements and electrical characteristics). Note that the command interrupting either a read or a write burst should be entered only on an even number of cycles from the initial burst command (nCCD). Note also that interruption of READ-P and WRT-P operations is not supported.

**Table 7. Read Burst Interruption**

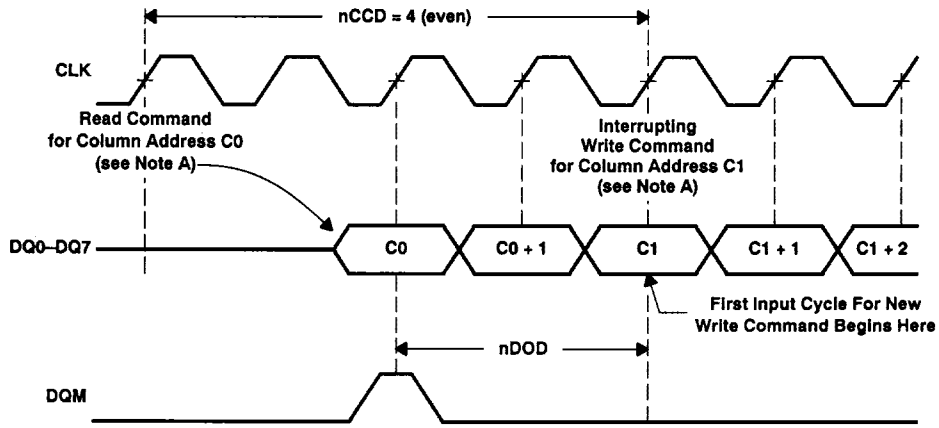
| INTERRUPTING COMMAND | EFFECT OR NOTE ON USE DURING READ BURST |
|---|---|
| DEAC, DCAB | Note that the DQ bus will be placed in high-impedance state when nHZP is satisfied or upon completion of the read burst, whichever occurs first. (Refer to Figure 16.) |
| WRT, WRT-P | The WRT command immediately supersedes the read burst in progress, but note that DQM must be made high nDOD CLK cycles previous to the WRT (or WRT-P) command entry to avoid DQ bus contention. (Refer to Figure 4.) |
| READ, READ-P | Current output cycles will continue until the programmed latency from the superseding READ (or READ-P) command has been met, after which the new output cycles will begin. (Refer to Figure 3.) |
| STOP | The DQ bus will be placed in high-impedance state two clock cycles after the stop command is entered or upon completion of the read burst, whichever occurs first. The bank will remain active. |




NOTE A: For the purposes of this example Read Latency = 2, and Burst Length > 2.

**Figure 3. Read Burst Interrupted By Read Command**

PRODUCT PREVIEW




NOTE A: For the purposes of this example Read Latency = 2, and Burst Length > 2.

**Figure 4. Read Burst Interrupted By Write Command**

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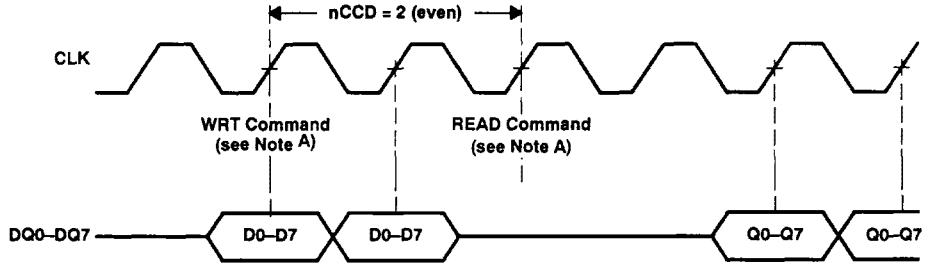
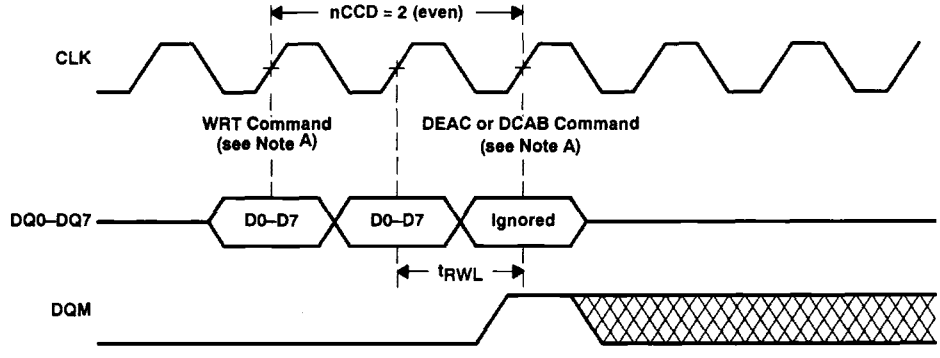
**Table 8. Write Burst Interruption**

| INTERRUPTING COMMAND | EFFECT OR NOTE ON USE DURING WRITE BURST |
|---|---|
| DEAC, DCAB | The DEAC/DCAB command immediately supersedes the write burst in progress. Note that DQM must be used to mask the DQ bus such that the write recovery specification ($t_{RWL}$) is not violated by the interrupt. (Refer to Figure 6.) |
| WRT, WRT-P | The new WRT (or WRT-P) command and data-in immediately supersede the write burst in progress. |
| READ, READ-P | Data-in on previous cycle will be written. No further data-in will be accepted. (Refer to Figure 5.) |
| STOP | The data on the input pins at the time of the burst STOP command will not be written, and no further data will be accepted. The bank will remain active. |




NOTE A: For the purposes of this example, Read Latency = 2, Burst Length > 2, and $t_{CK} = t_{RWL}$.

**Figure 5. Write Burst Interrupted By Read Command**




NOTE A: For the purposes of this example, Read Latency = 2, Burst Length > 2, and $t_{CK} = t_{RWL}$.

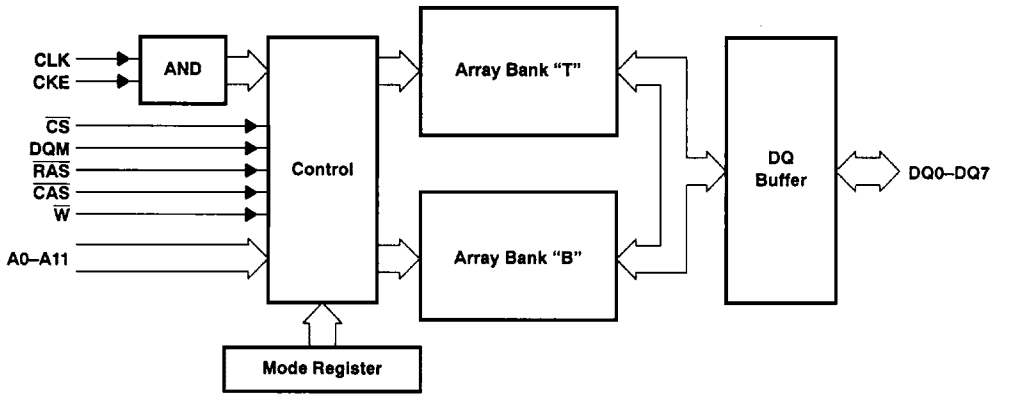
**Figure 6. Write Burst Interrupted By DEAC/DCAB Command**

## power up

After power up to the full $V_{CC}$ level, a 200-μs pause should be allowed (no input except CLK), after which both banks of the device must be deactivated (placed in precharge) and the mode register should be set. Eight REFR commands should then be performed to complete the device initialization. (Refer to Tables 1 and 2, and the set mode register description.)

PRODUCT PREVIEW

## functional block diagram




## absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... – 0.5 to 4.6 V
Voltage range on $V_{CC}$ ..... – 0.5 to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this datasheet are with respect to $V_{SS}$.

## recommended operating conditions

| PARAMETER | | LVTTL INTERFACING | | | GTL INTERFACING | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 3 | 3.3 | 3.6 | 3 | 3.3 | 3.6 | V |
| $V_{SS}$ | Supply voltage | | 0 | | | 0 | | V |
| $V_{TT}$ | GTL terminator voltage | | | | 1.08 | 1.2 | 1.32 | V |
| $V_{REF}$ | GTL reference voltage | | | | 2 $V_{TT}$/3 – 2% | 0.8 | 2$V_{TT}$/3+2% | V |
| $V_{IH}$ | High-level input voltage | 2 | | $V_{CC}$+0.3 | $V_{REF}$+0.05‡ | 1.2 | | V |
| $V_{IL}$ | Low-level input voltage | – 0.3 | | 0.8 | | 0.4 | $V_{REF}$–0.05‡ | V |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

‡ $V_{IH}$ and $V_{IL}$ levels are only for DC testing. For AC timing, $V_{IH}$ of 1.2 V and $V_{IL}$ of 0.4 V should be used.

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## electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted) (see Note 2)

| PARAMETER | | TEST CONDITIONS | | | SDRAM-10 | | | SDRAM-12 | | | SDRAM-15 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −2 mA | | LVTTL | 2.4 | | | 2.4 | | | 2.4 | | | V |
| | | $\|I_{OH}\| \le 10\ \mu A$ | | GTL | $V_{TT}$ − 0.05 | 1.2 | | $V_{TT}$ − 0.05 | 1.2 | | $V_{TT}$ − 0.05 | 1.2 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA | | LVTTL | | | 0.4 | | | 0.4 | | | 0.4 | V |
| | | $I_{OL}$ = 32 mA | | GTL | | | 0.4 | | | 0.4 | | | 0.4 | |
| $I_I$ | Input current (leakage) | 0 V ≤ $V_I$ ≤ $V_{CC}$ + 0.3 V, All other pins = 0 V to $V_{CC}$ | | | | | ±10 | | | ±10 | | | ±10 | μA |
| $I_O$ | Output current (leakage) | 0 V ≤ $V_O$ ≤ $V_{CC}$ + 0.3 V, Output disabled | | | | | ±10 | | | ±10 | | | ±10 | μA |
| $I_{CC1}$ | Average read or write current | $t_{RC}$ = min | | 1 bank active | | | 90 | | | 80 | | | 70 | mA |
| | | | | 2 banks active | | | 160 | | | 150 | | | 125 | mA |
| $I_{CC2}$ | Standby current | Both banks deactivated | CKE = $V_{IH}$ | LVTTL | | | 16 | | | 16 | | | 16 | mA |
| | | | | GTL | | | 20 | | | 20 | | | 20 | |
| | | | CKE = $V_{IL}$ | LVTTL | | | 2 | | | 2 | | | 2 | |
| | | | | GTL | | | 3 | | | 3 | | | 3 | |
| | | | CKE = 0 V (CMOS) | LVTTL | | | 1 | | | 1 | | | 1 | |
| | | One or both banks active | CKE = $V_{IL}$ | LVTTL | | | 4 | | | 4 | | | 4 | |
| | | | | GTL | | | 5 | | | 5 | | | 5 | |
| $I_{CC3}$ | Consecutive CBR commands | $t_{RC}$ = min | | | | | 90 | | | 80 | | | 70 | mA |
| $I_{CC4}$ | Burst current, gapless burst | $t_{CK}$ = min | | | | | 120 | | | 100 | | | 80 | mA |
| $I_{CC6}$ | Self-refresh current | CKE = $V_{IL}$ | | LVTTL | | | 2 | | | 2 | | | 2 | mA |
| | | | | GTL | | | 3 | | | 3 | | | 3 | mA |
| | | CKE = 0 V (CMOS) | | LVTTL | | | 1 | | | 1 | | | 1 | mA |

NOTE 2: All specifications apply to the device after power-up initialization.



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**capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)**

| | | MIN | NOM | MAX | UNT |
|---|---|---|---|---|---|
| $C_{i(S)}$ | Input capacitance, CLK input | | | 7 | pF |
| $C_{i(AC)}$ | Input capacitance, address and control inputs: A0–A11, $\overline{CS}$, DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$ | | | 5 | pF |
| $C_{i(E)}$ | Input capacitance, CKE input | | | 5 | pF |
| $C_o$ | Output capacitance | | | 10 | pF |

NOTE 3: $V_{CC}$ = 3.3 ± 0.3 V and bias on pins under test is 0 V.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER† | | | SDRAM-10 | | SDRAM-12 | | SDRAM-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{CK}$ | CLK (system clock) cycle time | Read Latency = 1 | 30 | | 35 | | 40 | | ns |
| | | Read Latency = 2 | 15 | | 17.5 | | 20 | | |
| | | Read Latency = 3 | 10 | | 12.5 | | 15 | | |
| $t_{CKH}$ | CLK (system clock) high pulse duration | | 3 | | 3.5 | | 4 | | ns |
| $t_{CKL}$ | CLK (system clock) low pulse duration | | 3 | | 3.5 | | 4 | | ns |
| $t_{AC}$ | Data-out access from CLK (see Note 4) | Read Latency = 1 | 28 | | 33 | | 38 | | ns |
| | | Read Latency = 2 | 13 | | 15 | | 18 | | |
| | | Read Latency = 3 | 8 | | 10 | | 12 | | |
| $t_{OH}$ | Data-out hold from CLK | | 2 | | 2 | | 2 | | ns |
| $t_{LZ}$ | CLK to DQ LO-Z (see Note 5) | | 0 | | 0 | | 0 | | ns |
| $t_{HZ}$ | CLK to DQ HI-Z (see Note 6) | | | 7 | | 7 | | 7 | ns |
| $t_{DS}$ | Data-in setup time | | 2 | | 2 | | 2 | | ns |
| $t_{AS}$ | Address setup time | | 2 | | 2 | | 2 | | ns |
| $t_{CS}$ | Control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM) setup time | | 2 | | 2 | | 2 | | ns |
| $t_{CES}$ | CKE setup time (suspend entry/exit, power-down entry) | | 2 | | 2 | | 2 | | ns |
| $t_{CESP}$ | CKE setup time (power-down exit) (see Note 7) | | 8 | | 10 | | 12 | | ns |
| $t_{DH}$ | Data-in hold time | | 2 | | 3 | | 4 | | ns |
| $t_{AH}$ | Address hold time | | 2 | | 3 | | 4 | | ns |
| $t_{CH}$ | Control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM) hold time | | 2 | | 3 | | 4 | | ns |
| $t_{CEH}$ | CKE hold time | | 2 | | 3 | | 4 | | ns |
| $t_{RC}$ | REFR command to ACTV, MRS, or REFR command; Self-refresh exit to ACTV, MRS, or REFR command | | 100 | | 110 | | 130 | | ns |
| $t_{RAS}$ | ACTV command to DEAC or DCAB command | | 60 | 100 000 | 70 | 100 000 | 80 | 100 000 | ns |
| $t_{RCD}$ | ACTV command to READ or WRT command | | 30 | | 35 | | 40 | | ns |
| $t_{RP}$ | DEAC or DCAB command to ACTV, MRS, or REFR command | | 40 | | 40 | | 50 | | ns |
| $t_{APR}$ | Final data-out of READ-P operation to ACTV, MRS, or REFR command | | $t_{RP}$ + (nEP * $t_{CK}$) | | | | | | ns |

† A command, data-in, or data-out is referenced at the rising transition of CLK.
Setup and hold times are referenced to the rising transition of CLK.
The reference level used for timing measurements is 1.4 V for LVTTL, and 0.8 V for GTL.
AC measurements assume $t_T$ = 1 ns.
All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted.
All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted.
All specifications referring to consecutive commands are specified as consecutive commands for the same bank, unless otherwise noted.
Note that a CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during a HOLD operation).

NOTES: 4. $t_{AC}$ is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data-out $t_{AC}$ is referenced from the rising transition of CLK that is Read Latency – 1 cycles after the READ command.
5. $t_{LZ}$ is measured from the rising transition of CLK that is Read Latency – 1 cycles after the READ command.
6. $t_{HZ}$ (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
7. If $t_{CESP} > t_{CK}$, then NOOP or DESL commands must be entered until $t_{CESP}$ is met. Note that CLK must be active and stable (if CLK was turned off for power-down) before CKE is returned high.

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## timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

| PARAMETER† | | | SDRAM-10 | | SDRAM-12 | | SDRAM-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{APW}$ | Final data-in of WRT-P operation to ACTV, MRS, or REFR command | | 60 | | 60 | | 80 | | ns |
| $t_{RWL}$ | Final data-in to DEAC or DCAB command | | 20 | | 20 | | 30 | | ns |
| $t_{RRD}$ | ACTV command for one bank to ACTV command for the other bank | | 20 | | 25 | | 30 | | ns |
| $t_T$ | Transition time, all inputs (see Note 7) | | 1 | 5 | 1 | 5 | 1 | 5 | ns |
| $t_{REF}$ | Refresh interval | | | 64 | | 64 | | 64 | ms |
| nEP | Final data-out to DEAC or DCAB command | Burst Length > 1, Read Latency = 1 | 0 | | 0 | | 0 | | cycles |
| | | Burst Length > 1, Read Latency = 2 | –1 | | –1 | | –1 | | |
| | | Burst Length > 1, Read Latency = 3 | –2 | | –2 | | –2 | | |
| | | Burst Length = 1, Read Latency = 1 | 1 | | 1 | | 1 | | |
| | | Burst Length = 1, Read Latency = 2 | 0 | | 0 | | 0 | | |
| | | Burst Length = 1, Read Latency = 3 | –1 | | –1 | | –1 | | |
| nHZP | DEAC or DCAB interrupt of data-out burst to DQ HI-Z (see Note 8) | Read Latency = 1 | 1 | | 1 | | 1 | | cycles |
| | | Read Latency = 2 | 2 | | 2 | | 2 | | |
| | | Read Latency = 3 | 3 | | 3 | | 3 | | |
| nCCD | READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command (i = 1, 2, 3, . . . ) (see Note 9) | | 2i | | 2i | | 2i | | cycles |
| nCWL | Final data-in to READ command in either bank | | 1 | | 1 | | 1 | | cycles |
| nWCD | WRT command to first data-in | | 0 | 0 | 0 | 0 | 0 | 0 | cycles |
| nDID | ENBL or MASK command to data-in | | 0 | 0 | 0 | 0 | 0 | 0 | cycles |
| nDOD | ENBL or MASK command to data-out | | 2 | 2 | 2 | 2 | 2 | 2 | cycles |
| nCLE | HOLD command to suspended CLK edge; HOLD operation exit to entry of any command | | 1 | 1 | 1 | 1 | 1 | 1 | cycles |
| nRSA | MRS command to ACTV command | | 2 | | 2 | | 2 | | cycles |
| nCDD | DESL command to control input inhibit | | 0 | 0 | 0 | 0 | 0 | 0 | cycles |

† A command, data-in, or data-out is referenced at the rising transition of CLK.
Setup and hold times are referenced to the rising transition of CLK.
The reference level used for timing measurements is 1.4 V for LVTTL, and 0.8 V for GTL.
AC measurements assume $t_T$ = 1 ns.
All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted.
All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted.
All specifications referring to consecutive commands are specified as consecutive commands for the same bank, unless otherwise noted.
Note that a CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

NOTES: 8. Transition time, $t_T$, is measured between $V_{IH}$ and $V_{IL}$.
9. A data-out burst may be interrupted only on an even number of clock cycles after the initial READ command is entered (refer to nCCD). Note that interruption of READ-P and WRT-P operations is not supported.
10. A read or write burst can only be interrupted at even number cycle intervals after entry of the initial READ or WRT command. The nCCD specification applies only for the interruption of read or write bursts.

**Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters**

| | | | SDRAM-10 | | | | | SDRAM-12 | | | | SDRAM-15 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Operating frequency | | 100 | 80 | 66 | 50 | 33 | 80 | 66 | 50 | 33 | 66 | 50 | 33 | MHz |
| $t_{CK}$ | CLK (system clock) cycle time | | 10 | 12.5 | 15 | 20 | 30 | 12.5 | 15 | 20 | 30 | 15 | 20 | 30 | ns |
| | **KEY PARAMETER** | | **NUMBER OF CYCLES REQUIRED** | | | | | | | | | | | | |
| | Read latency, min programmed value | | 3 | 3 | 2 | 2 | 1 | 3 | 3 | 2 | 2 | 3 | 2 | 2 | cycles |
| $t_{RCD}$ | ACTV command to READ or WRT command | | 3 | 3 | 2 | 2 | 1 | 3 | 3 | 2 | 2 | 3 | 2 | 2 | cycles |
| $t_{RAS}$ | ACTV command to DEAC or DCAB command | | 6 | 5 | 4 | 3 | 2 | 6 | 5 | 4 | 3 | 6 | 4 | 3 | cycles |
| $t_{RP}$ | DEAC or DCAB command to ACTV, MODE, or REFR command | | 4 | 4 | 3 | 2 | 2 | 4 | 3 | 2 | 2 | 4 | 3 | 2 | cycles |
| $t_{RC}$ | REFR command to ACTV, mode, or REFR command; self-refresh exit to ACTV, MODE, or REFR command | | 10 | 8 | 7 | 5 | 4 | 9 | 8 | 6 | 4 | 9 | 7 | 5 | cycles |
| $t_{RWL}$ | Final Data-in to DEAC or DCAB command | | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 1 | cycles |
| $t_{RRD}$ | ACTV command for one bank to ACTV command for the other bank | | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 1 | cycles |
| $t_{APR}$ | Final data-out of READ-P operation to ACTV, MRS, or REFR command | Read Latency = 3 | 2 | 2 | 1 | 0 | 0 | 2 | 1 | 0 | 0 | 2 | 1 | 0 | cycles |
| | | Read Latency = 2 | – | – | 2 | 1 | 1 | – | – | 1 | 1 | – | 2 | 1 | cycles |
| | | Read Latency = 1 | – | – | – | – | 2 | – | – | – | – | – | – | – | cycles |
| $t_{APW}$ | Final data-in of WRT-P operation to ACTV, MODE or REFR command | | 6 | 5 | 4 | 3 | 2 | 5 | 4 | 3 | 2 | 6 | 4 | 3 | cycles |

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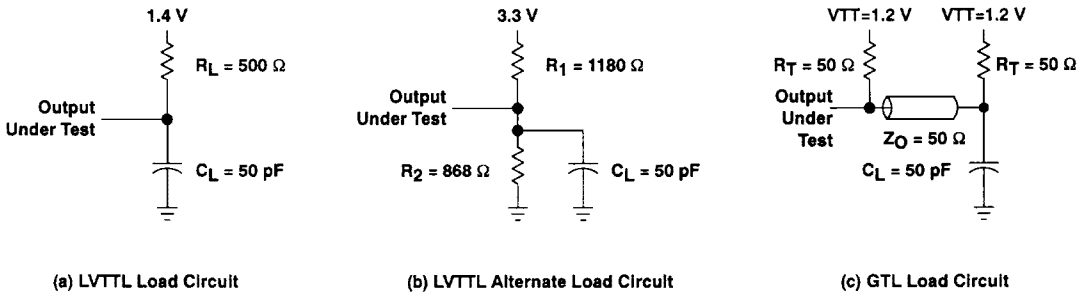
## PARAMETER MEASUREMENT INFORMATION




(a) LVTTL Load Circuit (b) LVTTL Alternate Load Circuit (c) GTL Load Circuit

Figure 7. Synchronous DRAM Load Circuits

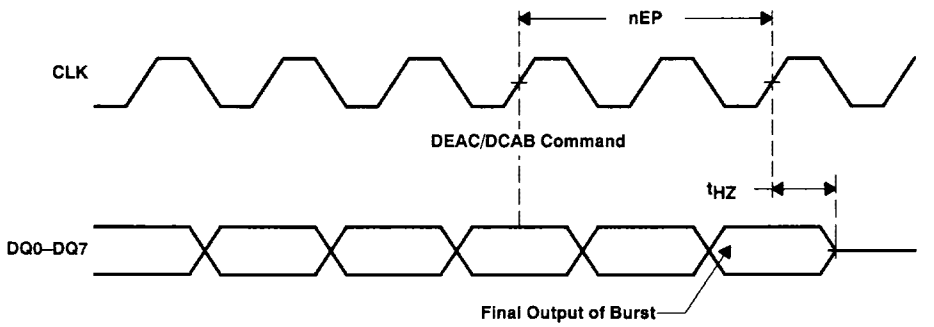



Figure 8. nEP (Assume Read Latency = 3)

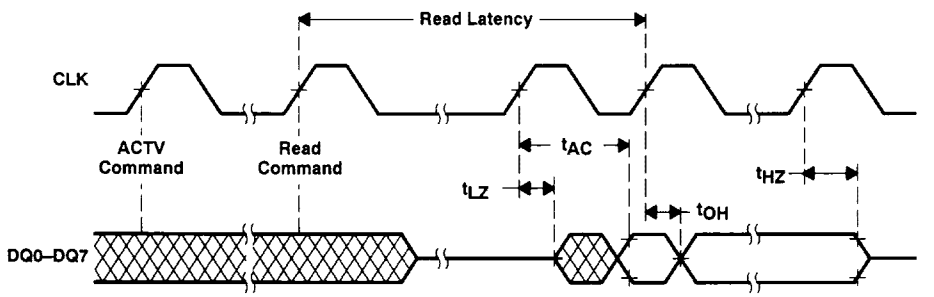



Figure 9. Output Parameters

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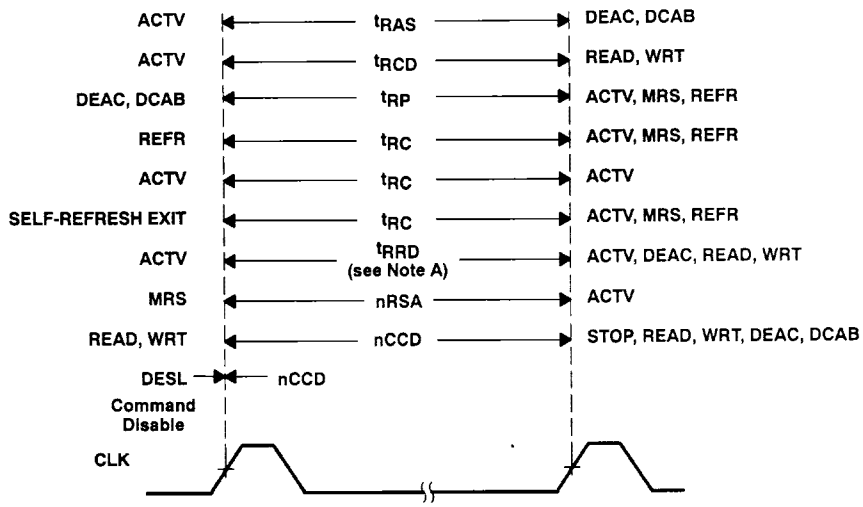
## PARAMETER MEASUREMENT INFORMATION




NOTE A: $t_{RRD}$ is specified for command execution in one bank to command execution in the other bank.

**Figure 10. Command to Command Parameters**

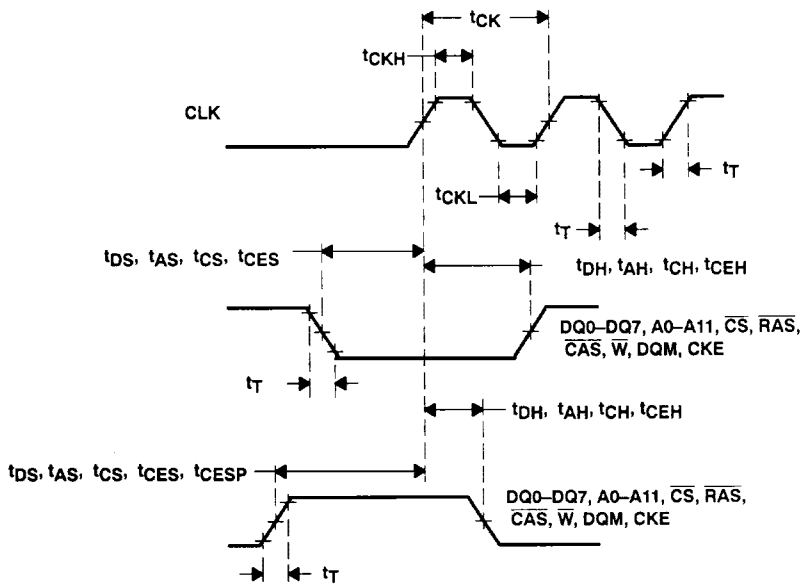



**Figure 11. Input Attribute Parameters**

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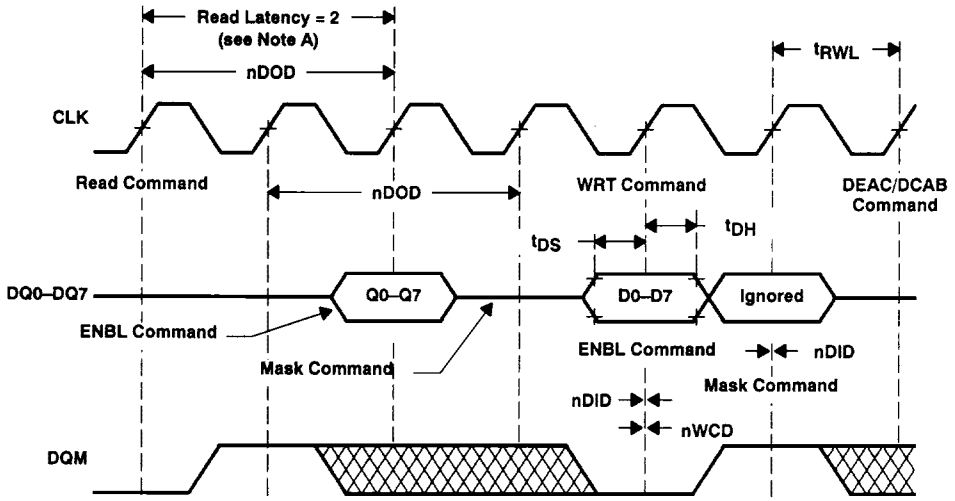
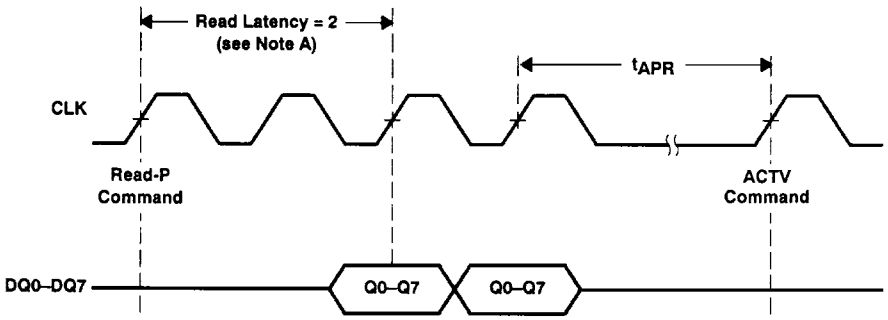
## PARAMETER MEASUREMENT INFORMATION




NOTE A: For purposes of this example assume Read Latency = 2, and Burst Length = 2.

**Figure 12. DQ Parameters**




NOTE A: For purposes of this example assume Read Latency = 2, and Burst Length = 2.

**Figure 13. Read Automatic Deactivate (Autoprecharge)**

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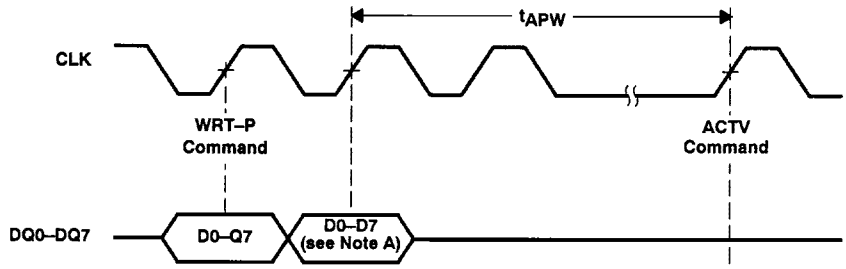
## PARAMETER MEASUREMENT INFORMATION




NOTE A: For purposes of this example the Burst length = 2.

**Figure 14. Write Automatic Deactivate (Autoprecharge)**

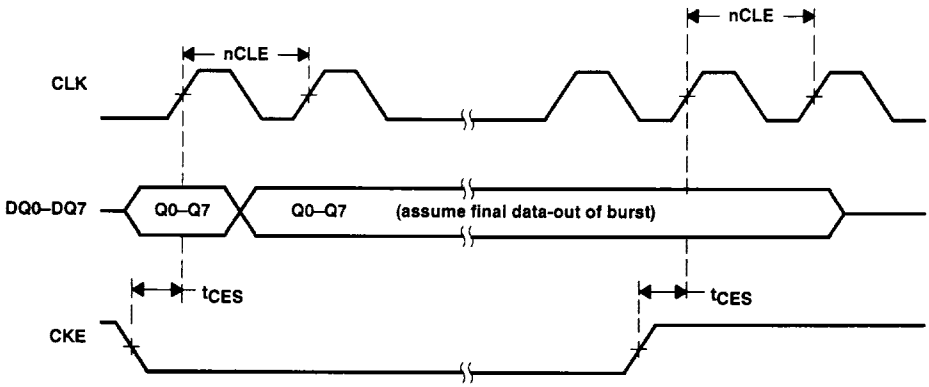



**Figure 15. Figure 12. CLK Suspend Operation**

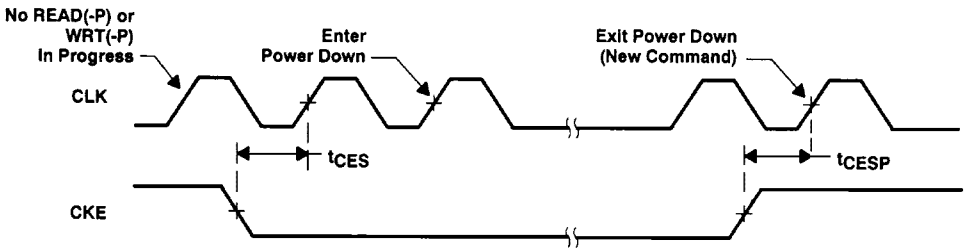



**Figure 16. Power-Down Operation**

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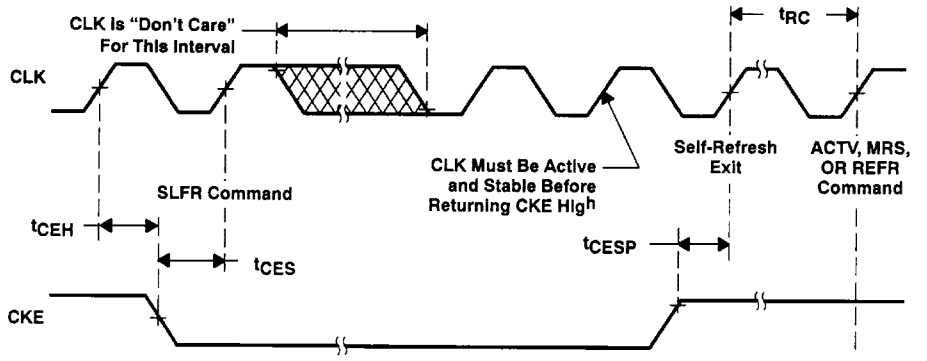
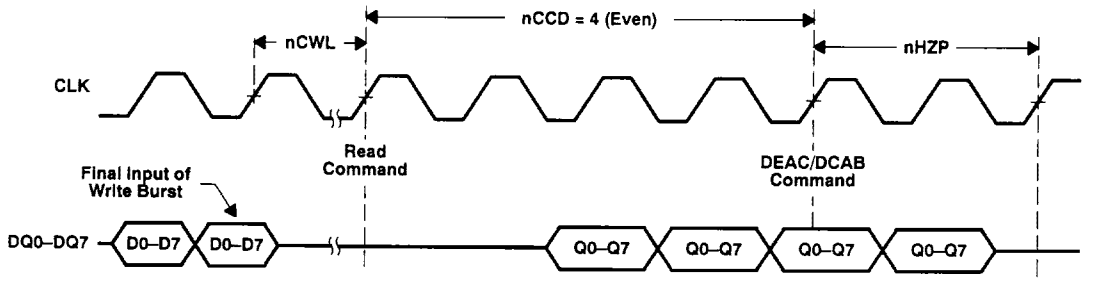
## PARAMETER MEASUREMENT INFORMATION




NOTE: Assume both banks are previously deactivated.

**Figure 17. Self-Refresh Entry/Exit**




NOTE: Assume read latency = 2 and burst length = 8.

**Figure 18. Write Burst Followed By DEAC/DCAB–Interrupted Read**

PRODUCT PREVIEW



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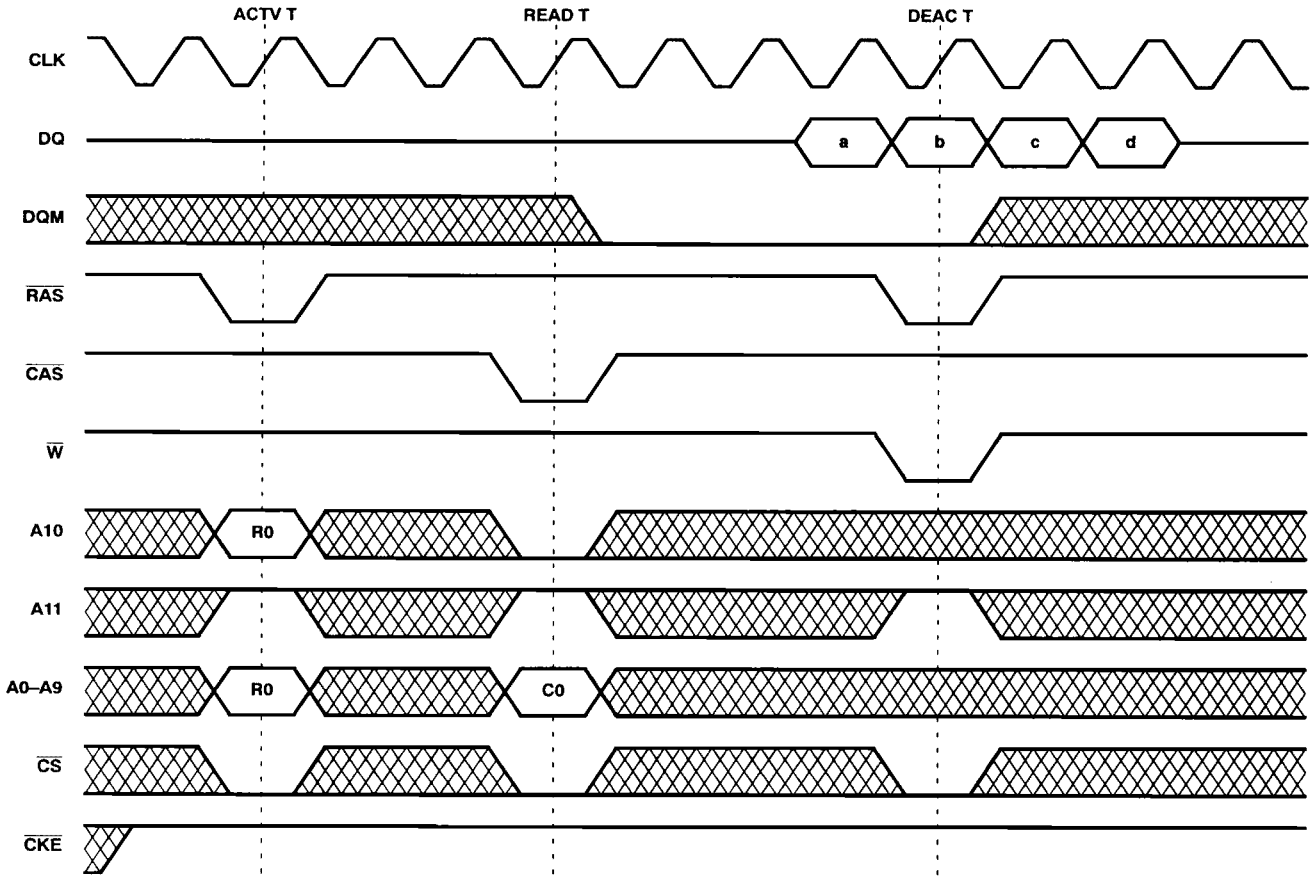


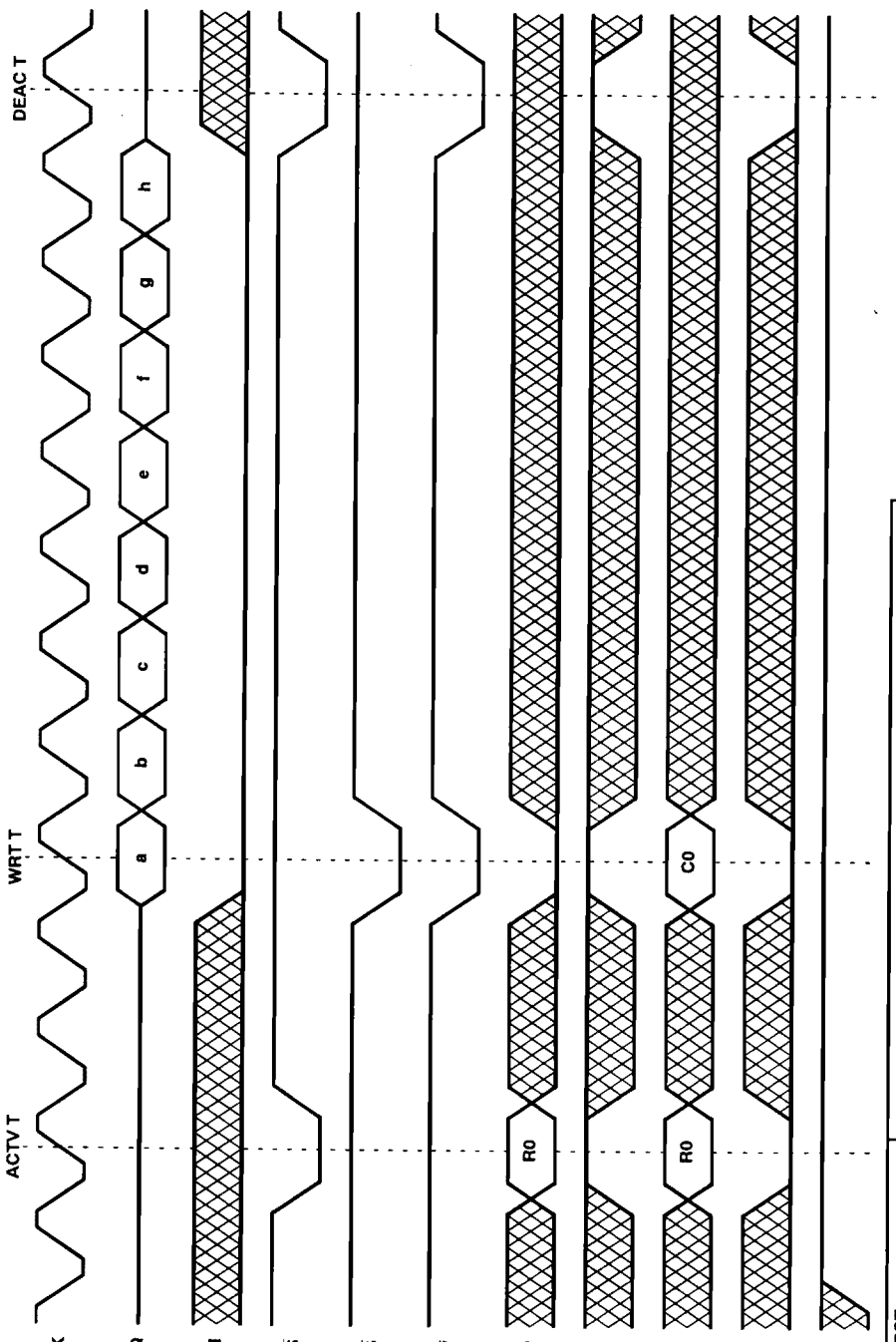

| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d |
|---|---|---|---|---|---|---|
| Q | T | R0 | C0† | C0 + 1 | C0 + 2 | C0 + 3 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 19. Read Burst (Read Latency = 3, Burst Length =4)**



**PRODUCT PREVIEW**




| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | a | b | c | d | e | f | g | h |
| D | T | R0 | C0† | C0 + 1 | C0 + 2 | C0 + 3 | C0 + 4 | C0 + 5 | C0 + 6 | C0 + 7 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)

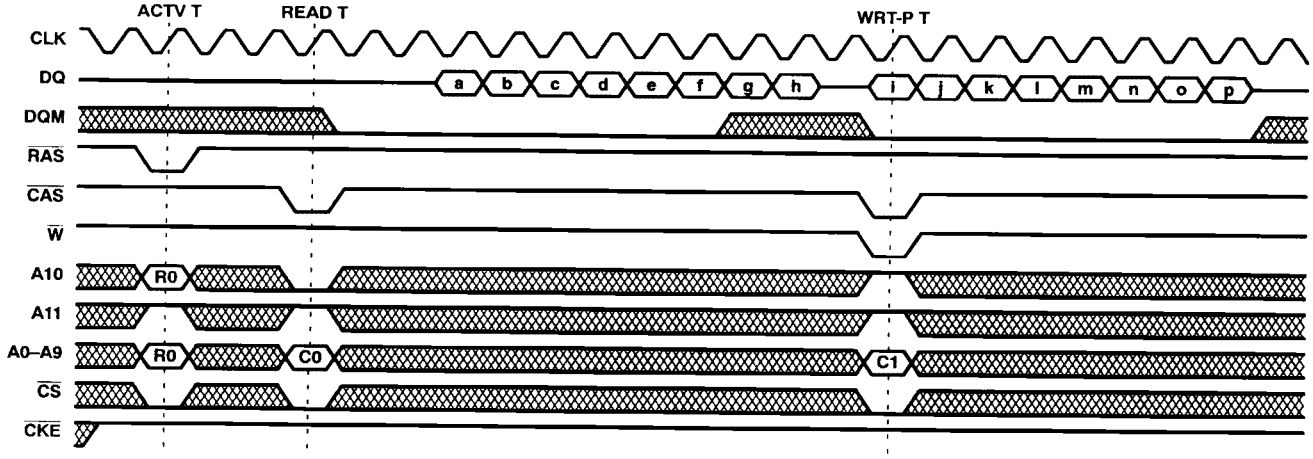
**Figure 20. Write Burst (Burst Length = 8)**

| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d |
|---|---|---|---|---|---|---|
| D | B | R0 | C0† | C0 + 1 | | |
| Q | B | R0 | | | C1‡ | C1 + 1 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 4.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 4.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 21. Write-Read Burst (Read Latency = 3, Burst Length = 2)**

**PRODUCT PREVIEW**




| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o | p |
| Q | T | R0 | C0† | C0+1 | C0+2 | C0+3 | C0+4 | C0+5 | C0+6 | C0+7 | | | | | | | | |
| D | T | R0 | | | | | | | | | C‡ | C1+1 | C1+2 | C1+3 | C1+4 | C1+5 | C1+6 | C1+7 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)
‡ Column address sequence depends on programmed burst type and C1.( Refer to Table 6.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 22. Read-Write Burst With Automatic Deactivate (Read Latency = 3, Burst Length = 8)**



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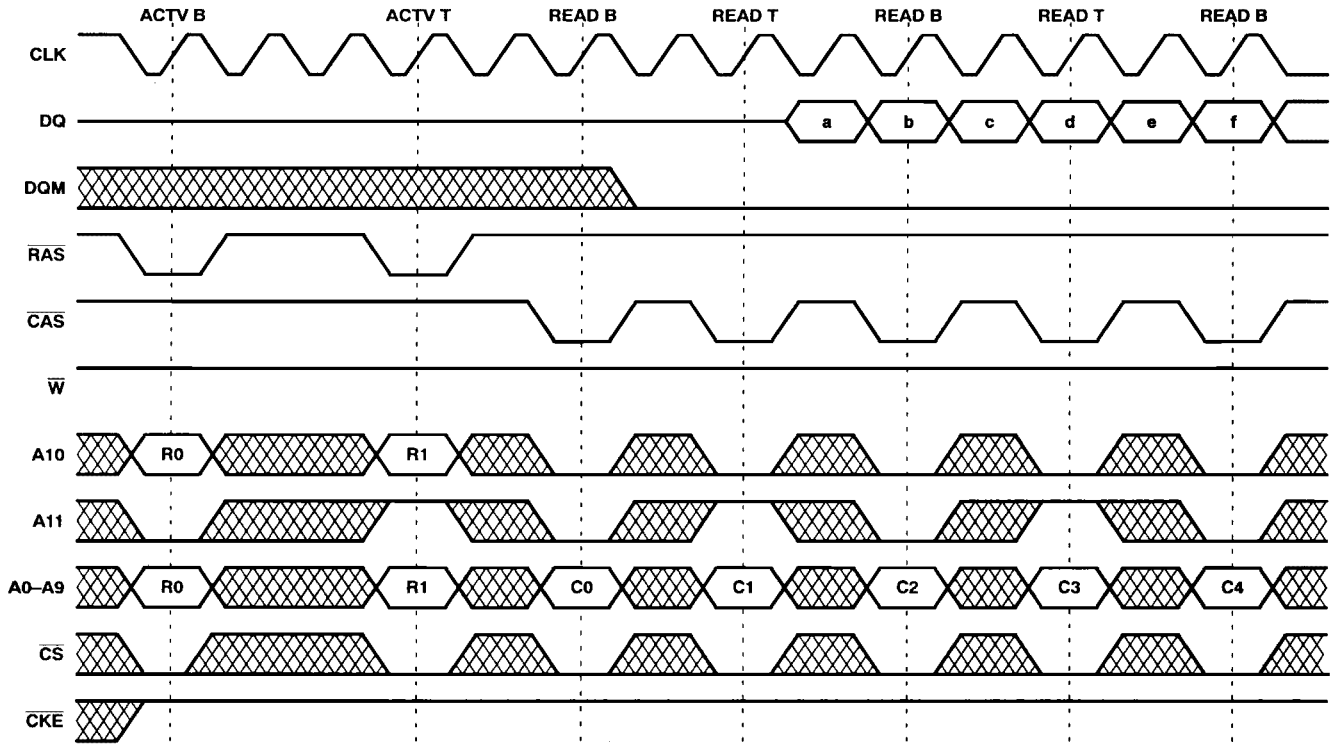


| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d | e | f | . | . |
|---|---|---|---|---|---|---|---|---|---|---|
| Q | B | R0 | C0† | C0 + 1 | | | | | | |
| Q | T | R1 | | | C1‡ | C1 + 1 | | | | |
| Q | B | R0 | | | | | C2§ | C2 + 1 | | |
| . | . | . | | | | | | | . | . |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 4.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 4.)
§ Column address sequence depends on programmed burst type and C2. (Refer to Table 4.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 23. Two-Bank Column Interleaving (Read Latency = 3, Burst Length = 2)**

**PRODUCT PREVIEW**

| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d | e | f | g | h | i | j | k | l | m | n | o | p | q | r | s | . |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Q | B | R0 | C0† | C0+1 | C0+2 | C0+3 | C0+4 | C0+5 | C0+6 | C0+7 | | | | | | | | | | | | |
| Q | T | R1 | | | | | | | | | C1‡ | C1+1 | C1+2 | C1+3 | C1+4 | C1+5 | C1+6 | C1+7 | | | | |
| Q | B | R2 | | | | | | | | | | | | | | | | | C2§ | C2+1 | C2+2 | . |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)
‡ Column address sequence depends on porgrammed burst type and C1.( Refer to Table 6.)
§ Column address sequence depends on porgrammed burst type and C2.( Refer to Table 6.)
NOTE: This example illustrates minimum $^tRCD$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 24. Two-Bank Row Interleaving With Automatic Deactivate (Read Latency = 3, Burst Length = 8)**



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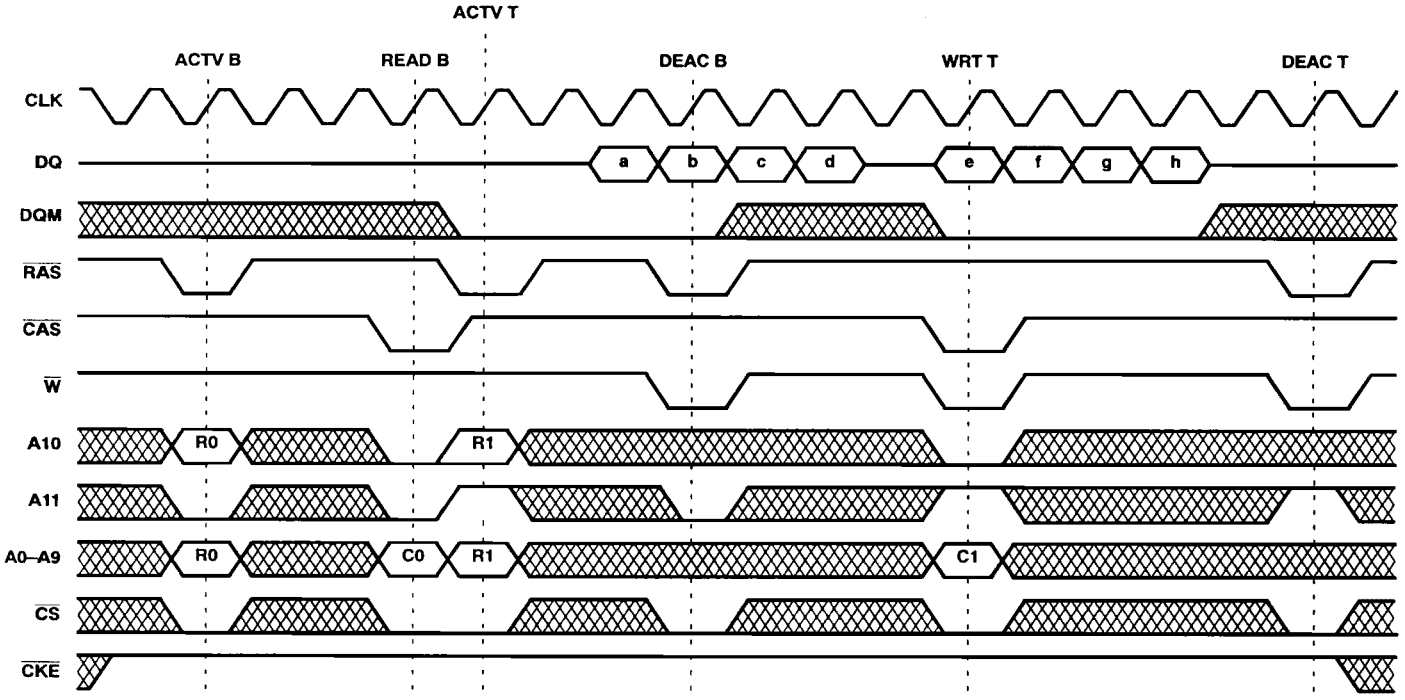
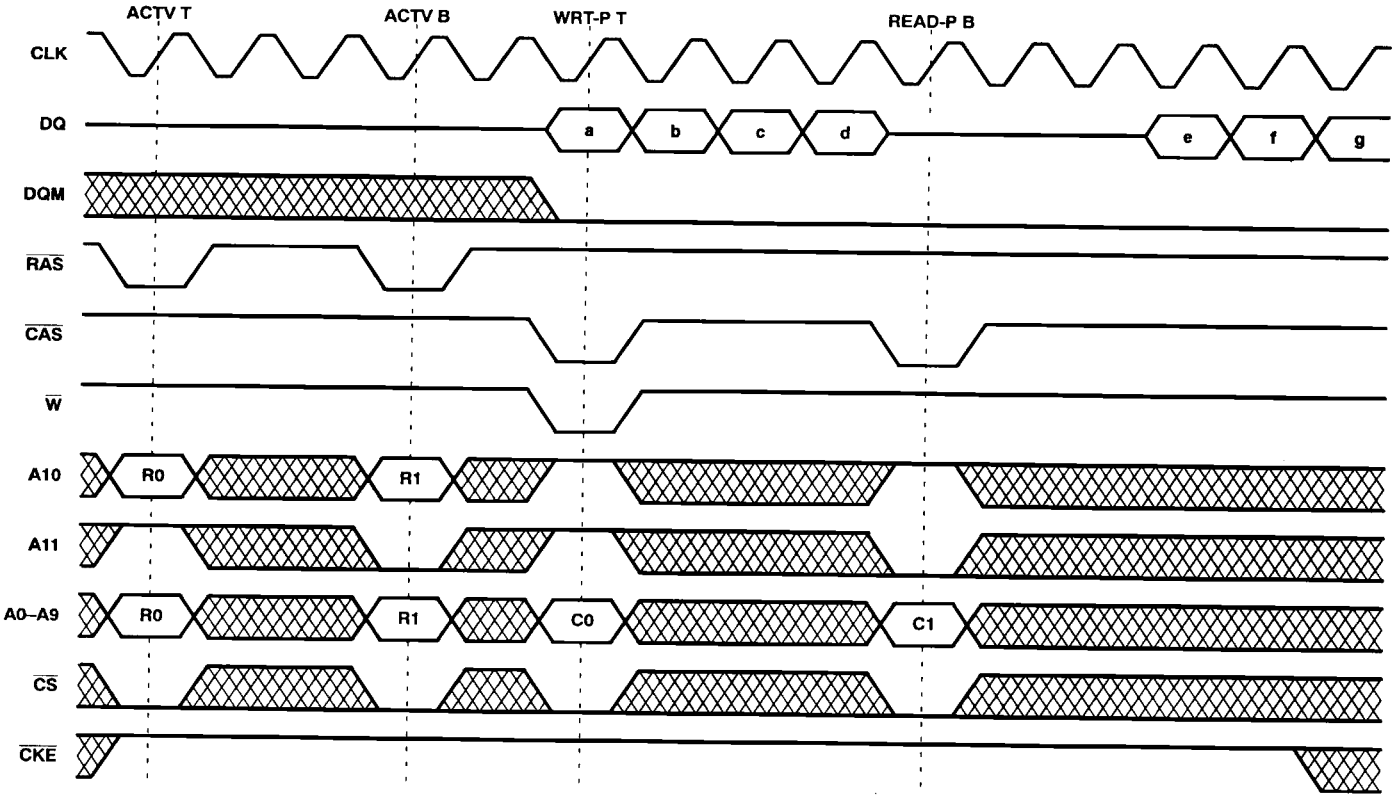



| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d | e | f | g | h |
|---|---|---|---|---|---|---|---|---|---|---|
| Q | B | R0 | C0† | C0+1 | C0+2 | C0+3 | | | | |
| D | T | R1 | | | | | C1‡ | C1+1 | C1+2 | C1+3 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 25. Read Burst Bank B, Write Burst Bank T (Read Latency = 3, Burst Length = 4)**




| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d | e | f | g | h |
|---|---|---|---|---|---|---|---|---|---|---|
| D | T | R0 | C0† | C0+1 | C0+2 | C0+3 | | | | |
| Q | B | R1 | | | | | C1‡ | C1+1 | C1+2 | C1+3 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

**Figure 26. Write Burst Bank T, Read Burst Bank B With Automatic Deactivate (Read Latency = 3, Burst Length = 4)**



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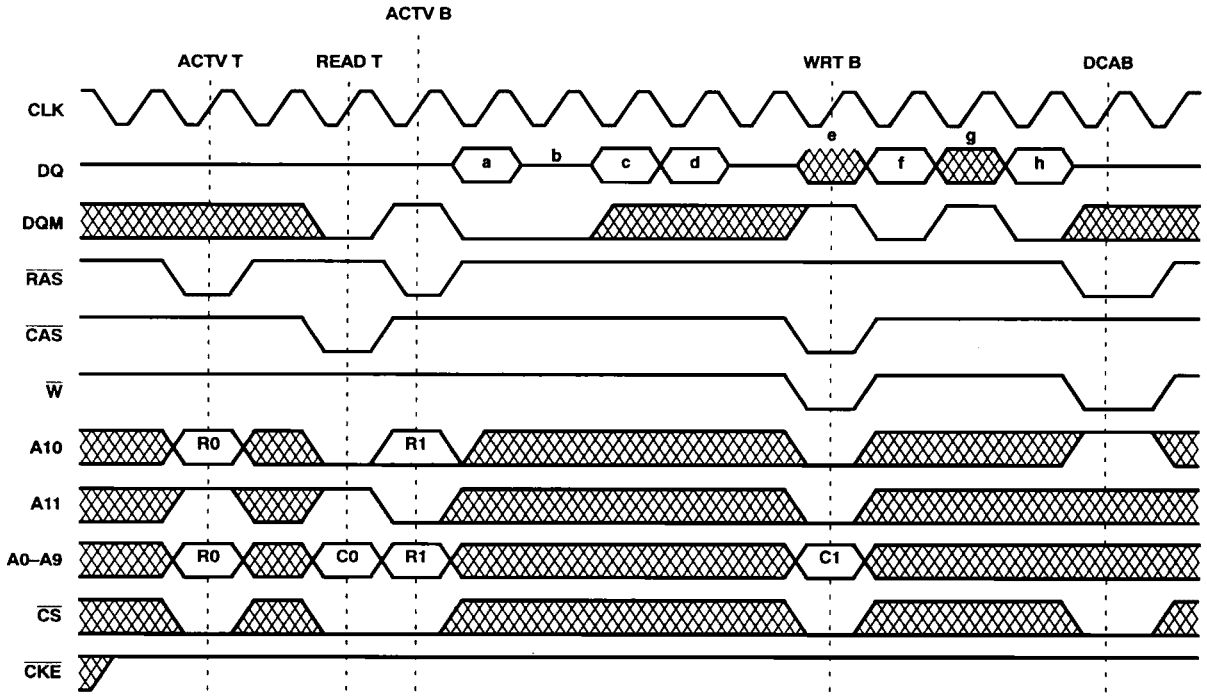


| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d | e | f | g | h |
|---|---|---|---|---|---|---|---|---|---|---|
| Q | T | R0 | C0† | C0+1 | C0+2 | C0+3 | | | | |
| D | B | R1 | | | | | C1‡ | C1+1 | C1+2 | C1+3 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-15 at 50 MHz.

**Figure 27. Use Of DQM For Output and Data-In Cycle Masking (Read Burst Bank T, Write Burst Bank B, Deactivate All Banks) (Read Latency = 2, Burst Length = 4)**



**PRODUCT PREVIEW**

| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | a | b | c | d | e | f | g | h |
| Q | T | R0 | C0† | C0+1 | C0+2 | C0+3 | C0+4 | C0+5 | C0+6 | C0+7 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-12 at 50 MHz.

**Figure 28. Refresh Cycles (Refreshes Followed By Read Burst Followed By Refresh)**
**(Read Latency = 2, Burst Length = 8)**



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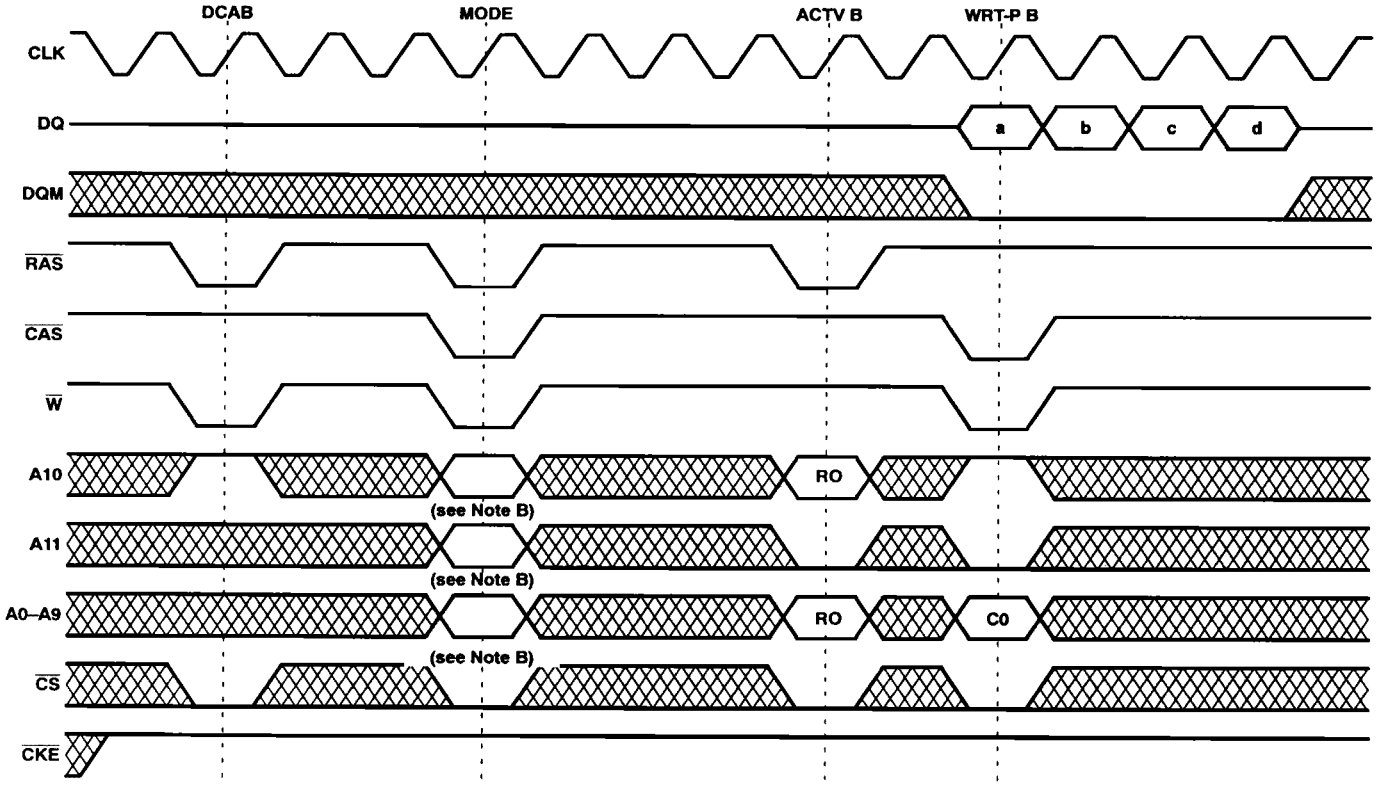



| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d |
|---|---|---|---|---|---|---|
| D | B | R0 | C0† | C0+1 | C0+2 | C0+3 |

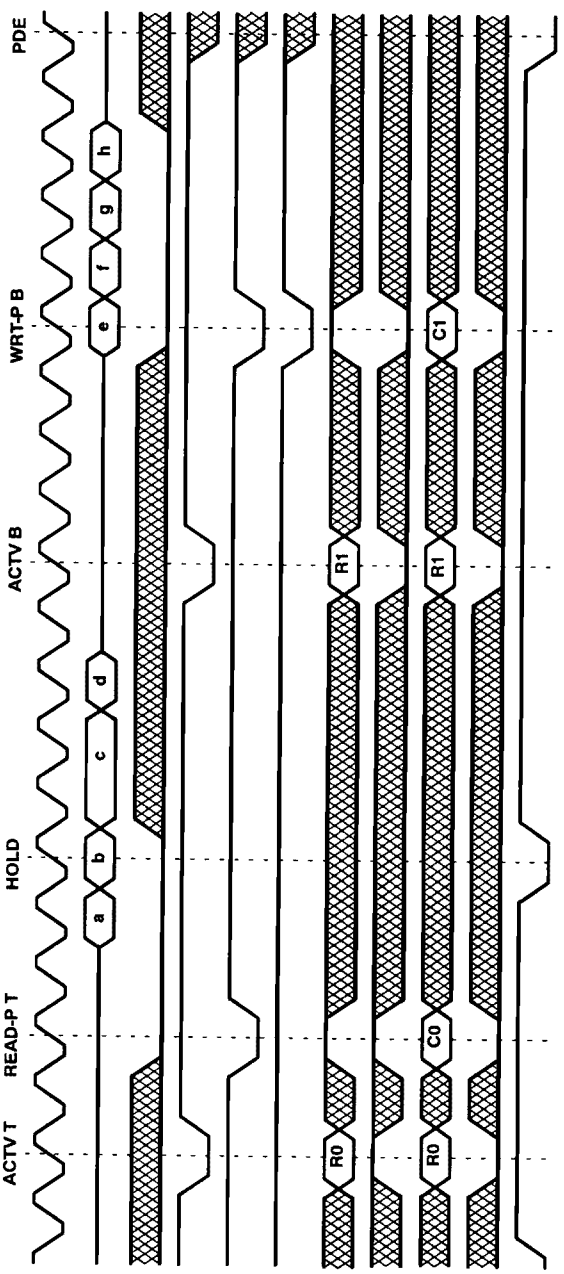
† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)

NOTES: A. This example illustrates minimum $t_{RCD}$ for the SDRAM-15 at 66 MHz.
B. Refer to Figure 1, Mode Register Programming, on page 9.

**Figure 29. Mode Register Programming (Deactivate All, Mode Program, Read Burst With Automatic Deactivate) (Read Latency = 2, Burst Length = 4)**



**PRODUCT PREVIEW**




| BURST TYPE (D/Q) | BANK (B/T) | ROW ADDR | BURST CYCLE a | b | c | d | e | f | g | h |
|---|---|---|---|---|---|---|---|---|---|---|
| Q | T | R0 | C0† | C0+1 | C0+2 | C0+3 | | | | |
| D | B | R1 | | | | | C1‡ | C1+1 | C1+2 | C1+3 |

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum $t_{RCD}$ and nCL for the SDRAM-15 at 50 MHz.

**Figure 30. Use Of $\overline{CKE}$ For Clock Gating (Hold) And Standby Mode (Read Burst Bank T With Hold, Write Burst Bank B, Standby Mode) (Read Latency = 2, Burst Length = 4)**