

Description

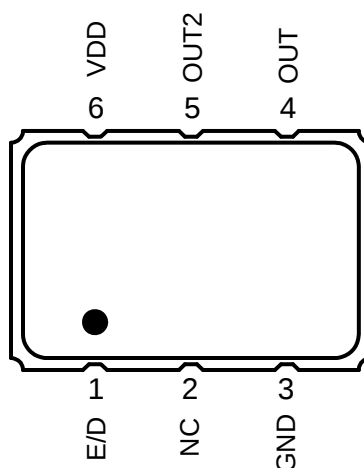
The XUN is an Ultra Precision HCSL crystal oscillator with 300fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 16kHz to 670MHz, the IDT XUN series crystal oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 4th order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XUN is an excellent choice over the conventional technologies. The XUN has stabilities as tight as $\pm 20\text{ppm}$ with extremely quick delivery for both standard and custom frequencies

Features

- Frequency range: 0.016MHz to 670MHz
- Output type: HCSL
- Frequency stability: $\pm 20\text{ppm}$, $\pm 25\text{ppm}$, $\pm 50\text{ppm}$, or $\pm 100\text{ppm}$
- Supply voltage: 1.8V, 2.5V, or 3.3V
- Phase jitter (1.875MHz to 20MHz): 100fs typical
- Phase jitter (12kHz to 20MHz): 300fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6)
7.0mm x 5.0mm x 1.3mm (JU6)
- Operating temperatures: -20°C to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$

Pin Assignment



6-pin CLCC

Pin Descriptions

Pin Number	Pin Name	Description
1	E/D	Enable/Disable ¹ (0=Output Disabled)
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output
6	VDD	Supply Voltage

1. Pulled high internally.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XUN. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0V
E/D	-0.5V to VDD + 0.5V
OUT	-0.5V to VDD + 0.5V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

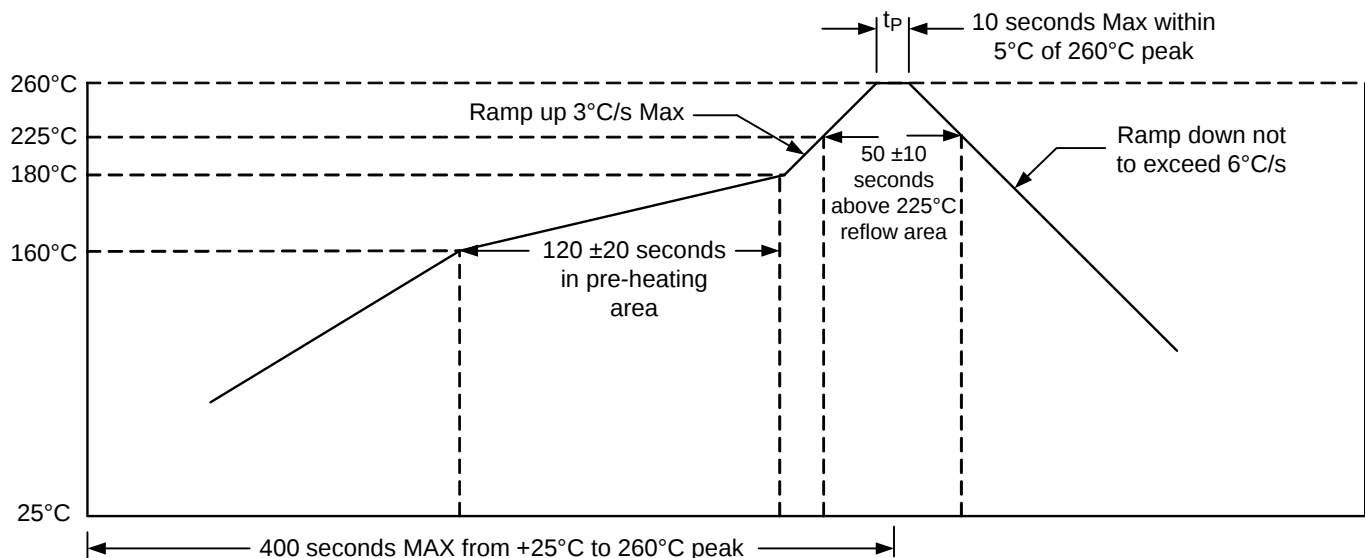
ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

Mechanical Testing

Parameter	Test Method
Mechanical Shock	Half-Sine wave with 0.3ms 3000G X, Y, Z each direction 1 time
Mechanical Vibration	Frequency: 10 to 55 MHz Amplitude: 1.5mm Frequency: 55~2000Hz Peak value: 20G Duration time: 4H for each X,Y,Z axis Total 12 hours
High Temp Operating Life (HTOL)	2000 Hours, 125°C (under power)
Hermetic Seal	Gross leak (Air leak test) Fine leak (Helium leak test) He-pressure: 6kgf/cm ² 2 hours

Solder Reflow Profile



DC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	Standard frequencies			145	mA
Output HIGH Voltage	V_{OH}	Std HCSL load	0.6		1.1	V
Output LOW Voltage	V_{OL}	Std HCSL load	0		0.2	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				$30\%V_{DD}$	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	± 20		± 100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	± 25		± 100	ppm
Aging (1 st year)		$T_a = 25^\circ C$			± 3	
Aging (10 years)		$T_a = 25^\circ C$			± 10	
Output Load		To GND		50		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP} (Standard frequencies)			330	ps
Output Fall Time		80% to 20% V_{PP} (Standard frequencies)			330	ps
Output Clock Duty Cycle	T_{DTCY}	At 50% V_{PP}	45		55	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		7	10	ps
Random Jitter	R_J	Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		0.6	0.7	ps
Deterministic Jitter	D_J			10	22	ps
Total Jitter	T_J			19	31	ps
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	Standard frequencies		300	400	fs
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-90		dBc/Hz
		1kHz of Carrier		-113		dBc/Hz
		10kHz of Carrier		-121		dBc/Hz
		100kHz of Carrier		-129		dBc/Hz
		1MHz of Carrier		-147		dBc/Hz
		10MHz of Carrier		-156		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at $25^\circ C$. We do not recommend hand soldering the devices

DC Characteristics

($V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	Standard frequencies			102	mA
Output HIGH Voltage	V_{OH}	Std HCSL load	0.55		0.95	V
Output LOW Voltage	V_{OL}	Std HCSL load	0		0.2	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				$30\%V_{DD}$	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

($V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	± 20		± 100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	± 25		± 100	ppm
Output Load		To GND		50		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP} (Standard frequencies)			315	ps
Output Fall Time		80% to 20% V_{PP} (Standard frequencies)			315	ps
Output Clock Duty Cycle	T_{DTCY}	At 50% V_{PP}	45		55	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		7	10	ps
Random Jitter	R_J	Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		0.7	1	ps
Deterministic Jitter	D_J			10	20	ps
Total Jitter	T_J			20	31	ps
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	Standard frequencies		350	500	fs
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-95		dBc/Hz
		1kHz of Carrier		-1113		dBc/Hz
		10kHz of Carrier		-123		dBc/Hz
		100kHz of Carrier		-129		dBc/Hz
		1MHz of Carrier		-147		dBc/Hz
		10MHz of Carrier		-153		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at $25^\circ C$. We do not recommend hand soldering the devices

DC Characteristics

($V_{DD} = 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	Standard frequencies			68	mA
Output HIGH Voltage	V_{OH}	Std HCSL load	0.45		0.7	V
Output LOW Voltage	V_{OL}	Std HCSL load	0		0.2	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				$30\%V_{DD}$	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

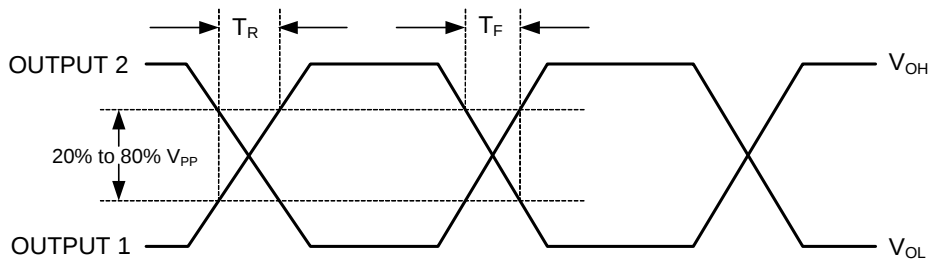
($V_{DD} = 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	± 20		± 100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	± 25		± 100	ppm
Output Load		To GND		50		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP} (Standard frequencies)			320	ps
Output Fall Time		80% to 20% V_{PP} (Standard frequencies)			320	ps
Output Clock Duty Cycle	T_{DTCY}	At 50% V_{PP}	40		60	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		7	10	ps
Random Jitter	R_J	Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		0.85	1.2	ps
Deterministic Jitter	D_J			10	22	ps
Total Jitter	T_J			20	35	ps
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	Standard frequencies		1	1.2	ps
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-84		dBc/Hz
		1kHz of Carrier		-105		dBc/Hz
		10kHz of Carrier		-111		dBc/Hz
		100kHz of Carrier		-121		dBc/Hz
		1MHz of Carrier		-144		dBc/Hz
		10MHz of Carrier		-148		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

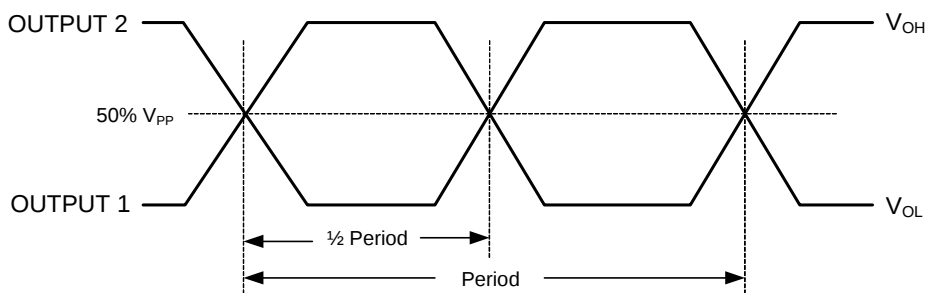
Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at $25^\circ C$. We do not recommend hand soldering the devices

Output Waveform

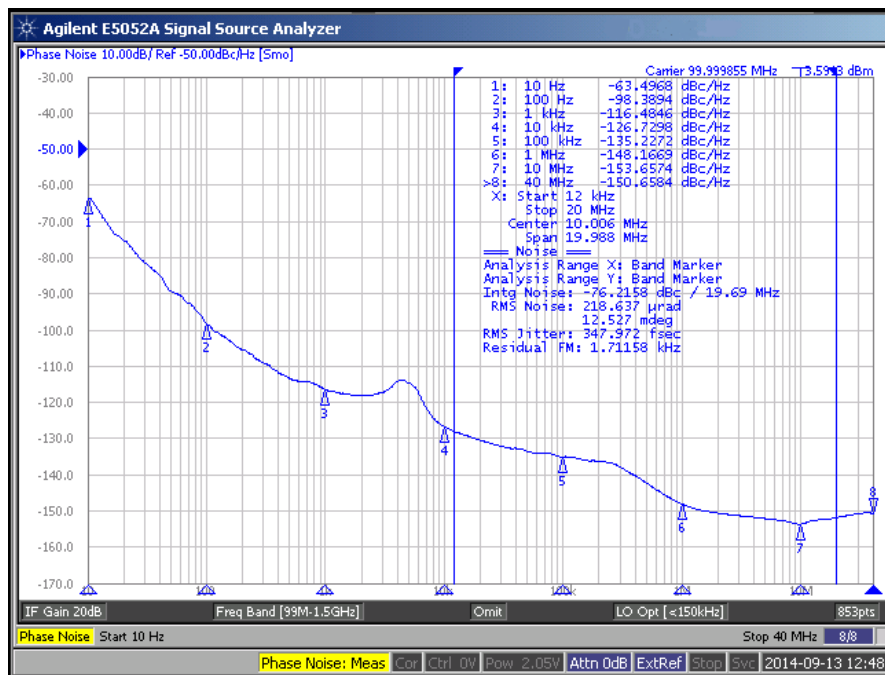
Rise Time/Fall Time Measurements



Oscillator Symmetry

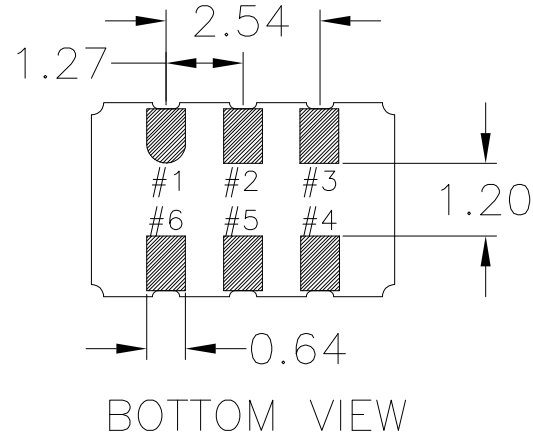
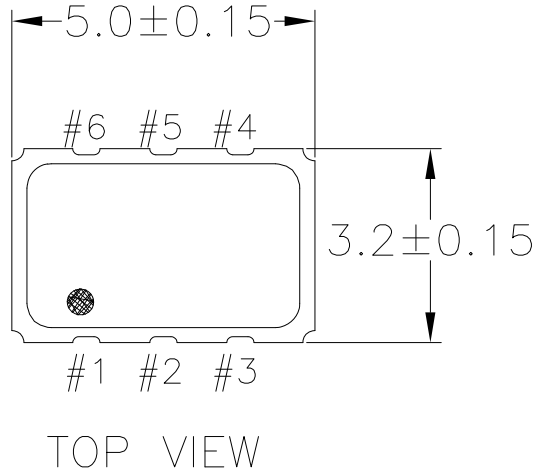
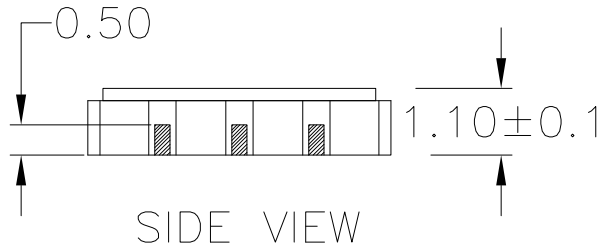


Typical Phase Noise (3.3V)



NOTES:

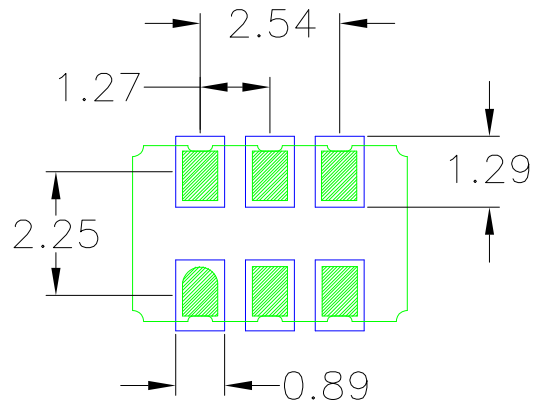
1. ALL DIMENSIONS IN MM.



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.com	
DECIMAL	ANGULAR		
XX±	±	TITLE JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick	
XXX±			
XXXX±		SIZE C DRAWING No. PSC-4411 REV 03	
APPROVALS	DATE		
DRAWN <i>BAC</i>	04/2/12	DO NOT SCALE DRAWING SHEET 1 OF 2	
CHECKED			

JS6 Package Outline and Dimensions (cont.)



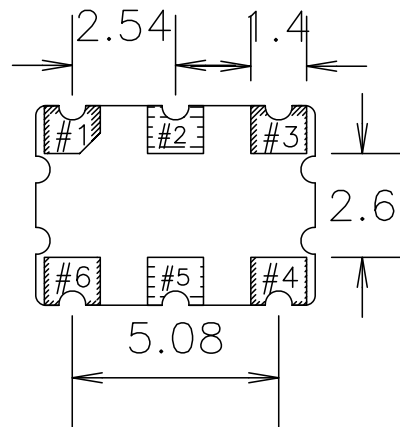
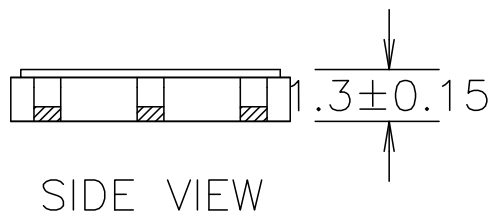
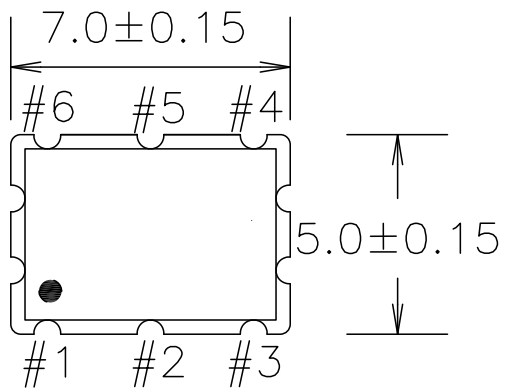
RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA

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DECIMAL	ANGULAR		
XX±	±	www.IDT.com	
XXX±		TITLE JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick	
XXXX±			
APPROVALS	DATE	SIZE	DRAWING No.
DRAWN <i>rac</i>	04/2/12	C	PSC-4411
CHECKED			REV 0.3
DO NOT SCALE DRAWING		SHEET 2 OF 2	

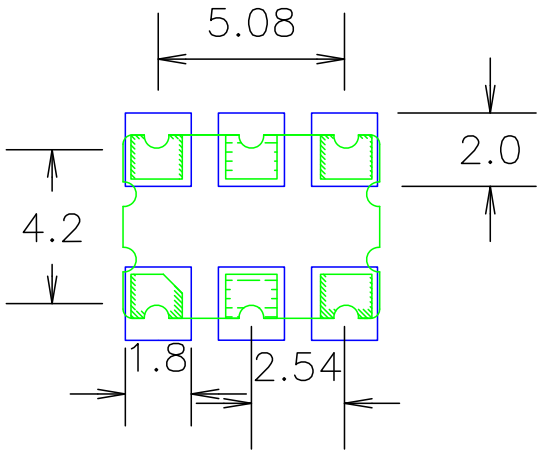


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA

NOTES:
1. ALL DIMENSIONS IN MM.

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DECIMAL	ANGULAR		
XX±	±	TITLE JU6 PACKAGE OUTLINE 7.0 x 5.0 mm BODY 1.3 mm Thick	
XXX±			
XXXX±		SIZE C DRAWING No. PSC-4430 REV 01	
APPROVALS	DATE		
DRAWN JCS	10/03/12	DO NOT SCALE DRAWING	
CHECKED			
		SHEET 1 OF 2	

JU6 Package Outline and Dimensions (cont.)



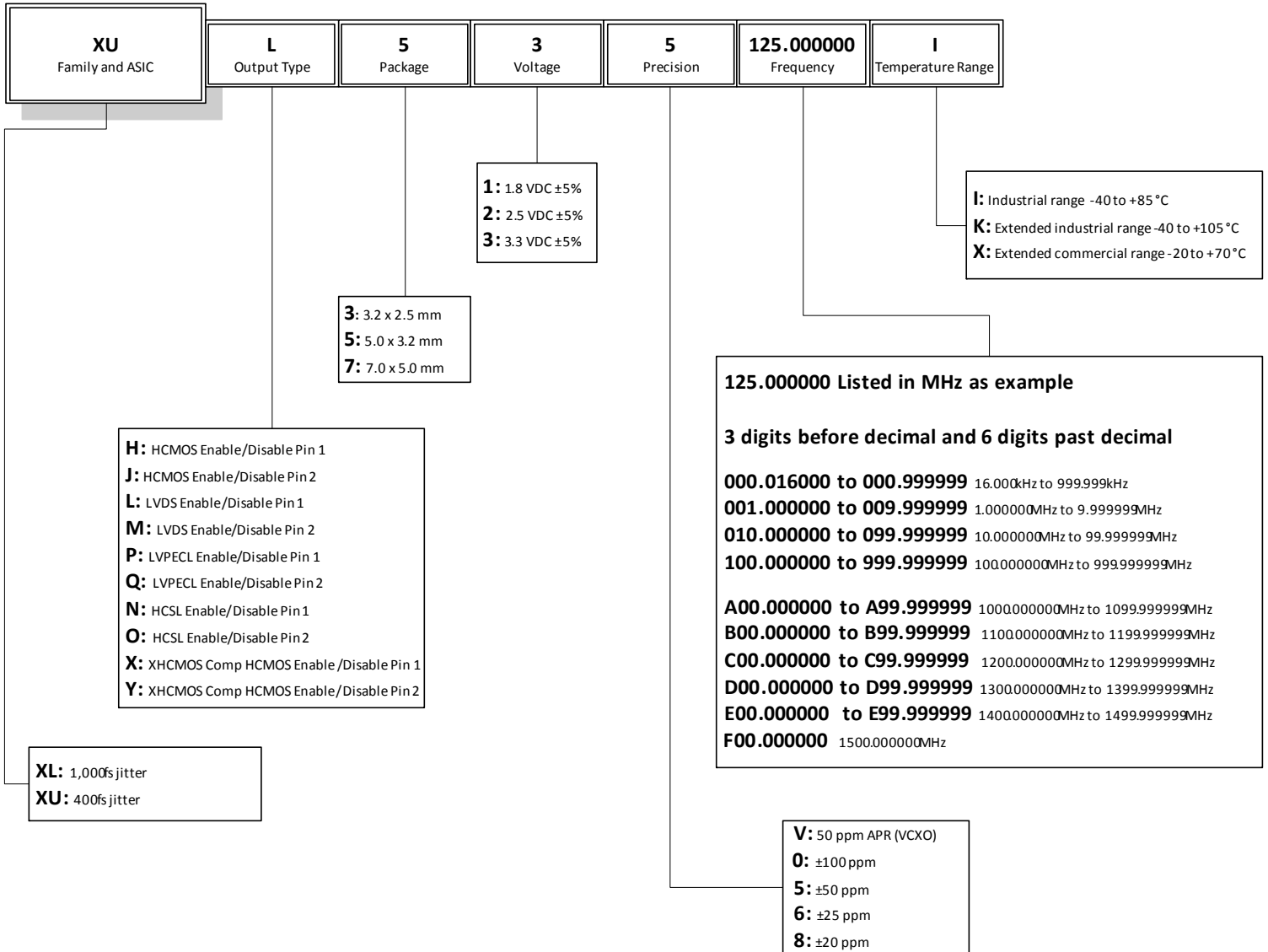
RECOMMENDED LAND PATTERN

- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW. AS VIEWED ON PCB.
 3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA

TOLERANCES UNLESS SPECIFIED		 IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-8116 FAX: (408) 492-8674	
DECIMAL	ANGULAR			
XX.X				
XXX.X				
APPROVALS	DATE	TITLE		
DRAWN <u>XX.X</u>	10/03/12	JU6 PACKAGE OUTLINE		
CHECKED		7.0 x 5.0 mm BODY		
		1.3 mm Thick		
		SIZE	DRAWING No.	REV
		C	PSC-4430	01
DO NOT SCALE DRAWING			SHEET 2 OF 2	

IDT Ordering Information



Revision History

Date	Originator	Description of Change
10/01/14	B. Chandhoke	1. Corrected typo in spec for Enable/Disable Low Voltage; from $\geq 30\%VDD$ to $\leq 30\%VDD$. 2. Moved from Advance to Preliminary.
12/15/14	B. Chandhoke	1. Added 7 x 5 x 1.3mm JU6 package option and package dimension/landing pattern drawings. 2. Updates to all DC char tables. 3. Updates to all AC char tables. 4. Updated ordering information table/graphic to show JU6 package option
10/28/16	P. Jenkins	Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables.
06/13/17	L.S.	Removed "Ordering Information Scheme #1 (for reference only)". Replaced with a single ordering information table.
06/20/17	L.S.	Corrected frequency errors in Ordering Information table.



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