MH1M08TNA-85L,-10L,-12L,-15L/ MH1M08TNA-85H,-10H,-12H,-15H

8388608-BIT(1048576-WORD BY 8-BIT)CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

The MH1M08TNA is a 8388608 bits CMOS static RAM module organized as 1048576-words by 8-bits. It consists of eight industry standard 128K x 8 static RAMs and one decoder.

The stand-by current is low enough for a battery back-up application. It is mounted a TSOP package on a 36-pin dual in line package.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH1M08TNA-85L	85ns	50mA	450μA
MH1M08TNA-10L	100ns		
MH1M08TNA-12L	120ns		
MH1M08TNA-15L	150ns		
MH1M08TNA-85H	85ns		130μA
MH1M08TNA-10H	100ns		
MH1M08TNA-12H	120ns		
MH1M08TNA-15H	150ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O
- 36-pin 600 mil Dual in-line package.

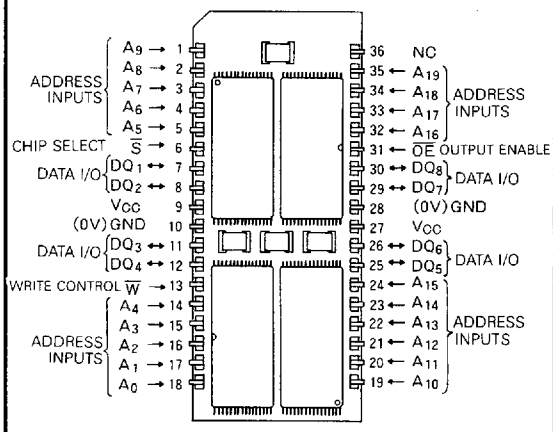
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the MH1M08TNA is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

PIN CONFIGURATION (TOP VIEW)



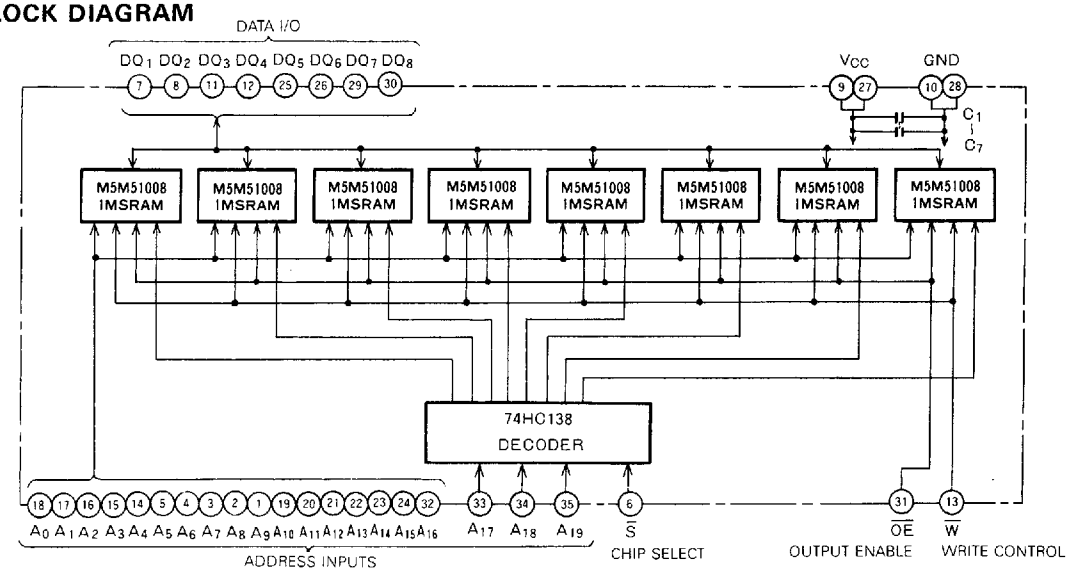
Outline 36N1C NC:NO CONNECTION

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

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selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−40~100	°C

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High input voltage			3.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage	I_{OH}=−1mA		2.4			V
V_{OL}	Low output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0~V_{CC}				±8	μA
I_O	Output current in off-state	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0~V_{CC}				±8	μA
I_{CC1}	Active supply current (AC. MOS level)	$\overline{S}$<0.2, $\overline{W}$>V_{CC}−0.3 output open other input <0.2 or >V_{CC}−0.3 Min. cycle			50	110	mA
I_{CC2}	Active supply current (AC. TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} output open other input =V_{IL} or V_{IH} Min. cycle			60	120	mA
I_{CC3}	Stand-by supply current	$\overline{S}$≧V_{CC}−0.2V, A_{15}~A_{19} ≦0.2 or ≧V_{CC}−0.2 Other inputs=0~V_{CC}	TNA-L			800	μA
			TNA-H		13	165	
I_{CC4}	Stand-by supply current	$\overline{S}$=V_{IH}, Other inputs=0~V_{CC}				24	mA
C_I	Input capacitance (T_a = 25°C)	V_I=GND, V_i=25mVmrs, f=1MHz				70	pF
C_O	Output capacitance (T_a = 25°C)	V_O=GND, V_O=25mVrms, f=1MHz				80	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
2: Typical value is V_{CC} = 5V, T_a = 25°C

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SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limit												Unit
		MH1M08TNA-85L MH1M08TNA-85H			MH1M08TNA-10L MH1M08TNA-10H			MH1M08TNA-12L MH1M08TNA-12H			MH1M08TNA-15L MH1M08TNA-15H			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			120			150			ns
$t_{a(A)}$	Address access time			85			100			120			150	ns
$t_{a(S)}$	Chip select access time			85			100			120			150	ns
$t_{a(OE)}$	Output enable access time			35			45			50			60	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			40			45			50			55	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30			35			40	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5			5			5			5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			5			5			ns
$t_{v(A)}$	Data valid time after address change	10			10			10			10			ns

TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limit												Unit
		MH1M08TNA-85L MH1M08TNA-85H			MH1M08TNA-10L MH1M08TNA-10H			MH1M08TNA-12L MH1M08TNA-12H			MH1M08TNA-15L MH1M08TNA-15H			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			120			150			ns
$t_{w(W)}$	Write pulse width	55			65			75			85			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(A-\overline{WH})}$	Address set up time with respect to $\overline{W}$ high	65			75			85			100			ns
$t_{su(S)}$	Chip select set up time	80			90			100			115			ns
$t_{su(D)}$	Data set up time	30			35			40			45			ns
$t_{h(D)}$	Data hold time	0			0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35			40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			5			5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			5			5			ns

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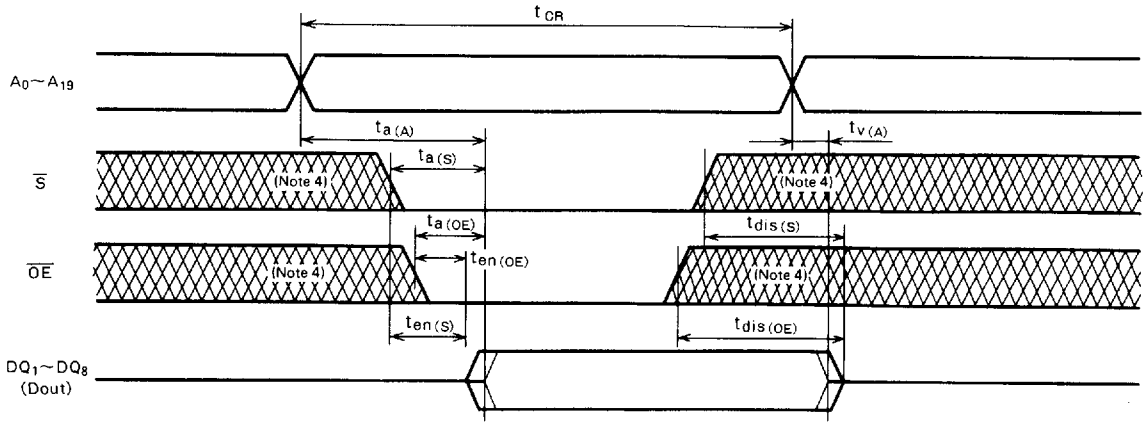
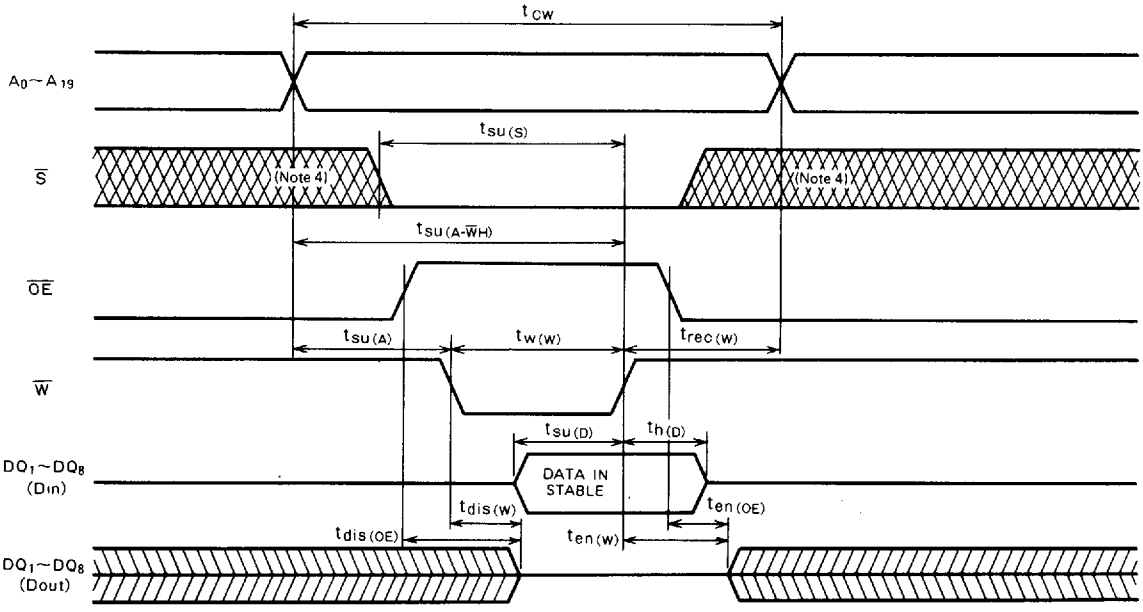
TIMING DIAGRAM

Read cycle



W="H" level

Write cycle (W control)



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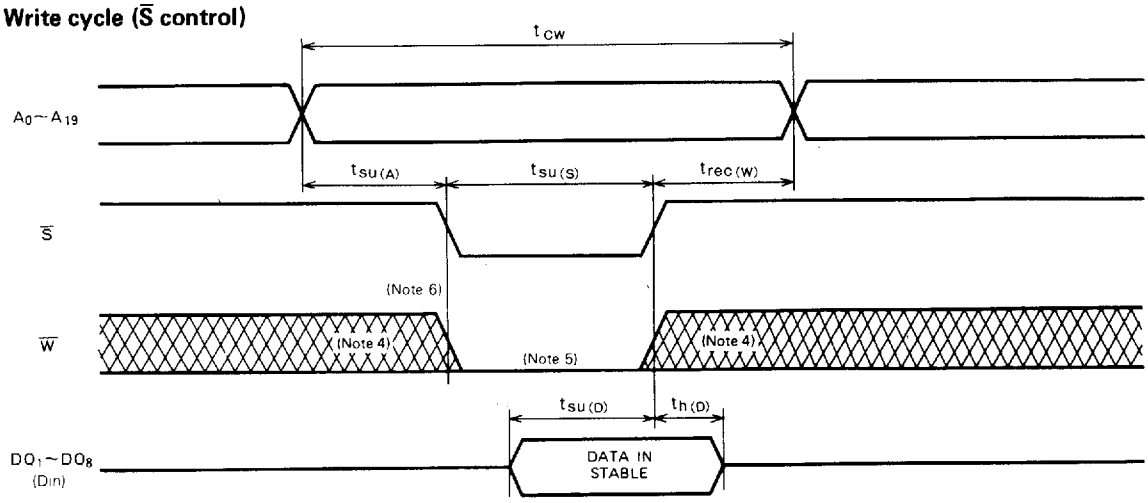
Write cycle ($\overline{S}$ control)



Note 3 Test condition
Input pulse level: 0.6~2.4V
Input pulse rise fall time: 10ns
Load 1 TTL, C_L = 100pF
Conditions of assessment: 1.5V
4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If W goes low simultaneously with or prior to $\overline{S}$, the output remains in the high, impedance state.
7. Don't active inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

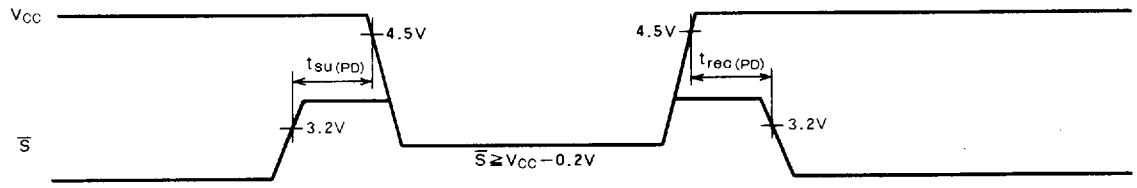
ELECTRICAL CHARACTERISTICS (T_a=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V≦$V_{CC(PD)}$		3.2			V
		2V≦$V_{CC(PD)}$≦2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, A_{15}~A_{19} <0.2 or >V_{CC}−0.2 other inputs=0~V_{CC}	TNA-L			450	μA
			TNA-H			130	

TIMING REQUIREMENTS (T_a=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS



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