June 1990
Edition 2.0

FUJITSU

DATA SHEET

MB814101-80/-10/-12

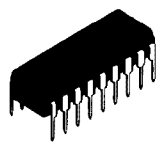
CMOS 4,194,304 BIT NIBBLE MODE DYNAMIC RAM

CMOS 4,194,304 x 1 Bit Nibble Mode Dynamic RAM

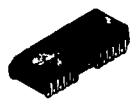
The Fujitsu MB814101 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814101 features a nibble mode of operation whereby high-speed serial access of up to 4 bits of data can be selected. The MB814101 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814101 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

The MB814101 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814101 are not critical and all inputs are TTL compatible.

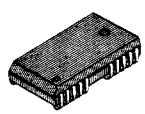
PRELIMINARY



DIP–18P–M04



LCC–26P–M04



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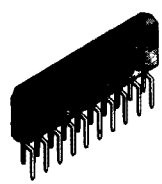

ZIP–20P–M02

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Features

Parameter	MB814101-80	MB814101-10	MB814101-12
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	30 ns max.	35 ns max.
Nibble Mode Cycle Time	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)		

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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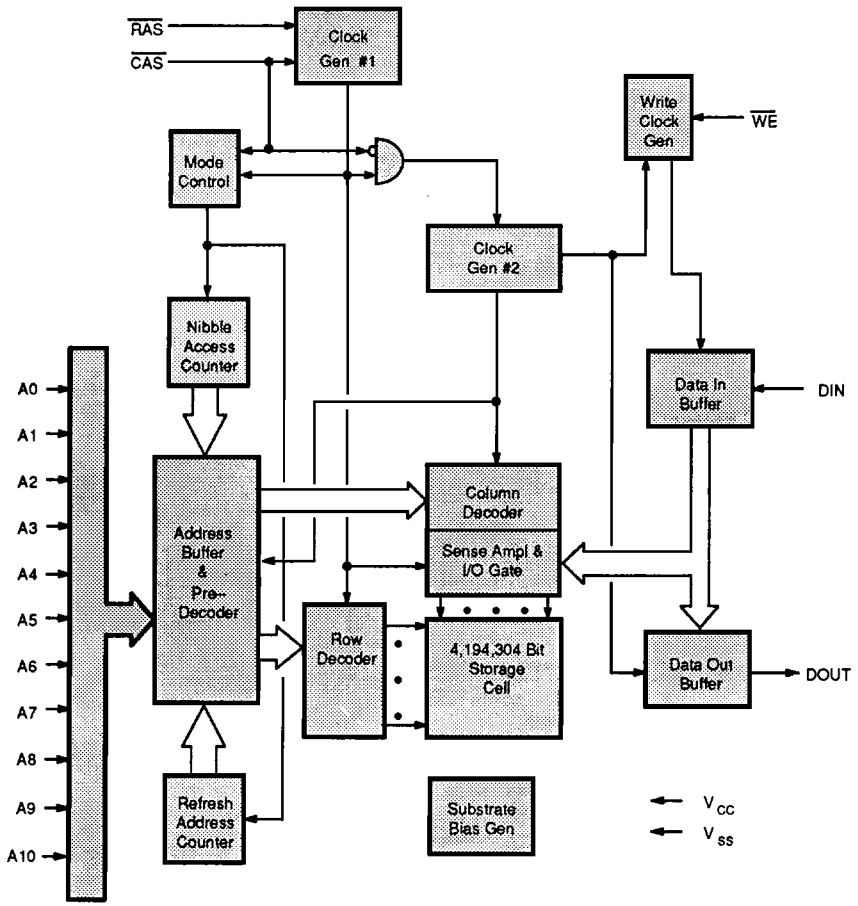
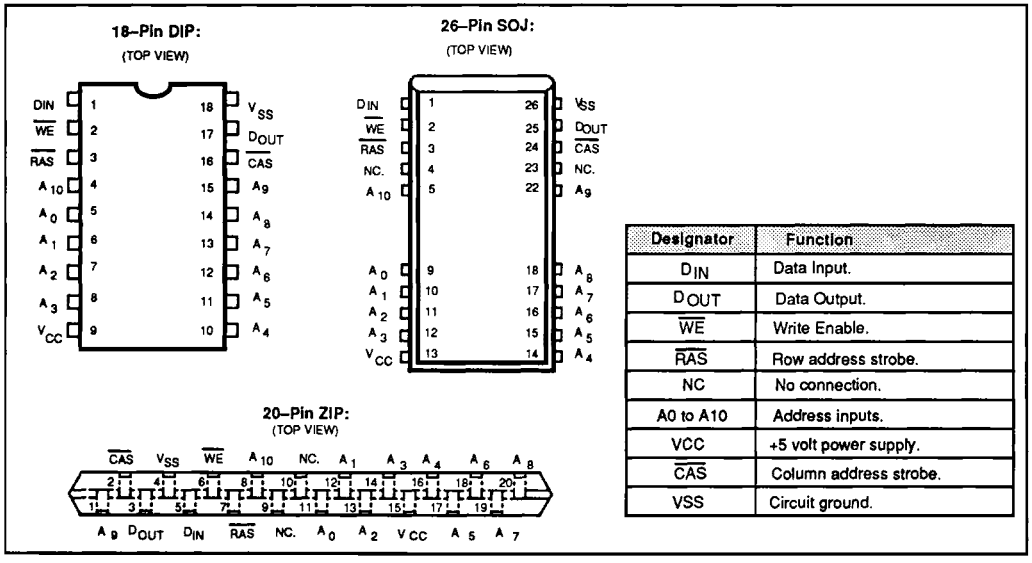
Fig. 1 – MB814101 DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, DOUT	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A10	Address inputs.
VCC	+5 volt power supply.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty–two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A0–A10) are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 4. First, eleven row address bits are applied on pins A0–through–A10 and latched with the row address strobe ($\overline{RAS}$) then, eleven column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

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Input data is written into memory in either of two basic ways—an early write cycle and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

t_{CAC} : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = −5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	−10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	−10	—	10	µA
Operating current (Average Power supply current)	MB814101-80	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814101-10					65	
	MB814101-12					55	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} −0.2V			1.0	
Refresh current #1 (Average power supply current)	MB814101-80	I_{CC3}	$\overline{CAS}$ = VIH, $\overline{RAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814101-10					65	
	MB814101-12					55	
Nibble Mode current	MB814101-80	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	50	mA
	MB814101-10					45	
	MB814101-12					40	
Refresh current #2 (Average power supply current)	MB814101-80	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	75	mA
	MB814101-10					65	
	MB814101-12					55	

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814101-80		MB814101-10		MB814101-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	185	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	30	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	20	—	25	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	20	—	25	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814101-80		MB814101-10		MB814101-12		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	30	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	10	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	20	—	ns
41	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
42	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	15	—	15	—	20	—	ns
51	Nibble Mode Read/Write Cycle Time		t_{NC}	50	—	55	—	60	—	ns
52	Nibble Mode Read-Modify-Write Cycle Time		t_{NRWC}	75	—	80	—	90	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	45	—	50	—	55	ns
54	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15	—	15	—	15	—	ns

Notes:

1. Referenced to VSS
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify-write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh.

Fig. 2 – t_{RAC} vs. t_{RCD}

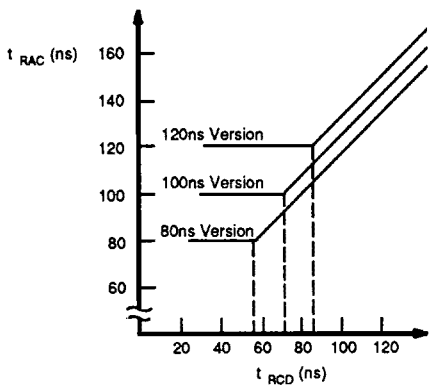
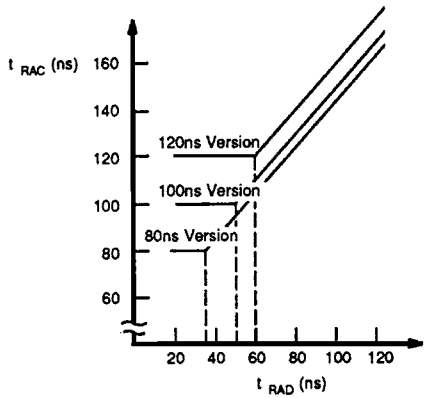


Fig. 3 – t_{RAC} vs. t_{RAD}



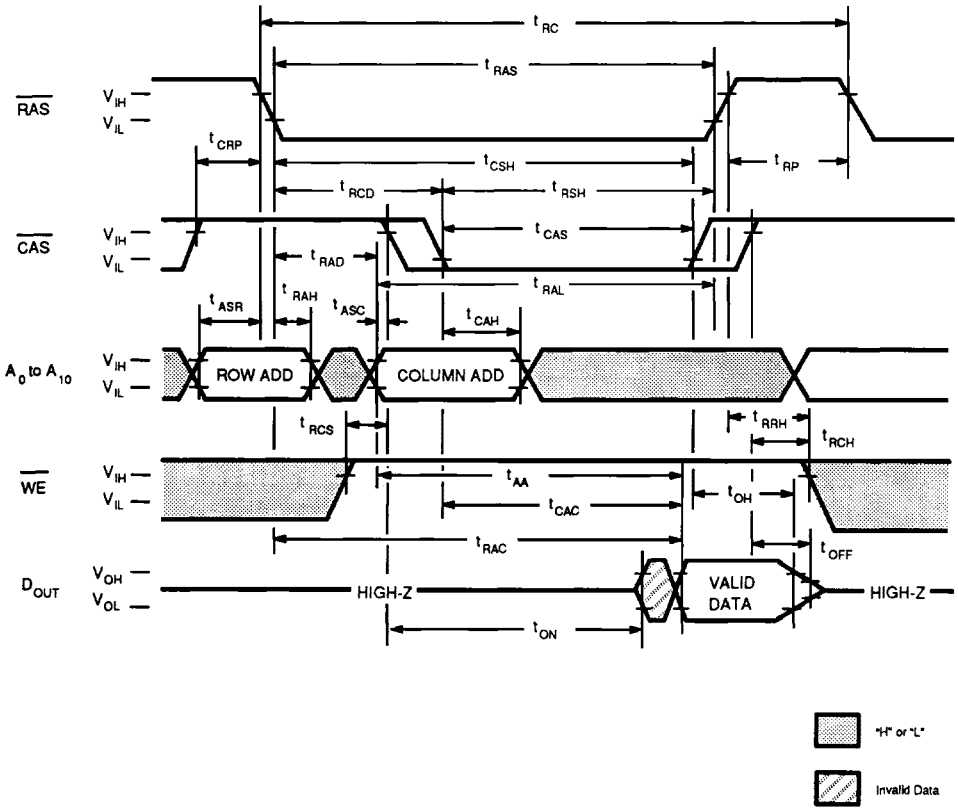
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	H	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Nibble Mode.

Fig. 4 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

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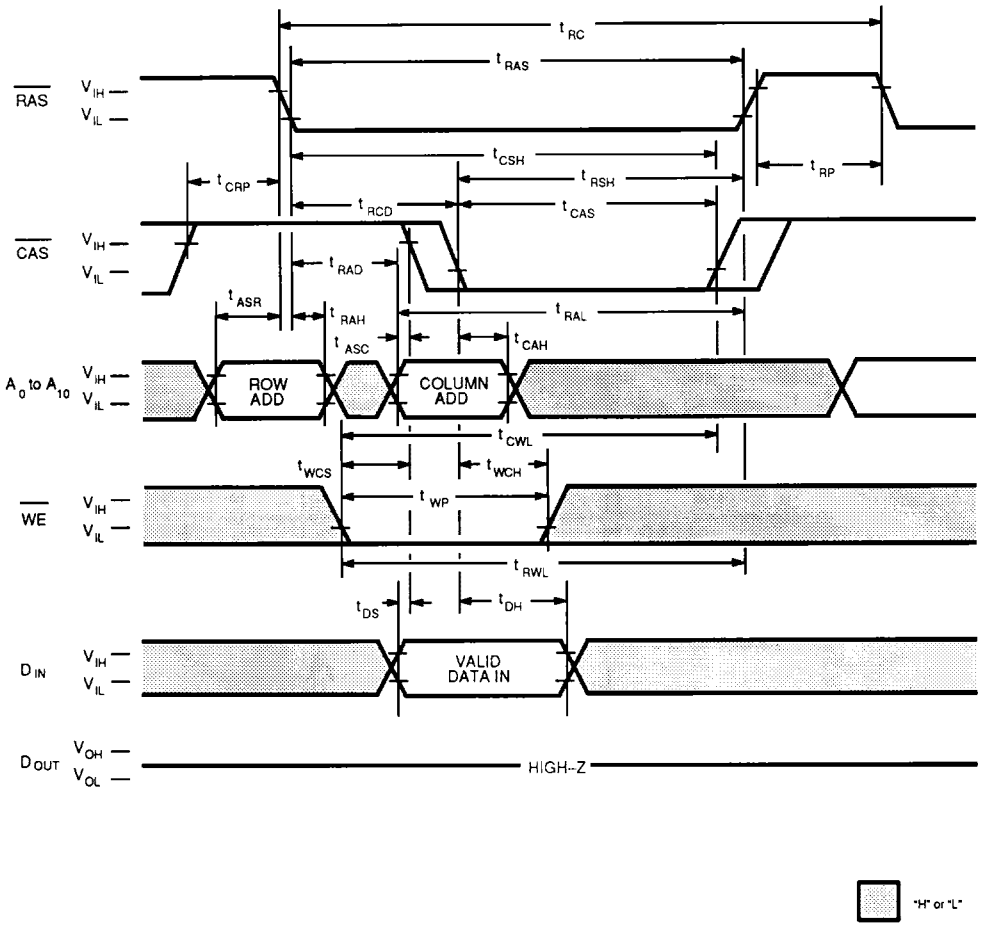
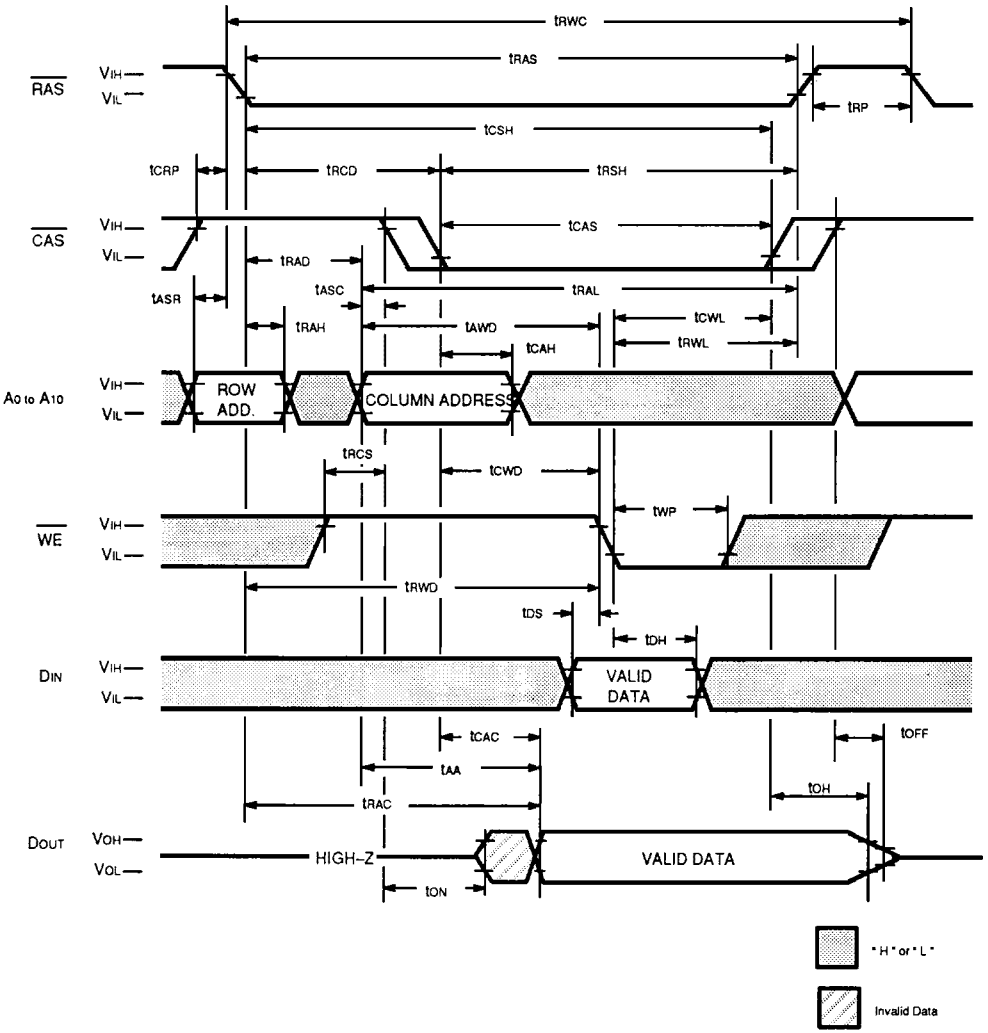
Fig. 5 — WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

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Fig. 7 – NIBBLE MODE READ CYCLE

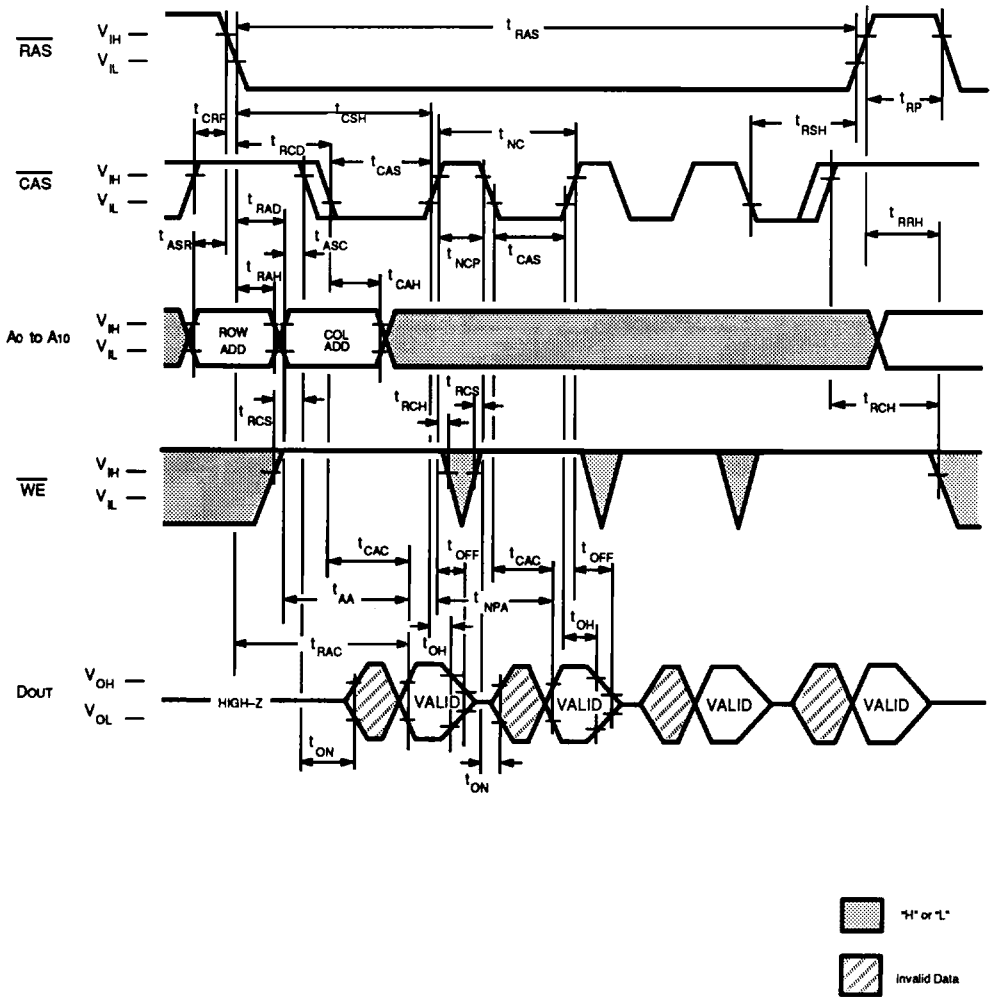

Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)

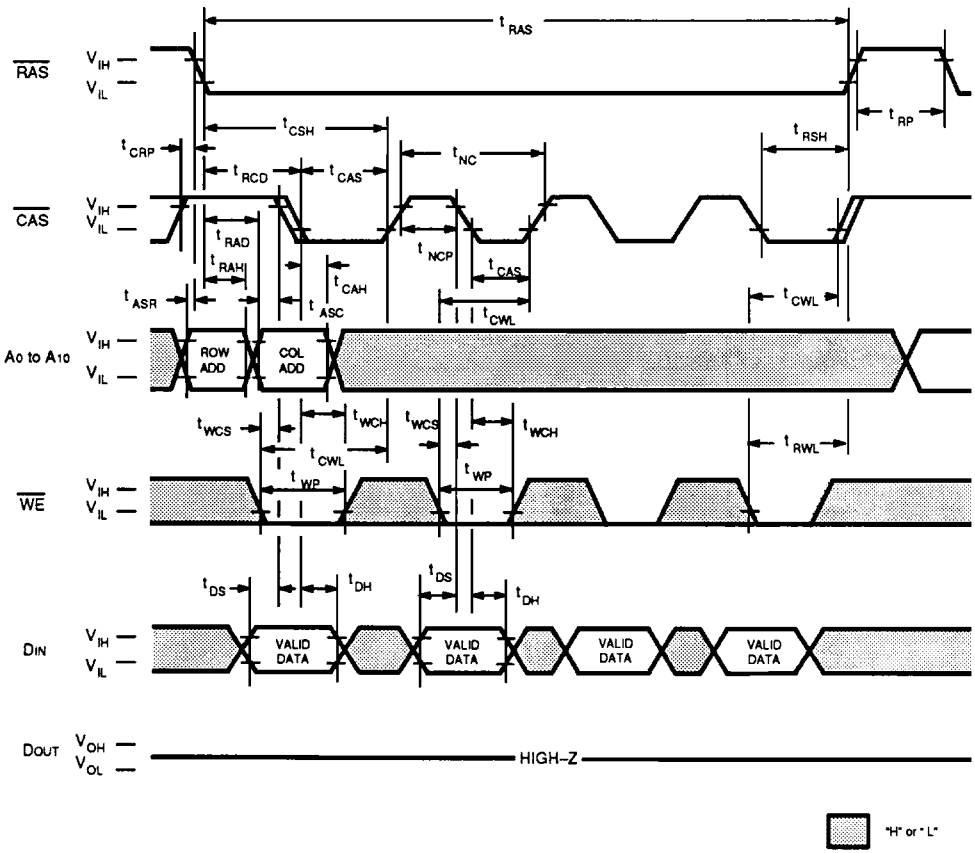

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Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

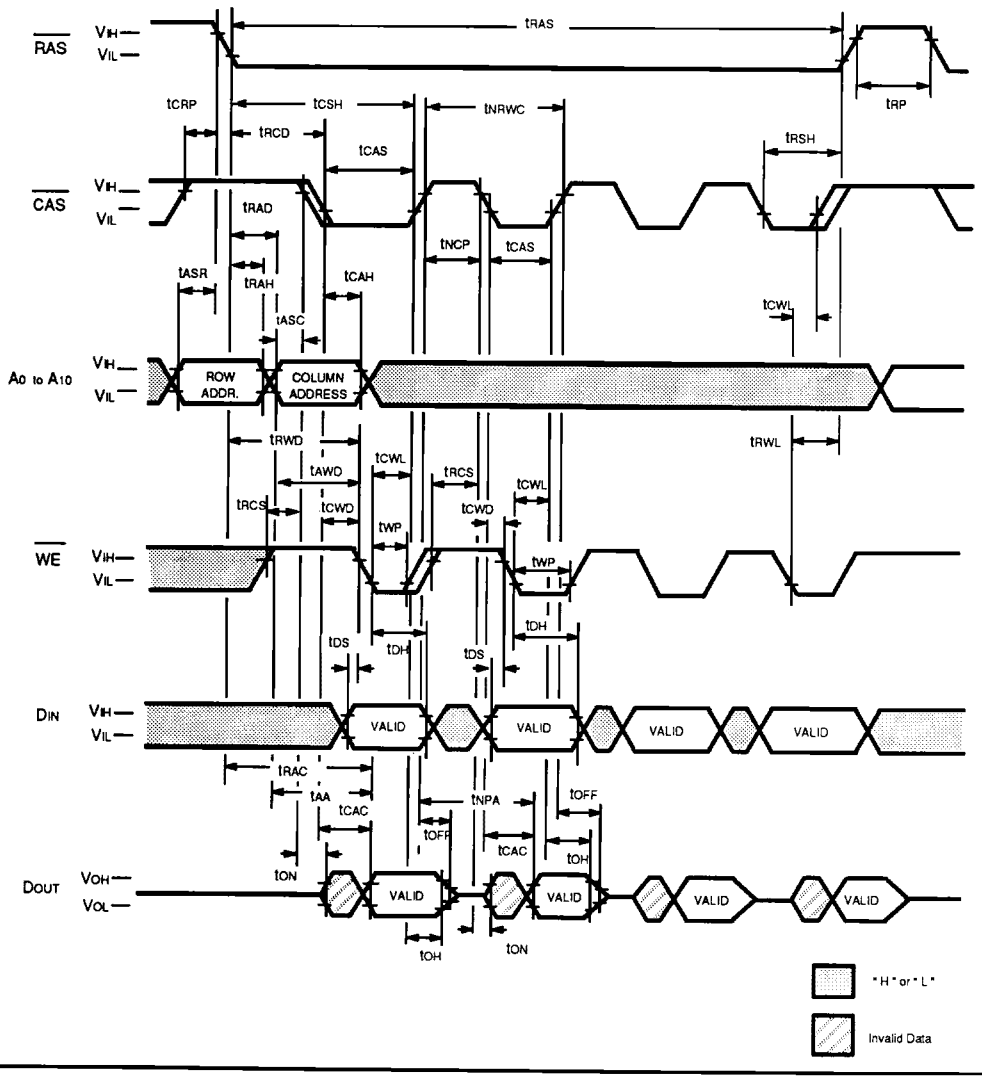
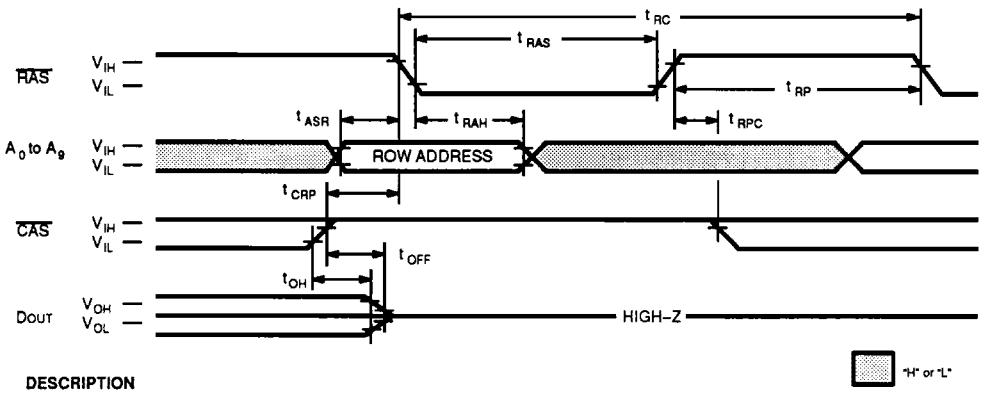


Fig. 10 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$, DIN, A10 = "H" or "L")

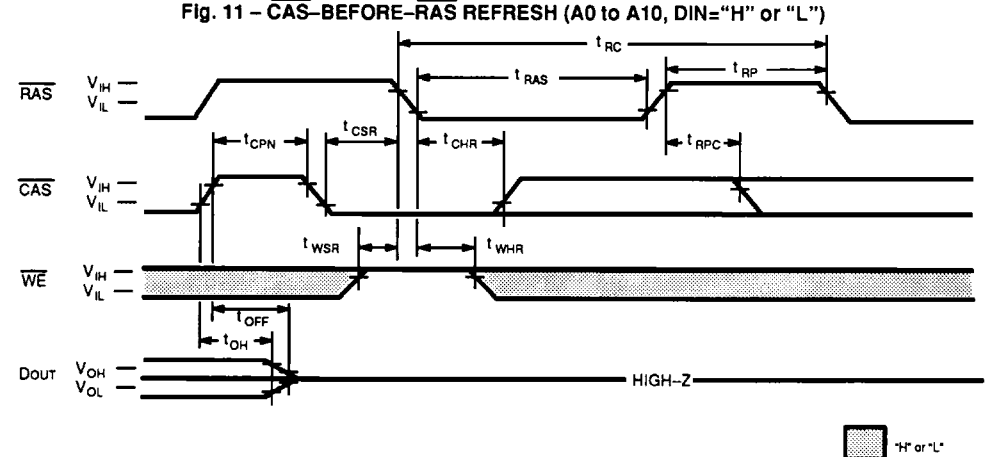


DESCRIPTION

The refresh of DRAM is executed by normal read, write or read–modify–write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 16.4ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re–written to the cell. The MB814100 has three types of refresh modes, $\overline{RAS}$–only refresh, $\overline{CAS}$–before–$\overline{RAS}$ refresh, and Hidden refresh.

The $\overline{RAS}$ only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, the DOUT pin is kept in a high impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (A0 to A10, DIN="H" or "L")



DESCRIPTION

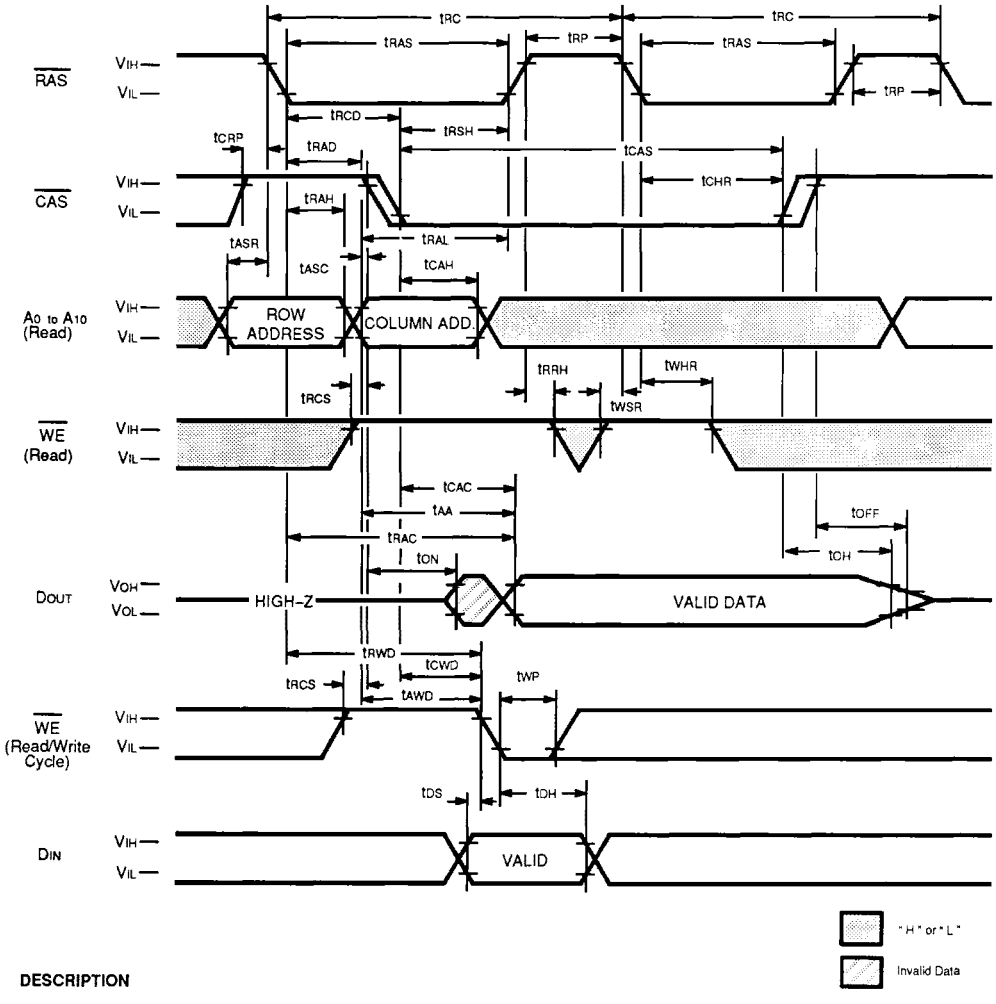
The $\overline{CAS}$–before–$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB814100 executes $\overline{CAS}$–before–$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" in order not to enter "test mode" to be specified later.

2

2

Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

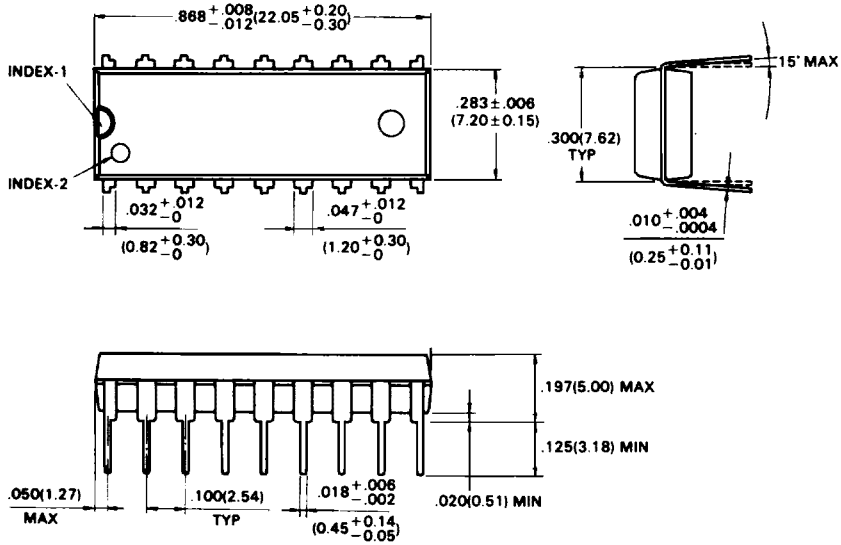
The hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$–before–$\overline{RAS}$ refresh.
$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" for the secound time in order not to enter "test mode" to be specified later.

PACKAGE DIMENSIONS

(Suffix : –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)



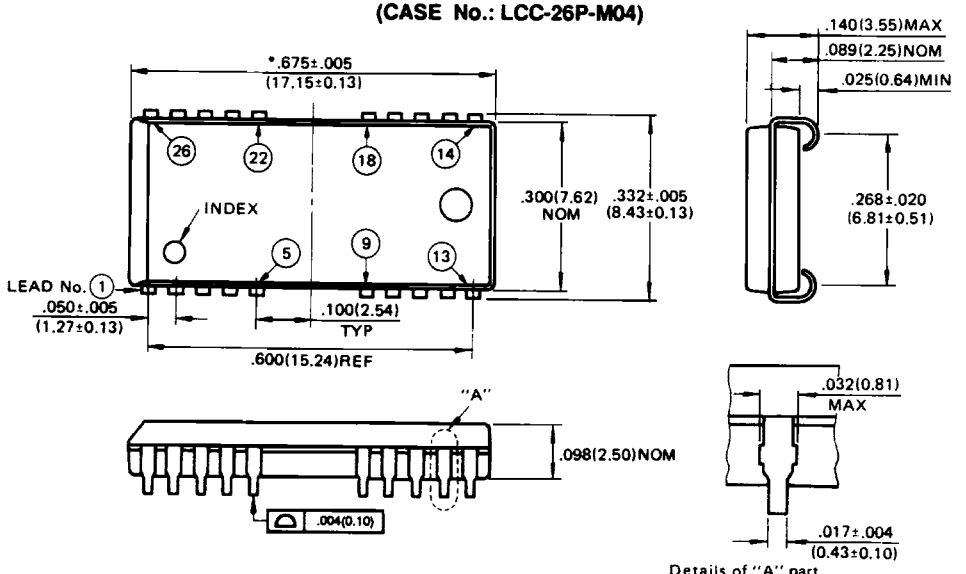
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)

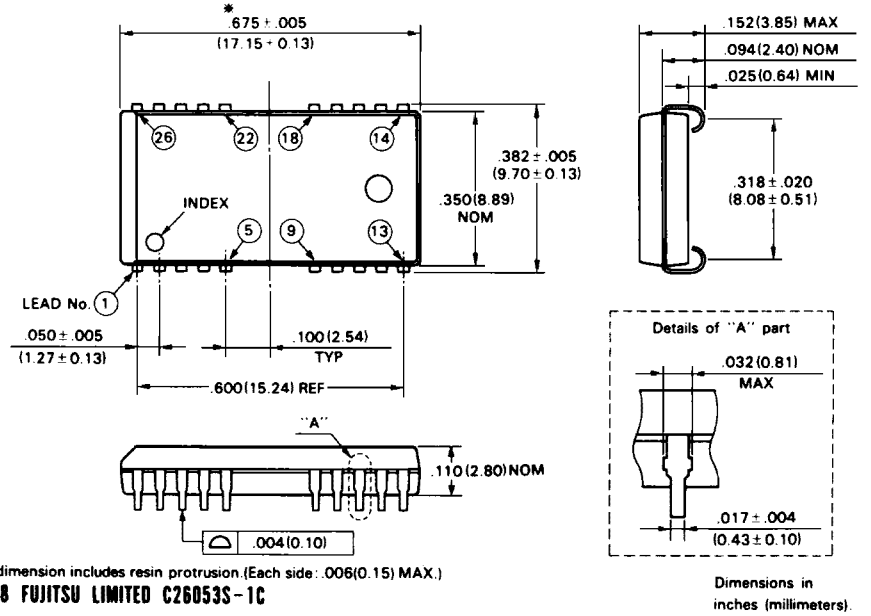


NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)



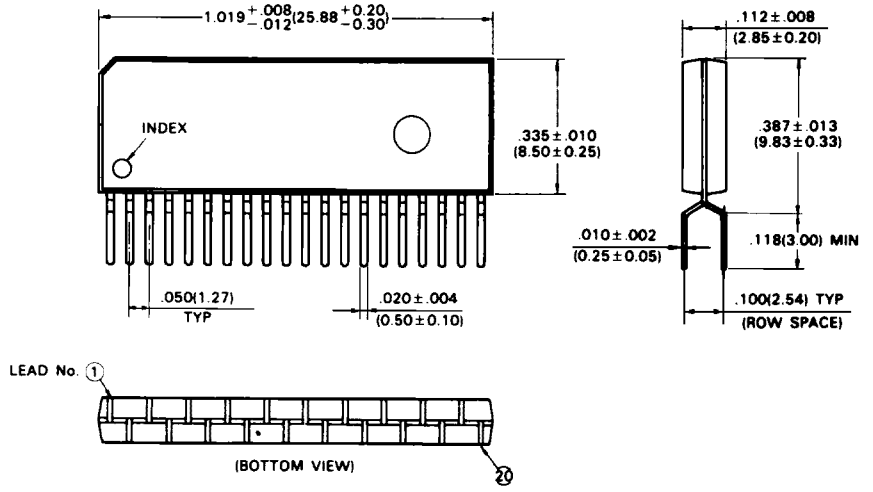
2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in inches (millimeters)