010226

Am93L41

Low-Power Four Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics

- 125 mw typical power dissipation.
- Typical add time for 4 bits of only 48 ns.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Provides all 16 possible logic operations of two variables typically in 42 ns.

FUNCTIONAL DESCRIPTION

The Am93L41 is a 4-bit high-speed parallel arithmetic logic unit (ALU)/digital function generator. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

An open collector A = B output is provided so that equivalence of two parallel words can be made by connecting A = B outputs of several ALU's together.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by providing carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. These carry signals can be used as inputs to the Am9342 look-ahead carry generator to form long word length high speed parallel arithmetic logic units.

For systems where ultra high speed is not required, the carry output signal (C_{n+4}) can be used to provide ripple block arithmetic operations. The ALU can be used with either Active HIGH or Active LOW inputs and can be expanded with the Am9342 look-ahead carry generator in either mode. The interconnection patterns are identical for both cases.

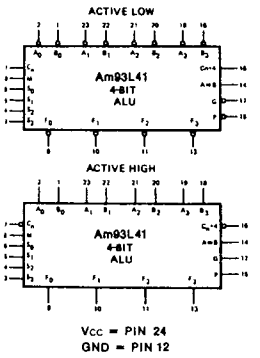
LOADING RULES

In Unit Loads (Notes)

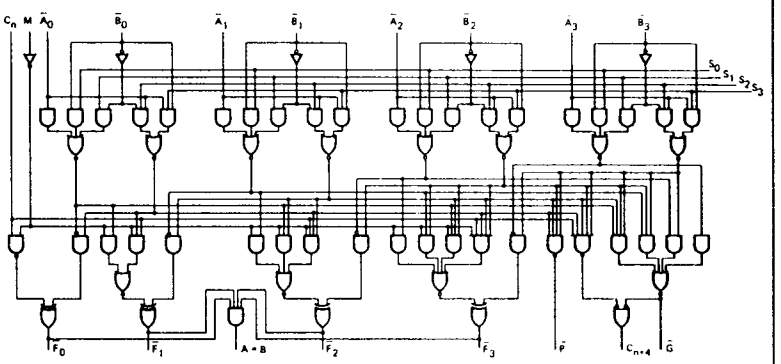
	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
M	0.5	0.25	1.0	1.0
all $\overline{A}$, all $\overline{B}$	1.5	0.75	3.0	3.0
S_0, S_1, S_2, S_3	2.0	1.0	4.0	4.0
C_n	2.5	1.25	5.0	5.0
Output Drive	HIGH	LOW	HIGH	LOW
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$, $\overline{G}$, $\overline{P}$, C_{n+4}	10	3	20	12
A = B	O/C	3	O/C	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



LOGIC DIAGRAM



Am93L41 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
24-Pin Molded DIP	0°C to +75°C	Am93L4159C
24-Pin Hermetic DIP	0°C to +75°C	U6N93L4159X
24-Pin Hermetic DIP	−55°C to +125°C	U6N93L4151X
24-Pin Hermetic Flat Pak	−55°C to +125°C	U4M93L4151X
Dice	Note	UXX93L41XXD

Revised Ordering Information See Section 9

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage

ELECTRIC HARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L4159X 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L4151X T_A −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−4.5	−10	−15	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		25	40	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C,

Parameter	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		18	36	54	ns
t_{pd-}				12	23	35	
t_{pd+}	C_n	any $\overline{F}$ (Note 3)	M = 0 V (SUM or DIFF mode)	16	31	47	ns
t_{pd-}				12	34	36	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	16	31	47	ns
t_{pd-}				12	23	35	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	18	35	53	ns
t_{pd-}				13	26	39	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	18	35	53	ns
t_{pd-}				13	26	39	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	19	37	56	ns
t_{pd-}				17	34	51	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	24	48	72	ns
t_{pd-}				24	47	71	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	27	53	80	ns
t_{pd-}				27	52	79	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (LOGIC mode)	19	38	57	ns
t_{pd-}				23	46	69	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	20	40	60	ns
t_{pd-}				22	44	66	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	22	44	66	ns
t_{pd-}				25	49	74	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	A = B	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	27	53	80	ns
t_{pd-}				25	50	75	

Note 3: F_i output is worst case.

OPERATION TABLE

Control Inputs	Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_3 S_2 S_1 S_0	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L L L L	A minus 1	$\overline{A}$	A	$\overline{A}$
H L L L	AB minus 1	$\overline{AB}$	A + B	$\overline{A+B}$
L H L L	$A\overline{B}$ minus 1	$\overline{A}+B$	$A+\overline{B}$	$\overline{AB}$
H H L L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L L H L	A plus $[A+\overline{B}]$	$\overline{A}+\overline{B}$	A plus $A\overline{B}$	$\overline{AB}$
H L H L	AB plus $[A+\overline{B}]$	$\overline{B}$	$A\overline{B}$ plus $[A+B]$	$\overline{B}$
L H H L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$
H H H L	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L L L H	A plus $[A+B]$	$\overline{A}B$	A plus AB	$\overline{A}+B$
H L L H	A plus B	$A \oplus B$	A plus B	$\overline{A \oplus B}$
L H L H	$A\overline{B}$ plus $[A+B]$	B	AB plus $[A+\overline{B}]$	B
H H L H	$A+B$	$A+B$	AB minus 1	AB
L L H H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H L H H	A plus AB	$A\overline{B}$	A plus $[A+B]$	$A+\overline{B}$
L H H H	A plus $A\overline{B}$	AB	A plus $[A+\overline{B}]$	$A+B$
H H H H	A	A	A minus 1	A

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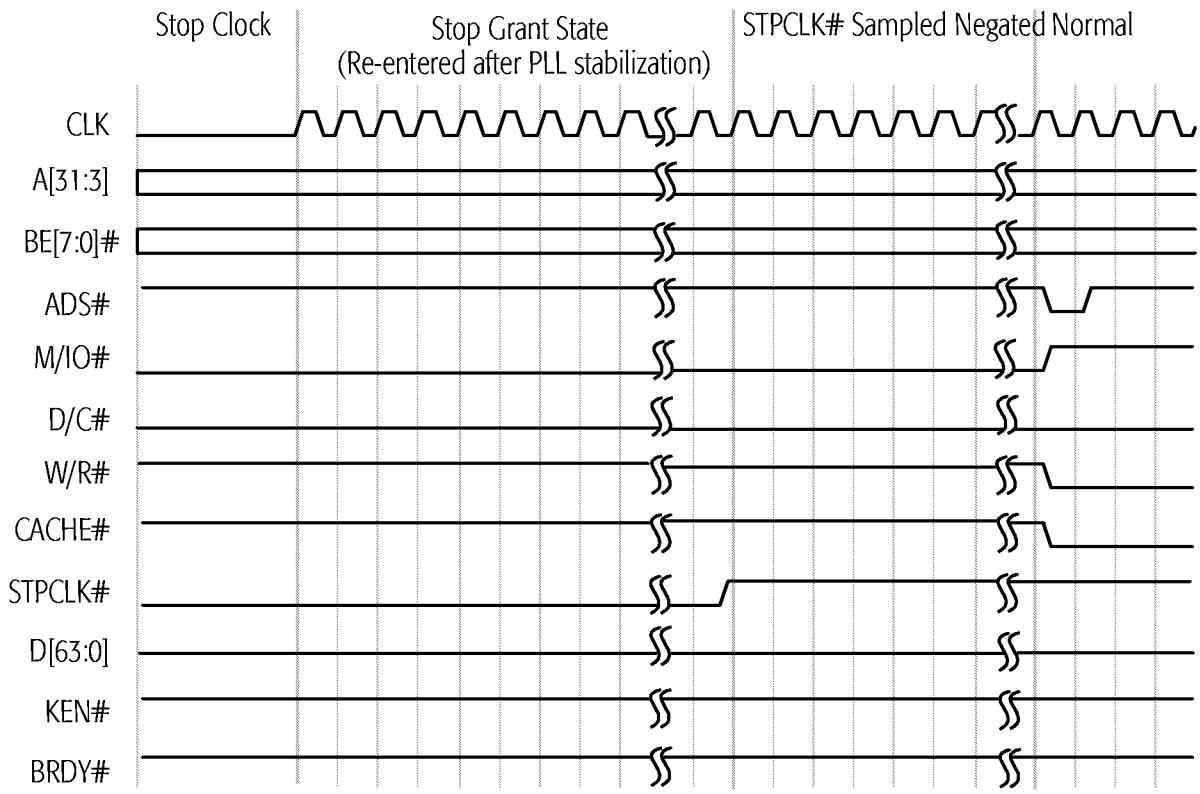

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

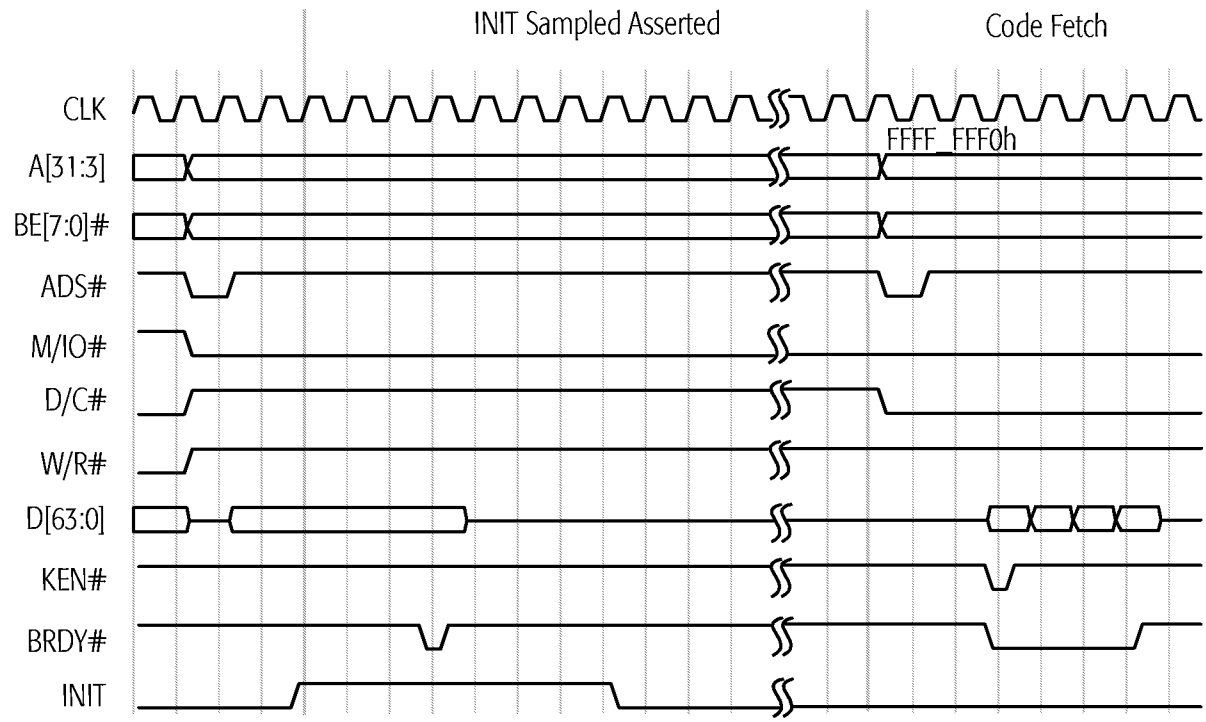

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.