SILICON STACKED GATE CMOS

32,768 WORD x 8 BIT CMOS ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

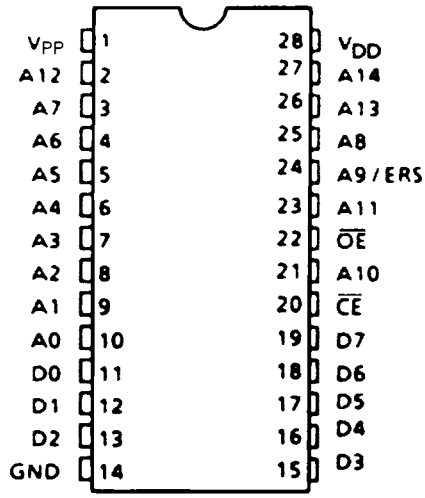
Description

The TC58257AP/AF is a 32,768 word x 8 bit electrically chip erasable programmable read only memory molded in a 28-pin plastic package. The TC58257AP/AF's access times are 200ns/250ns and it has a low standby mode which reduces the power dissipation without increasing access time. The electrical characteristics are the same as for the TC57256AD UV EPROM. Programming is achieved by using a high speed programming mode. The TC58257AP/AF has a chip erase mode which erases all bits at the same time.

Features

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Access time
  - TC58257AP/AF-20 200ns
  - TC58257AP/AF-25 250ns
- Low power dissipation
  - Active : 30mA/5MHz
  - Standby : 100μA
- Fully static operation
- High speed programming mode
- Electrical chip erasing mode
- Inputs and outputs TTL compatible
- Pin compatible with TC53257P, TC57256D/AD, and TC54256P/AP/AF
- Package
  - TC58257AP : DIP28-P-600
  - TC58257AF : SOP28-P-450

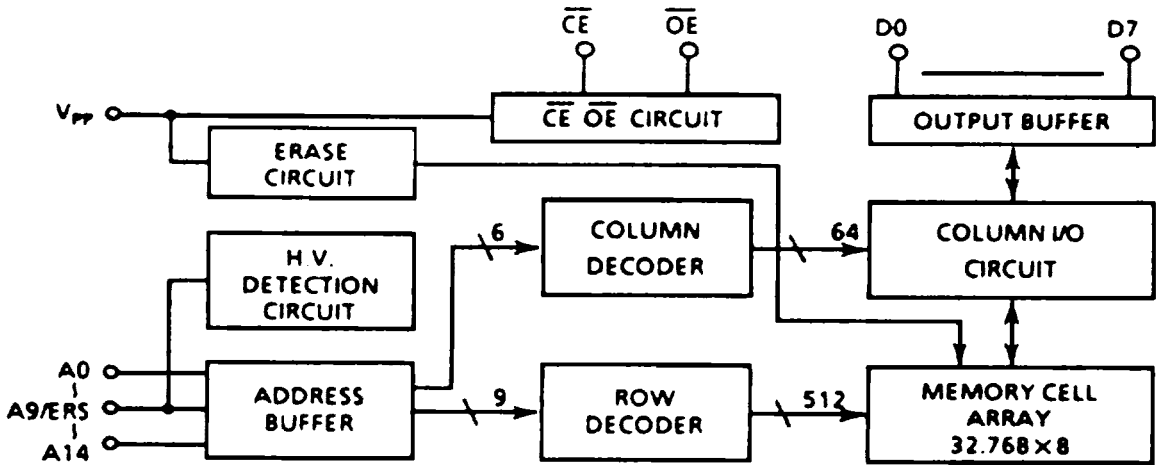
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
D0 ~ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
A9/ERS	Address and Erase Control Input
V_{PP}	Program and Erase Supply Voltage
V_{DD}	Power Supply Voltage
GND	Ground

Block Diagram



Operating Mode

MODE \ PIN	CE	OE	A9	V_{PP}	V_{DD}	A0 ~ A8 (10 ~ 14)	D0 ~ D7	POWER
Read	L	L	*	5V	5V	*	Data Output	Active
Output Deselect	*	H	*			*	High Impedance	
Standby	H	*	*			*	High Impedance	Standby
Program	L	H	*	12.75V or 12V	6.25V or 5V	*	Data Input	Active
Program Inhibit	H	*	*			*	High Impedance	
Program Verify	*	L	*			*	Data Out	
Chip Erase	L	H	12V	12.75V or 12V	5V	*	Don't Care	Active
Chip Erase Inhibit	H	*				*	High Impedance	

* = V_{IH} or V_{IL}

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V_{IN}	Input Voltage	-0.6 ~ 7.0	
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{DD} + 0.5	
P_D	Power Dissipation	1.0/0.6*	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	-10 ~ 70	
N_{EW}	Erase Write Endurance	100	Cycles

* SOP

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.50	5.00	5.50	
V_{PP}	Program Supply Voltage	V_{DD} - 0.6	V_{DD}	V_{DD} + 0.6	

DC Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4 ~ V_{DD}	–	–	±10	μA
I_{DDO}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA, f = 5MHz	–	–	30	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	1	
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V	–	–	100	μA
V_{OH}	Output High Voltage	I_{OH} = - 400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.10mA	–	–	0.4	
I_{PP1}	V_{PP} Current	V_{PP} = V_{DD} - 0.6 ~ V_{DD} + 0.6	–	–	±10	μA

AC Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%, V_{PP} = V_{DD}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	-20		-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	–	200	–	250	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}	–	70	–	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	0	60	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	0	60	0	90	
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	

AC Test Conditions

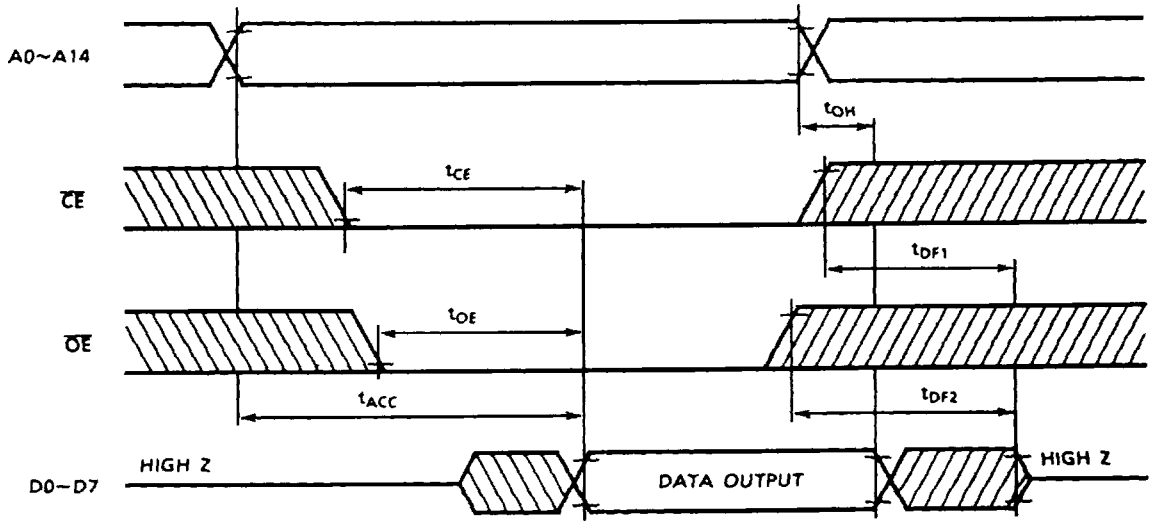
Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	12	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms (Read)



High Speed Programming Mode I

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	Program Supply Voltage	12.50	12.75	13.00	

DC Characteristics (Ta = -10 ~ 70°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	10	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 13.0V	–	–	50	

AC Programming Characteristics (Ta = -10 ~ 70°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	2	–	–	
t_{VS}	V_{PP} Setup Time	–	2	–	–	
t_{PW}	Program Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	95	100	105	
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	150	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	–	–	130	

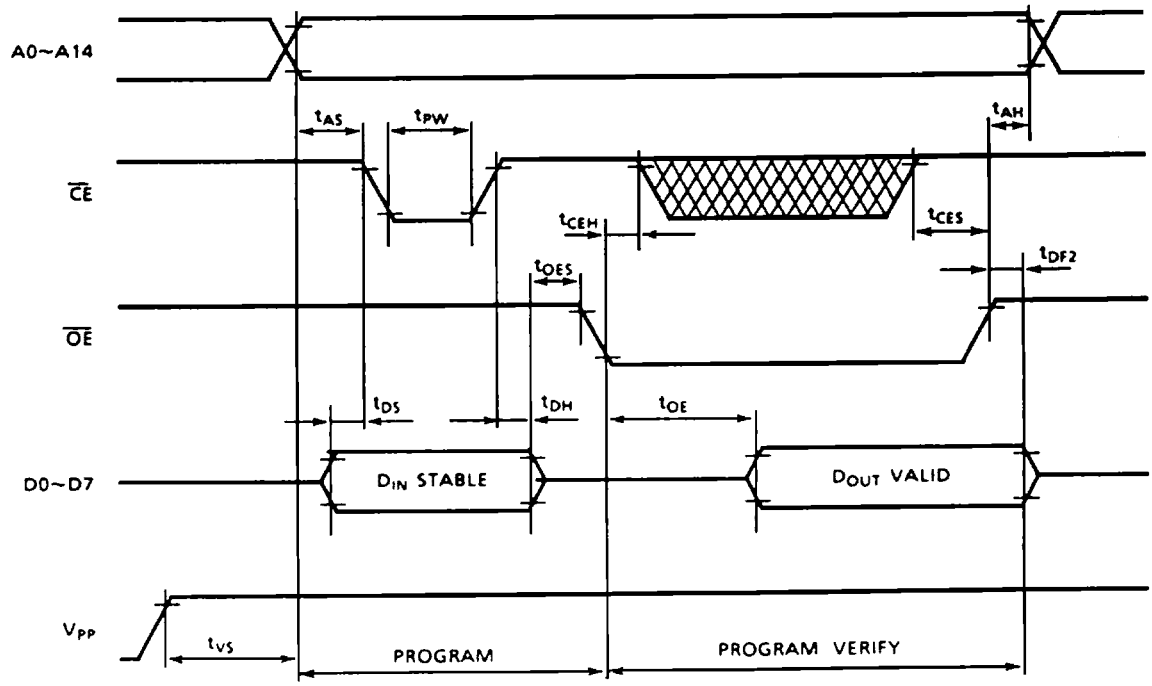
AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Timing Waveforms (Program)

High Speed Programming Mode I

(V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.75V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

High Speed Programming Mode II

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	
V_{PP}	Program Supply Voltage	11.50	12.0	12.5	

DC Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5.0V±10%, V_{PP} = 12.0V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	10	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 12.5V	–	–	50	

AC Programming Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%, V_{PP} = 12.0V±0.5V)

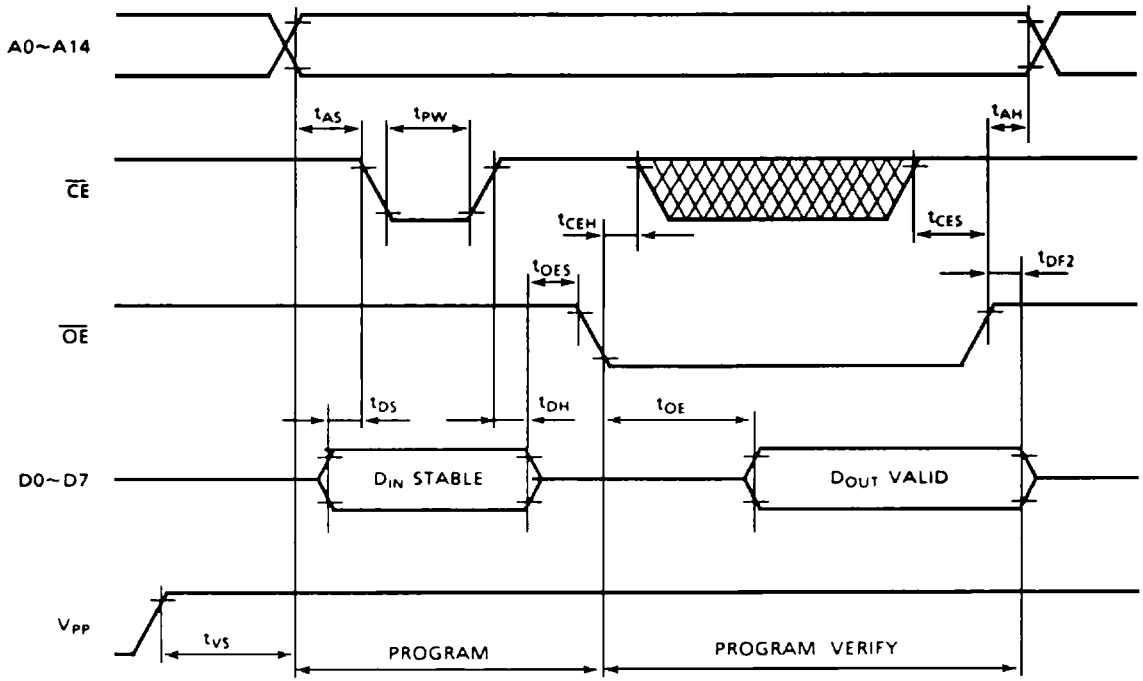
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	2	–	–	
t_{VS}	V_{PP} Setup Time	–	2	–	–	
t_{PW}	Program Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1.0	26.25	
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	150	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	–	–	130	

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

Timing Waveforms (Program)

High Speed Programming Mode II

(V_{DD} = 5V±10%, V_{PP} = 12.0V±0.5V)



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.0V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Chip Erase Mode I

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	
V_{PP}	Program Supply Voltage	12.50	12.75	13.00	
V_{IHH}	Input High Voltage H	11.5	12.0	12.5	

DC Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	±10	μA
I_{LIE}	A9/ERS Input Current	A9/ERS = 0 ~ V_{IHH}	–	–	±100	
I_{DD}	V_{DD} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 13.0V	–	–	50	

AC Erasing Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%, V_{PP} = 12.75V±0.25V)

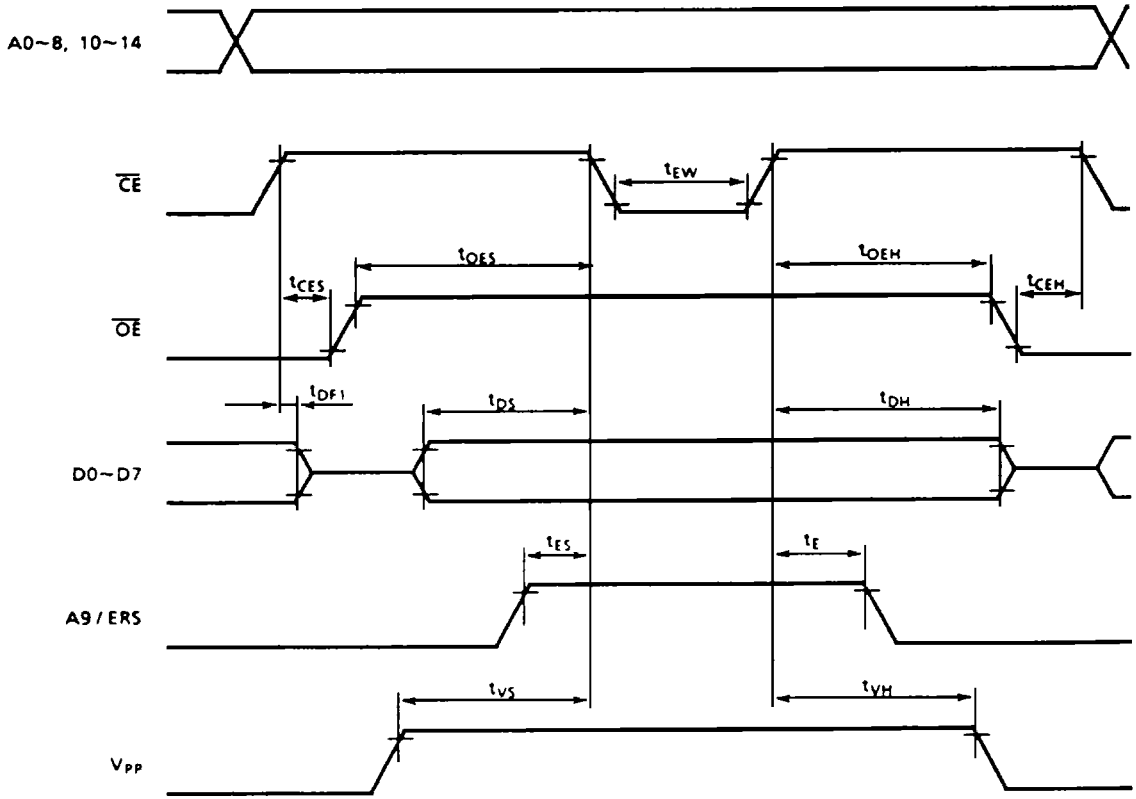
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{OEH}	$\overline{OE}$ Hold Time	–	500	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	500	–	–	
t_{VS}	V_{PP} Setup Time	–	2	–	–	
t_{VH}	V_{PP} Hold Time	–	500	–	–	
t_{ES}	A9/ERS Setup Time	–	2	–	–	
t_{EH}	A9/ERS Hold Time	–	2	–	–	
t_{EW}	Erase Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, A9 = V_{IHH}	950	1000	1050	ms
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	–	–	150	ns

Input Pulse Rise and Fall Time : 10ns Max.
Input Pulse Levels : 0.45V ~ 2.4V

Timing Waveforms (Erase)

Chip Erase Mode I

(V_{DD} = 5V±10%, V_{PP} = 12.75V±0.25V)



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.75V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for the erase operation. Voltages over 14V should not be applied to the V_{PP} terminal. When the voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Chip Erase Mode II

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	
V_{PP}	Program Supply Voltage	11.5	12.0	12.5	
V_{IHH}	Input High Voltage H	11.5	12.0	12.5	

DC Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	±10	μA
I_{LIE}	A9/ERS Input Current	A9/ERS = 0 ~ V_{IHH}	–	–	±100	
I_{DD}	V_{DD} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 12.5V	–	–	50	

AC Erasing Characteristics (Ta = -10 ~ 70°C, V_{DD} = 5V±10%, V_{PP} = 12.0V±0.5V)

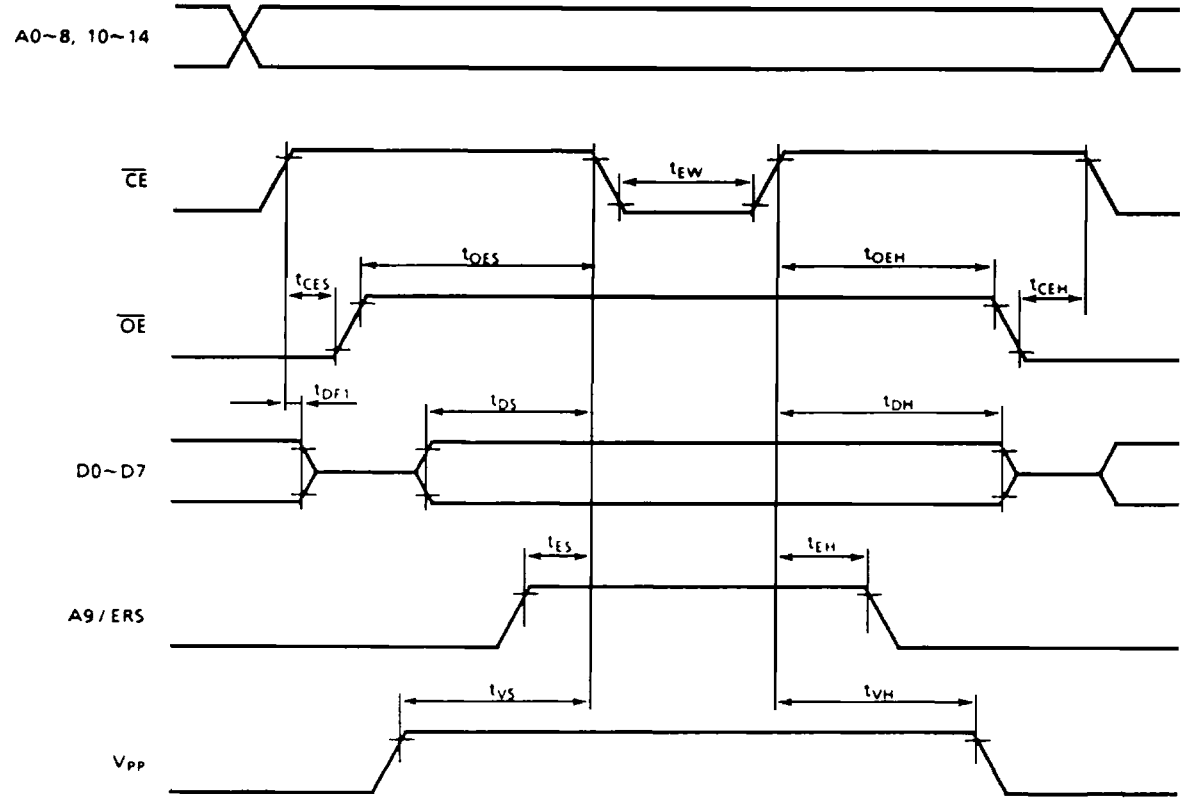
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{OEH}	$\overline{OE}$ Hold Time	–	500	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	500	–	–	
t_{VS}	V_{PP} Setup Time	–	2	–	–	
t_{VH}	V_{PP} Hold Time	–	500	–	–	
t_{ES}	A9/ERS Setup Time	–	2	–	–	
t_{EH}	A9/ERS Hold Time	–	2	–	–	
t_{EW}	Erase Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, A9 = V_{IHH}	1950	2000	2050	ms
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	–	–	150	ns

Input Pulse Rise and Fall Time : 10ns Max.
Input Pulse Levels : 0.45V ~ 2.4V

Timing Waveforms (Erase)

Chip Erase Mode II

(V_{DD} = 5V±10%, V_{PP} = 12.0V±0.5V)



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.0V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for the erase operation. Voltages over 14V should not be applied to the V_{PP} terminal. When the voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Operation Information

The TC58257AP/AF's eight operating modes are listed in the following table.
Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE \ PIN		$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{DD}	D0 ~ D7	POWER
Read Operation	Read	L	L	*	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
Program Operation	Program	L	H	*	1) 12.75V 2) 12V	1) 6.25V 2) 5V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
	Program Verify	*	L	*			Data Out	
Erase Operation	Erase	L	H	12V	1) 12.75V 2) 12V	5V	Don't Care	Active
	Erase Inhibit	H	*				High Impedance	

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

1) High Speed Program/Erase Mode I
2) High Speed Program/Erase Mode II

Standby Mode

The TC58257AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a MOS high level voltage (V_{DD}) to the $\overline{CE}$ input, the TC58257AP/AF is placed in the standby mode which reduces the operating current to 100μA and puts the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Program Mode

When the TC58257AP/AF is initially received by customers, all bits of the device are in the "1" state, which is the erased state. Therefore, the object of the program operation is to introduce "0" data into the desired bit locations.

The TC58257AP/AF is in the programming mode when V_{PP} = 12.75V (12.0V), $\overline{CE}$ = V_{IL}, and $\overline{OE}$ = V_{IH}. The TC58257AP/AF can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when $\overline{OE}$ = V_{IL}.

Program Inhibit Mode

When the programming voltage (12.75V or 12.0V) is applied to the V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC58257AP/AF from being programmed. The programming of two or more TC58257AP/AFs in parallel with different data is easily accomplished. All inputs except for $\overline{CE}$ may be commonly connected, then a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only while a TTL high level signal is applied to the $\overline{CE}$ of the other devices.

High Speed Programming Mode I

The device is set up in high speed programming mode I when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{DD} = 6.25V. Programming is achieved by applying a single 100μs TTL low level pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using the program verify mode. If the programmed data is not correct, another program pulse of 100μs is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{DD} = V_{PP} = 5V.

High Speed Programming Mode II

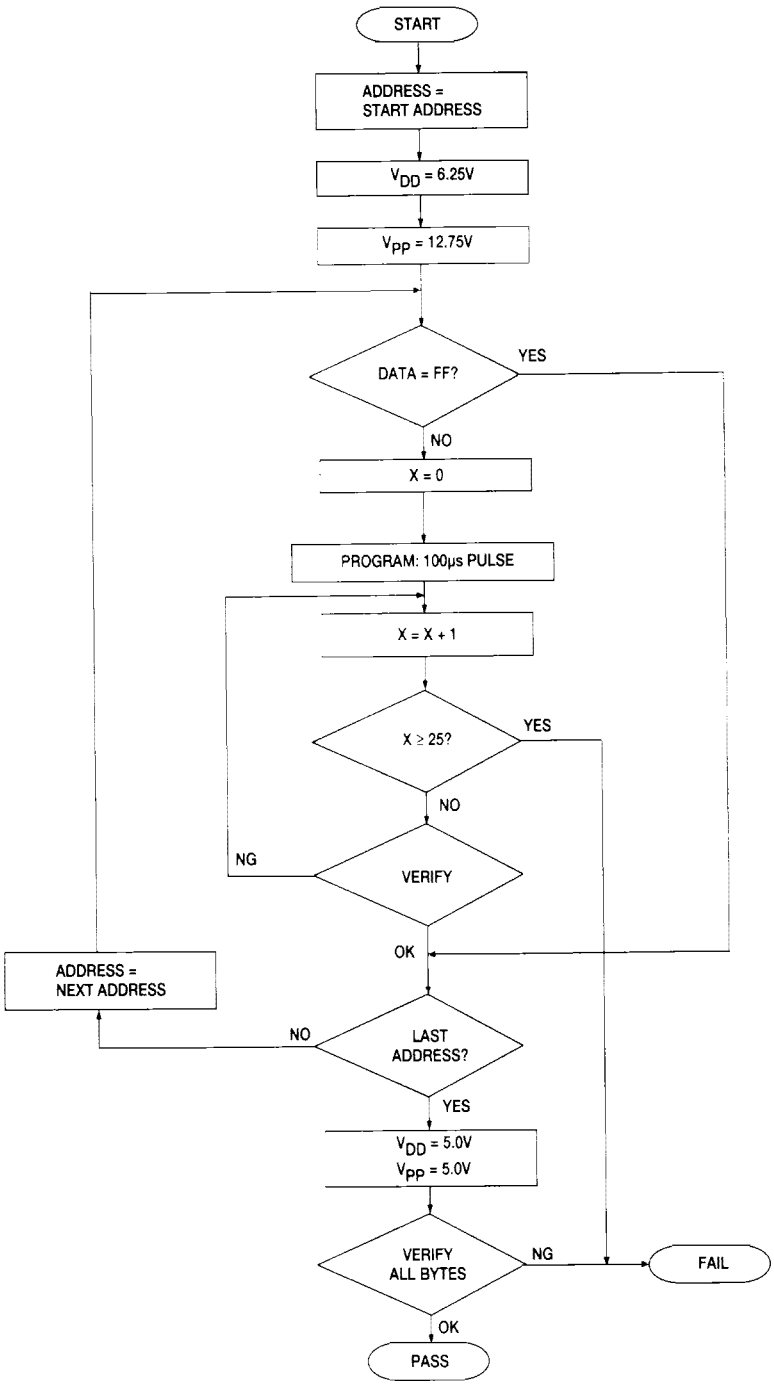
The device is set up in high speed programming mode II when the programming voltage (+12.0V) is applied to the V_{PP} terminal with V_{DD} = 5.0V. Programming is achieved by applying a single 1ms TTL low level pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using the program verify mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

After correctly programming the selected address, an overprogram pulse with the same width as that needed for initial programming should be applied.

When programming has been completed, the data in all addresses should be verified with V_{DD} = V_{PP} = 5V.

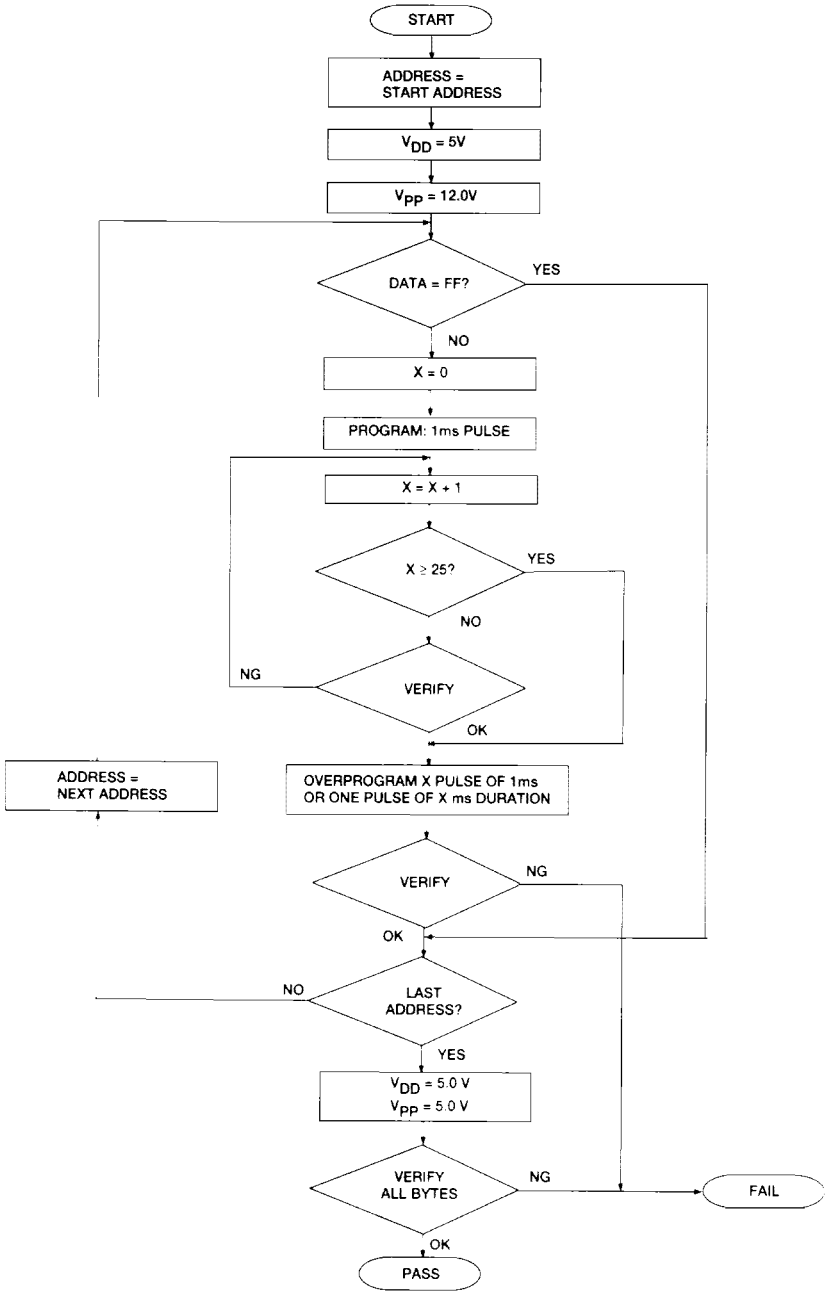
High Speed Programming Mode I

Flow Chart



High Speed Programming Mode II

Flow Chart



Electric Signature Mode

The electric signature mode allows one to read out a code from the TC58257AP/AF which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC58257AP/AF by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit being the MSB (D7). The following table shows the electric signature of the TC58257AP/AF.

PINS / SIGNATURE	A0 (10)	D7 (19)	D6 (18)	D5 (17)	D4 (16)	D3 (15)	D2 (13)	D1 (12)	D0 (11)	HEX. DATA
Manufacturer Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	1	0	0	1	0	0	A4

Notes: A9 = 12V±0.5V
A1 ~ A8, A10 ~ A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}