November 1989
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FUJITSU

DATA SHEET

MB81C4258-70/-80/-10/-12

CMOS 1,048,576 BIT STATIC COLUMN MODE DYNAMIC RAM

CMOS 262,144 x 4 BIT Static Column Mode Dynamic RAM

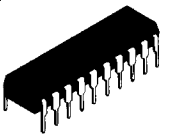
PRELIMINARY

The Fujitsu MB81C4258 is CMOS fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4258 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technologymakes the MB81C4258 High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

The specification is applied to "BC" version revised with intent to realized faster access time. So faster speed version (70ns and 80ns) are available on this chip.



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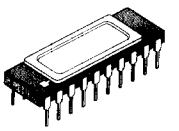

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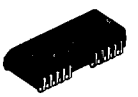

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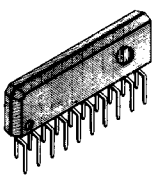

ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C4258 -70	MB81C4258 -80	MB81C4258 -10	MB81C4258 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Static Column Mode Cycle Time	48ns min.	50ns min.	55ns min.	65ns min.
Low Power Dissipation	413mW max.	385mW max.	330mW max.	275mW max.
• Operating current • Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static Column Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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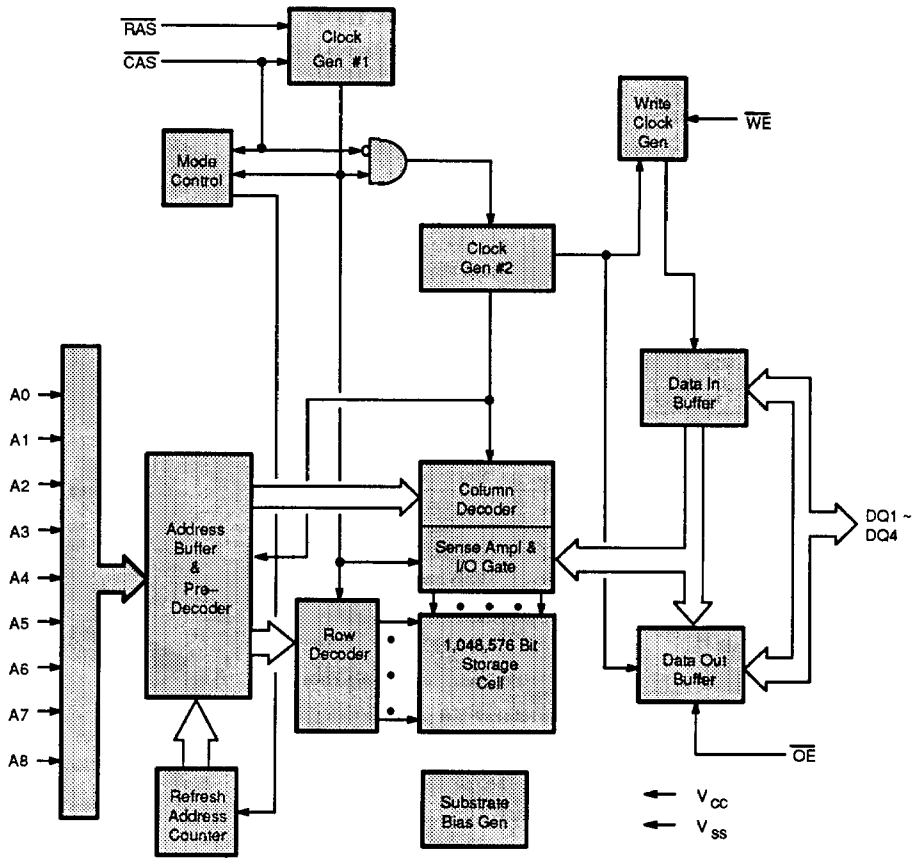
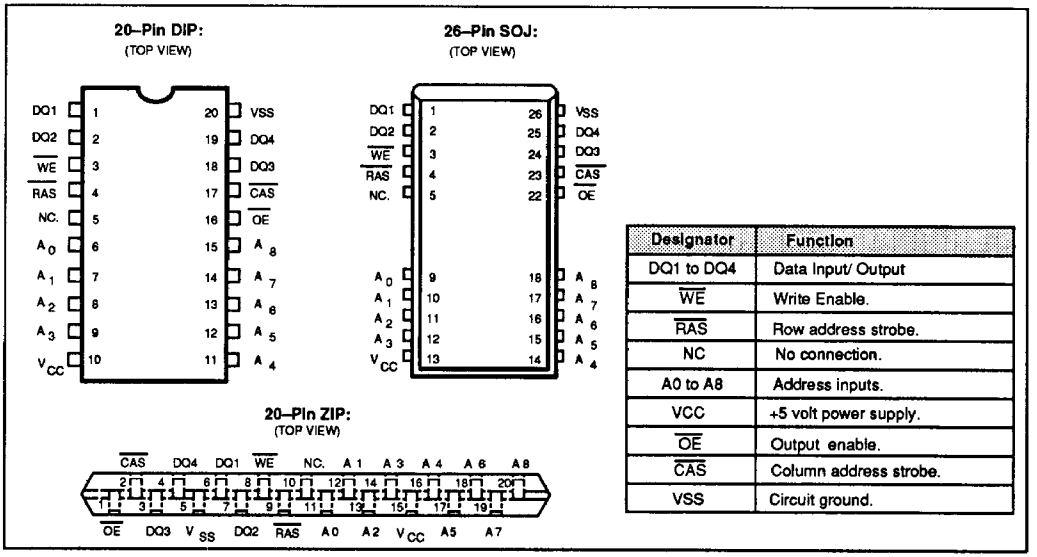
Fig. 1 – MB81C4258 DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	−1.0	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

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WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

STATIC COLUMN MODE OF OPERATION

The static column mode operation allows continuous read, write, or read–modify–write cycle within a row by applying new column address. In the static column mode, $\overline{RAS}$ can be kept low throughout static column mode operation. The following four cycles are allowed in the static column mode.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = −5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	−10	—	10	µA
Output leakage current		$I_{DQ(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	−10	—	10	µA
Operating current (Average Power supply Current) 2	MB81C4258-70	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C4258-80					70	
	MB81C4258-10					60	
	MB81C4258-12					50	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} −0.2V			1.0	
Refresh current #1 (Average power supply current) 2	MB81C4258-70	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	70	mA
	MB81C4258-80					65	
	MB81C4258-10					55	
	MB81C4258-12					45	
Static Column Mode current 2	MB81C4258-70	I_{CC4}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IL} t_{SC} = min	—	—	37	mA
	MB81C4258-80					35	
	MB81C4258-10					30	
	MB81C4258-12					23	
Refresh current #2 (Average power supply current) 2	MB81C4258-70	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C4258-80					65	
	MB81C4258-10					55	
	MB81C4258-12					45	

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4258-70		MB81C4258-80		MB81C4258-10		MB81C4258-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	197	—	212	—	240	—	275	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time	23	t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)		t_{CPN}	15	—	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time	7	t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time	7	t_{CAH}	20	—	20	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Hold Time		t_{WCH}	20	—	20	—	20	—	25	—	ns
29	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
30	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
31	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
32	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
33	DIN Hold Time		t_{DH}	20	—	20	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4258-70		MB81C4258-80		MB81C4258-10		MB81C4258-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
34	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
35	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before–$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before–$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
37	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	22	—	25	—	30	ns
38	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	—	25	ns
39	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
40	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	15	t_{OEH}	0	—	0	—	0	—	0	—	ns
41	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	25	—	ns
42	DIN to $\overline{CAS}$ Delay Time	16	t_{DZC}	0	—	0	—	0	—	0	—	ns
43	DIN to $\overline{OE}$ Delay Time	16	t_{DZO}	0	—	0	—	0	—	0	—	ns
44	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Static Column Mode Read/Write Cycle Time		t_{SC}	48	—	50	—	55	—	65	—	ns
51	Static Column Mode Read–Modify–Write Cycle Time		t_{SRWC}	121	—	125	—	135	—	155	—	ns
52	Access Time Relative to Last Write	17	t_{ALW}	—	91	—	95	—	105	—	125	ns
53	Access Time from $\overline{WE}$ Precharge		t_{WPA}	—	25	—	25	—	30	—	35	ns
54	Output Hold Time for Column Address Change		t_{AOH}	10	—	10	—	10	—	10	—	ns
55	Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	18	t_{AHR}	15	—	15	—	15	—	15	—	ns
56	Last Write to Column Address Delay Time	19,20	t_{LWAD}	25	48	25	50	25	55	30	65	ns
57	Column Address Hold Time Referenced to Last Write		t_{AHLW}	91	—	95	—	105	—	125	—	ns
58	$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	70	—	80	—	100	—	120	—	ns
59	$\overline{WE}$ Inactive Time		t_{WI}	13	—	15	—	15	—	20	—	ns
60	Write Set Up Time for Output Disable	21	t_{WS}	0	—	0	—	0	—	0	—	ns
61	Write Hold Time for Output Disable	21	t_{WH}	0	—	0	—	0	—	0	—	ns
62	$\overline{OE}$ Hold Time Referenced to $\overline{RAS}$	22	t_{OEHR}	20	—	20	—	20	—	20	—	ns
63	$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$	22	t_{OEHC}	20	—	20	—	20	—	20	—	ns
64	Static Column Mode CAS Precharge Time		t_{CP}	15	—	15	—	15	—	15	—	ns
65	Write Command Hold Time Referenced to $\overline{RAS}$		t_{WHR}	5	—	5	—	5	—	5	—	ns

Notes:

1. Referenced to VSS
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that write cycle only.
8. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Assumes that t_{WCS} < t_{WCS} (min)
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
18. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
19. Operation within the t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, access time is controlled by t_{AA} .
20. t_{LWAD} (min) = t_{CAH} (min)+ t_T(t_T − 5ns).
21. t_{WS} and t_{WH} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state through entire cycle.
22. Either t_{OEHR} or t_{OEHC} is satisfied.
23. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh, $\overline{CAS}$ -before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

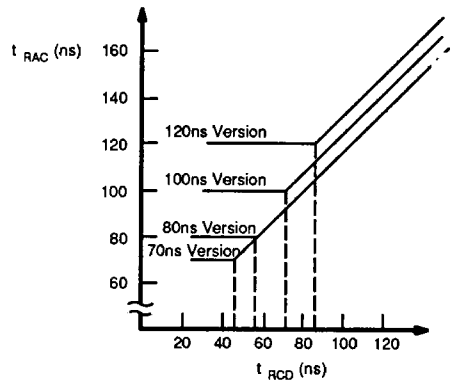
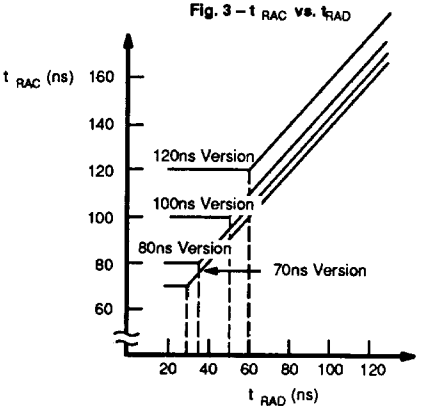


Fig. 3 – t_{RAC} vs. t_{RAD}



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FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	O	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	*1 High-Z	O	$t_{WS} \geq t_{WS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	L → H	Valid	Valid	Valid	Valid	O	
Static Column Mode Read Cycle	L	L	H	L	*2 Valid	Valid	—	Valid	X	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Static Column Mode Write Cycle	L	L	L	H	*2 Valid	Valid	Valid	*1 High-Z	X	
Static Column Mode Read–Modify–Write Cycle	L	L	H → L	L → H	*2 Valid	Valid	Valid	Valid	X	
Static Column Mode Mixed Cycle	L	L	L/H	L/H	*2 Valid	Valid	Valid	High-Z or Valid	X	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High-Z	O	
Hidden Refresh Cycle	H → L	L	X	L	—	—	—	Valid	O	Previous data is kept

Notes:

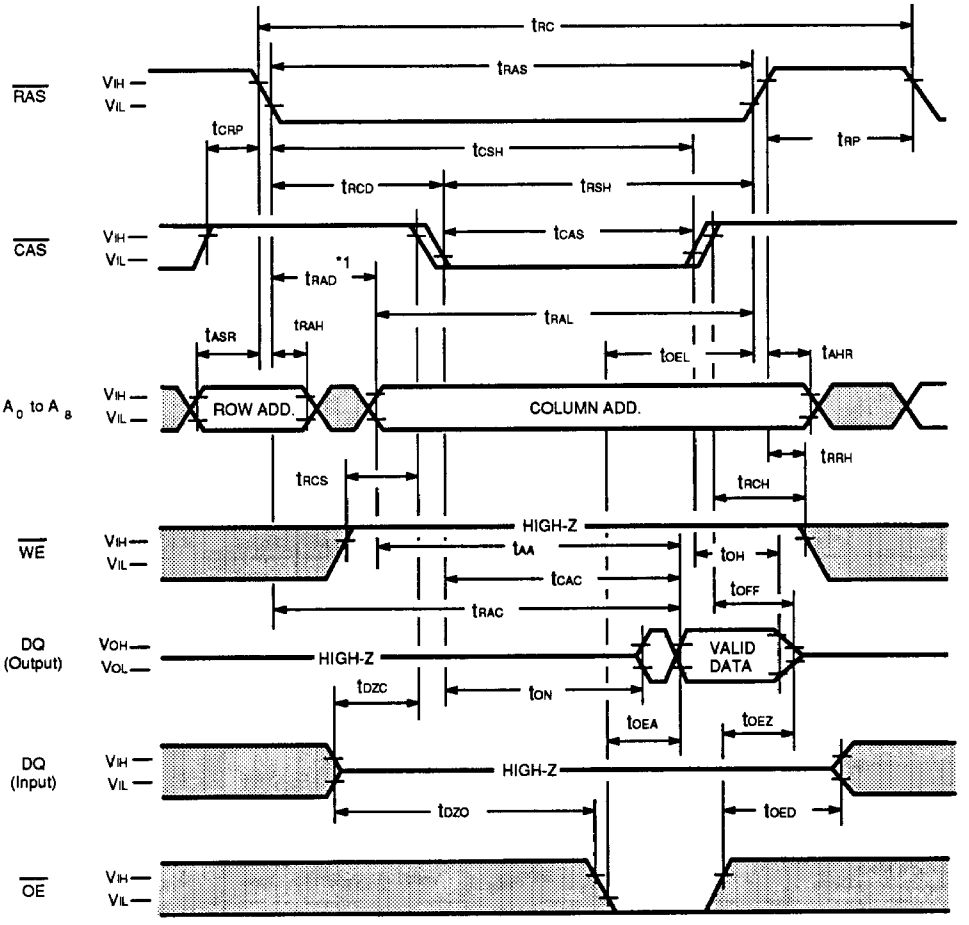
X : "H" or "L"

*1: If tWS < tWS (min) and tWH < tWH (min), the data output become invalid.

*2: After first cycle, row address is not necessary.

2

Fig. 4 – READ CYCLE



*1; If tRAD ≥ tRAD (max), access time is tCAC or tAA whichever occur later.

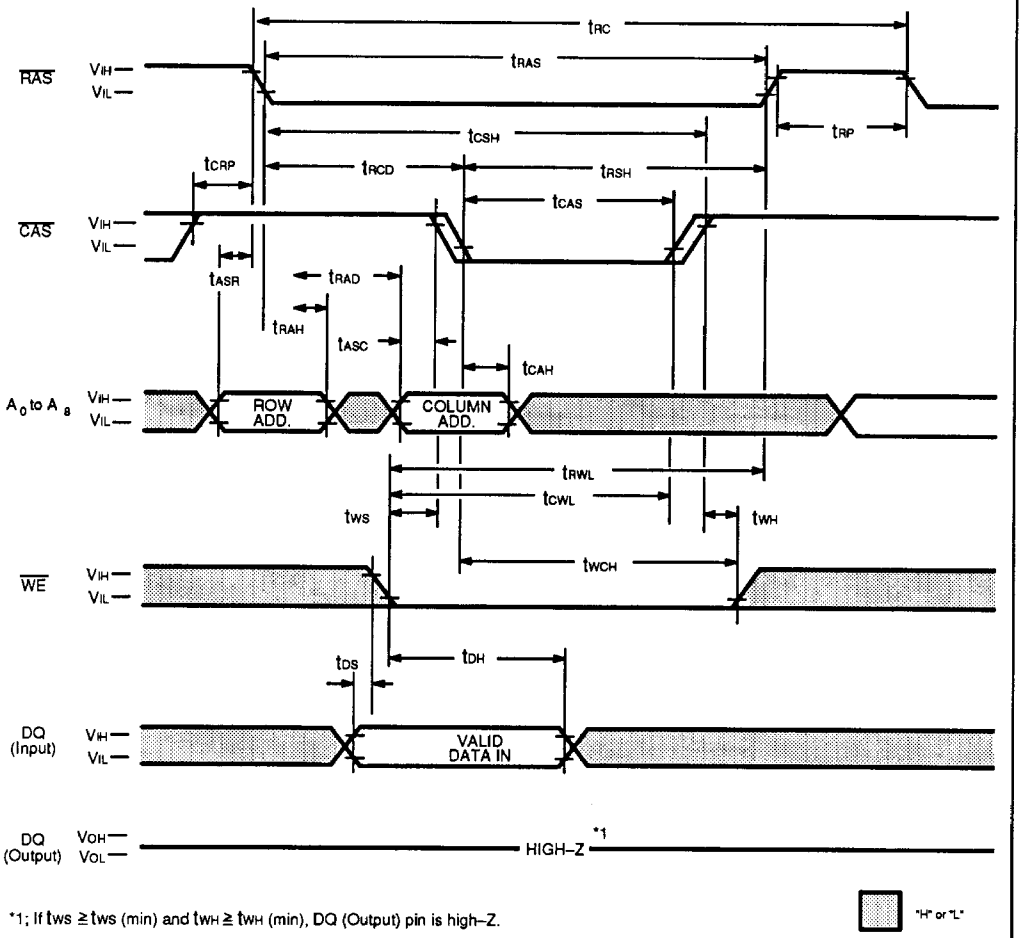
DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), OE, (tOEA) or column addresses (tAA) under the following conditions:

- If tRCD > tRCD (max), access time = tCAC.
- If tRAD > tRAD (max), access time = tAA.
- If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after tOH is satisfied.

Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



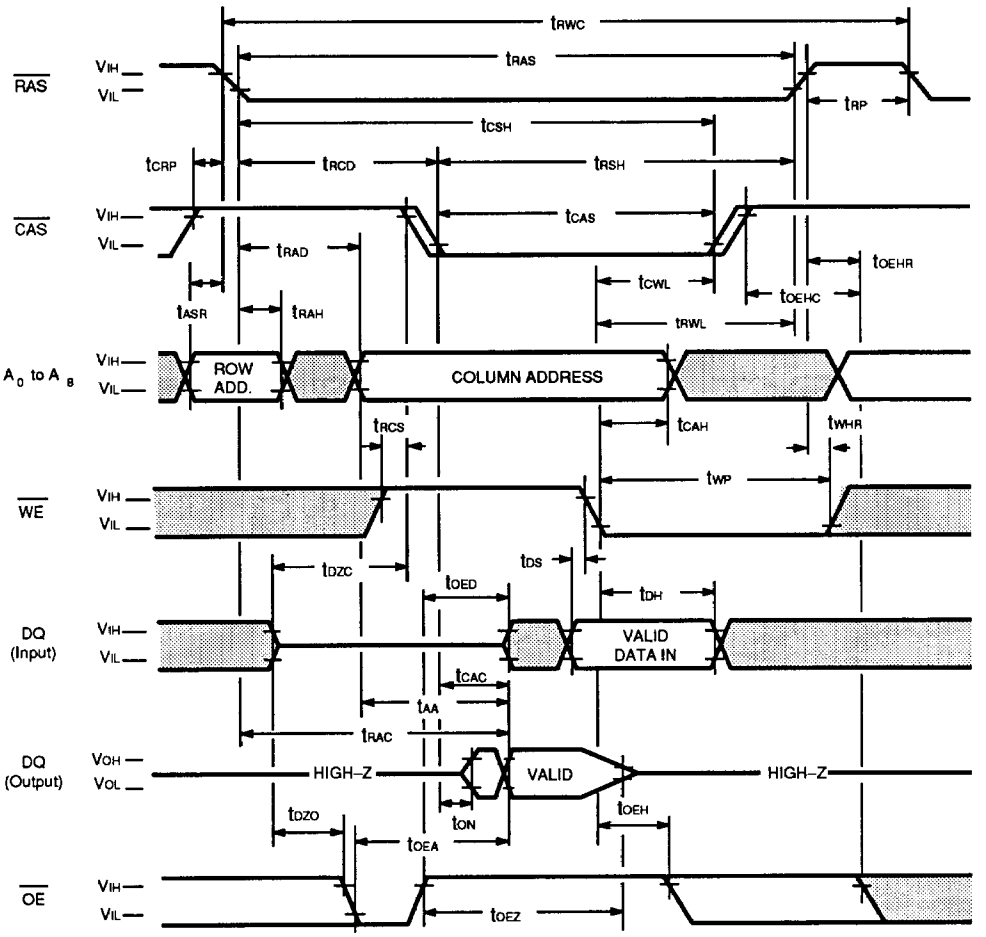
*1; If tWS ≥ tWS (min) and tWH ≥ tWH (min), DQ (Output) pin is high-Z.

DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways—early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above twcs satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

2

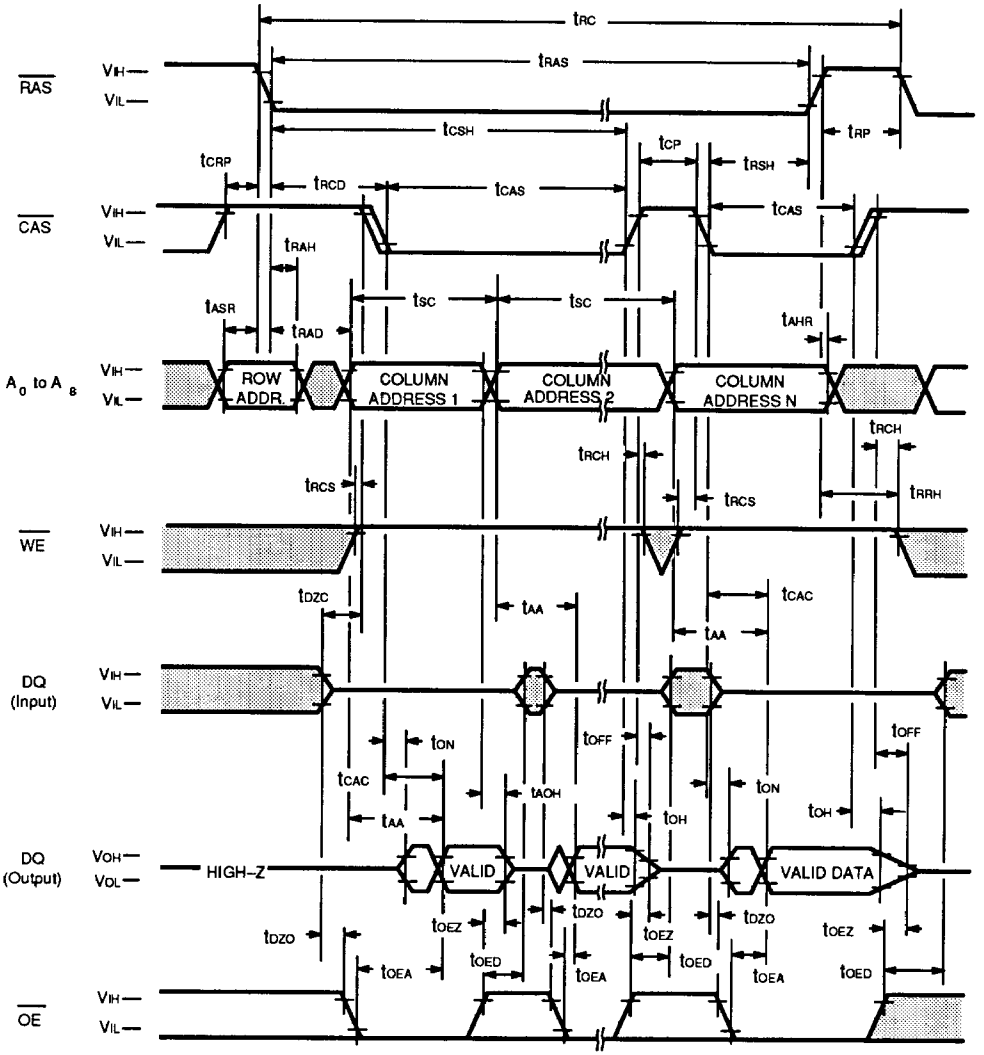
Fig. 6 – READ–MODIFY–WRITE–CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 7 – STATIC COLUMN MODE READ CYCLE

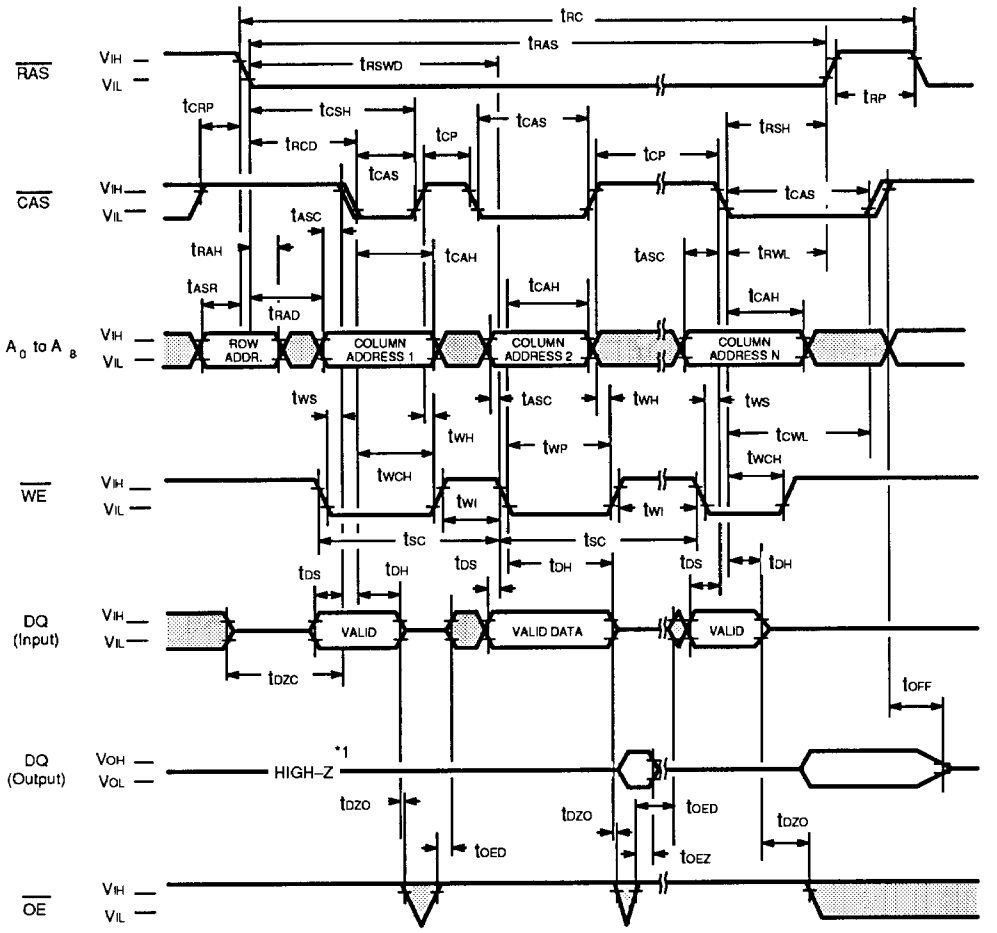


DESCRIPTION

In a static column mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input or t_{OEA} from the falling edge of $\overline{OE}$. The data remains valid for a time t_{AOH} after the column address is changed.

2

Fig. 8 – STATIC COLUMN MODE WRITE CYCLE ($\overline{OE}$ = "H " or "L")



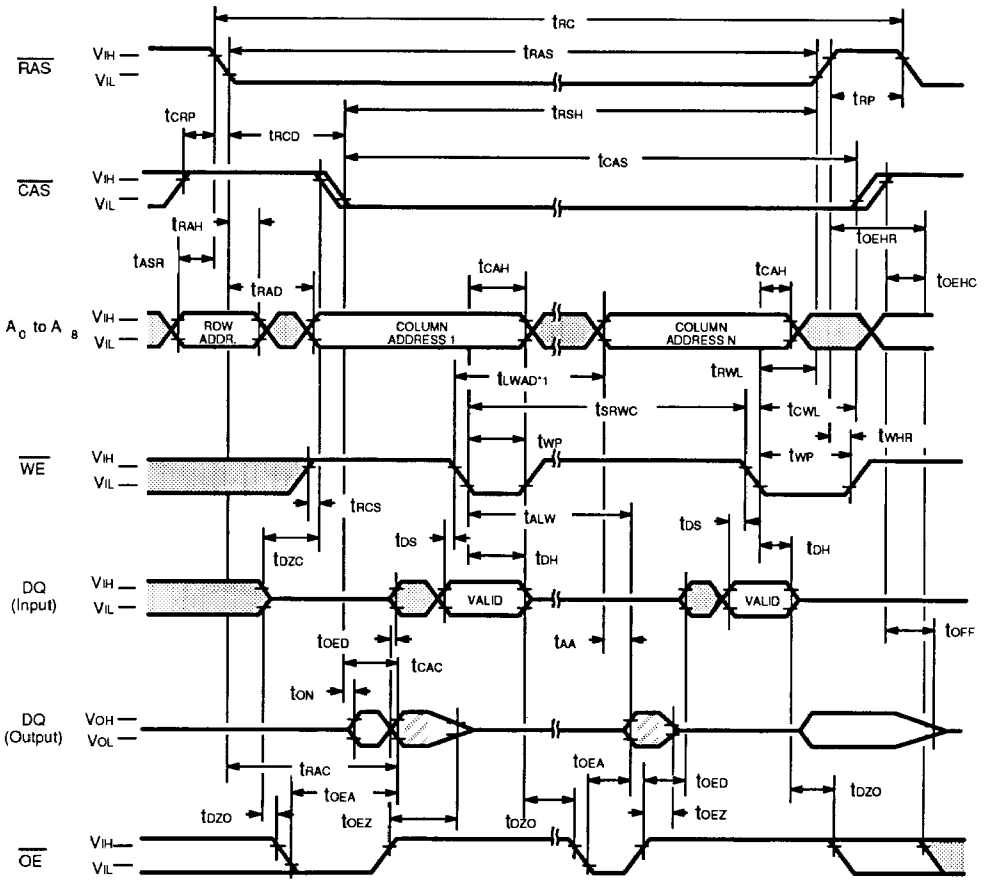
*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), DQ (Output) pin is high-Z.

"H" or "L"

DESCRIPTION

In a static column mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static column mode write cycle. The $\overline{OE}$ must be high before the data are applied to DQ pins.

Fig. 9 – STATIC COLUMN MODE READ–MODIFY–WRITE CYCLE



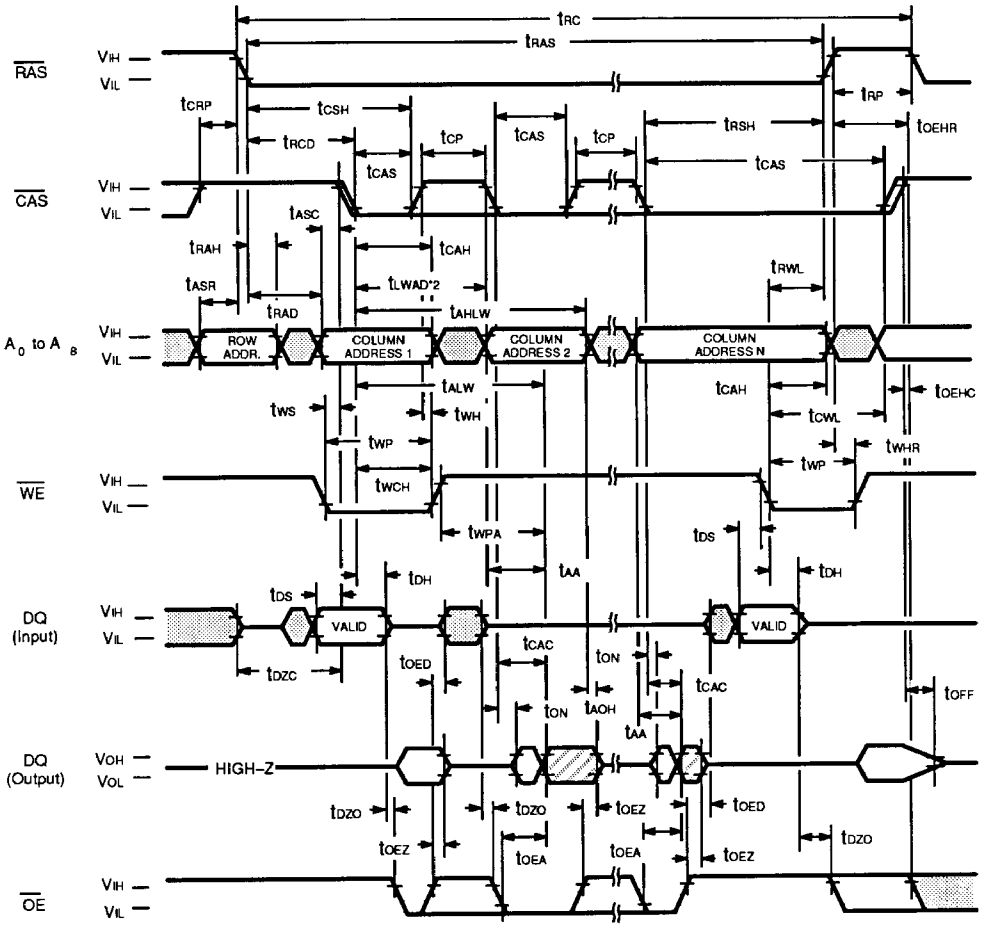
*1; If t_{LWAD} (min) ≤ t_{LWAD} ≤ t_{LWAD} (max), t_{ALW} = t_{SC} (min) + t_{AA} (max).

DESCRIPTION

In the static column mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the faling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of WE. The OE must be high before the data are applied to DQ pins.

2

Fig. 10 – STATIC COLUMN MODE MIXED CYCLE *1



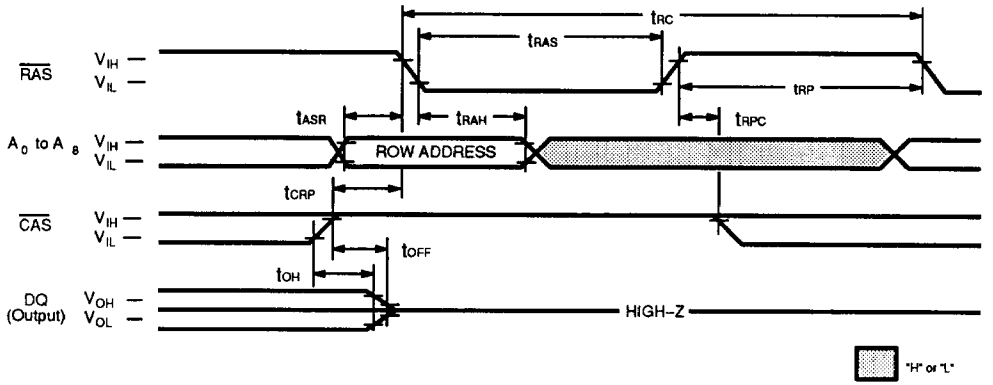
*1; This is an example of static column mode mixed cycle.
*2; If t_{LWAD} is satisfied its min/max value, $t_{ALW} = t_{SC}$ (min) + t_{AA} (max)

DESCRIPTION

In the static column mode, read, write, and read-modify-write cycles can be mixed in any order.
In the next read cycle of static column mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. t_{ALW} from the falling edge of $\overline{WE}$ or $\overline{CAS}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$
5. t_{OEA} from the falling edge of $\overline{OE}$

Fig. 11 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

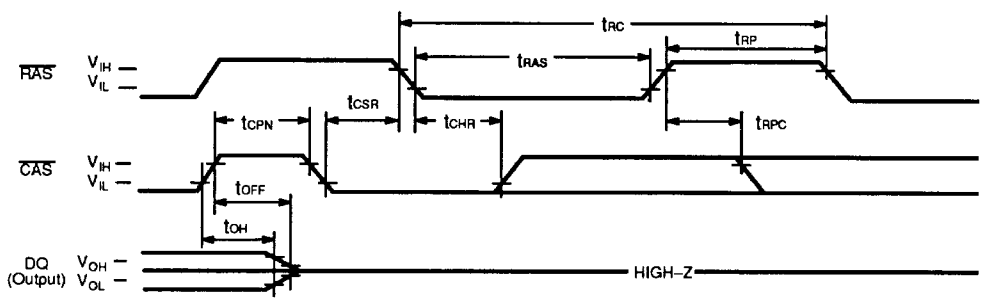


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available; $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

Fig. 12 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (A0 to A8 = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

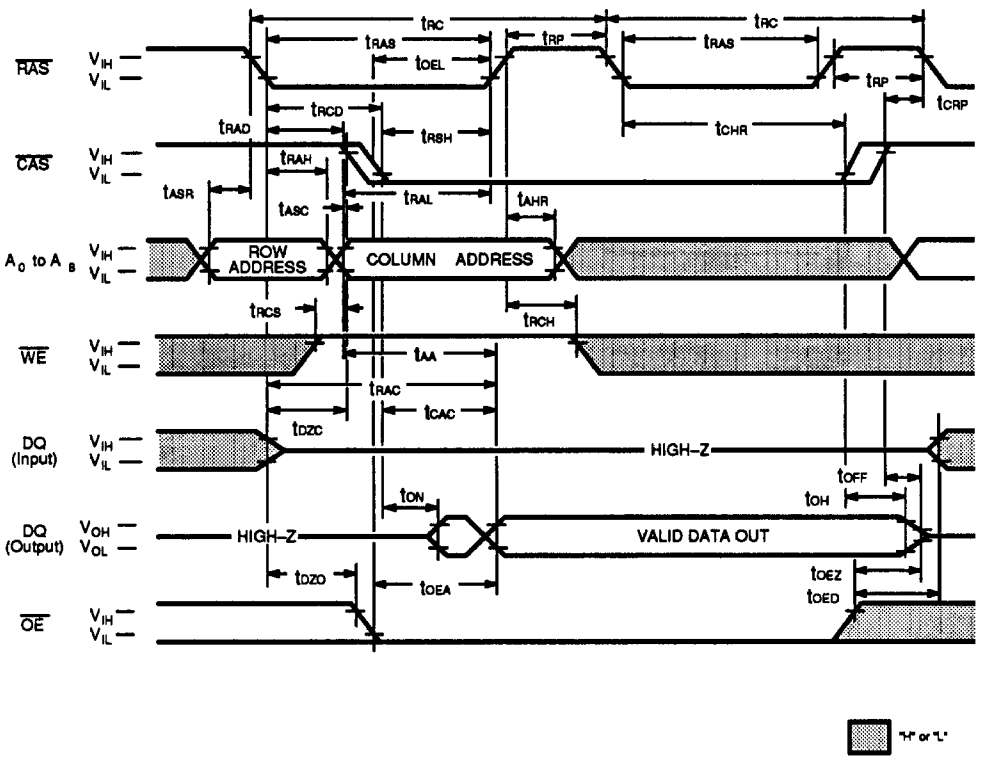


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

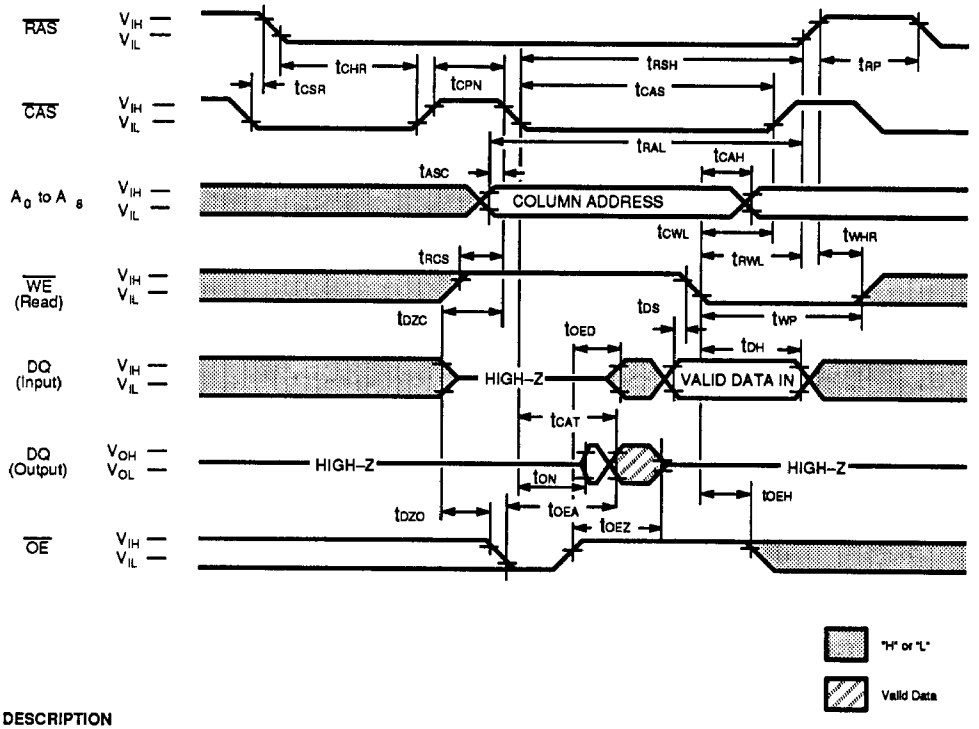
Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above, Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{CAS}$.

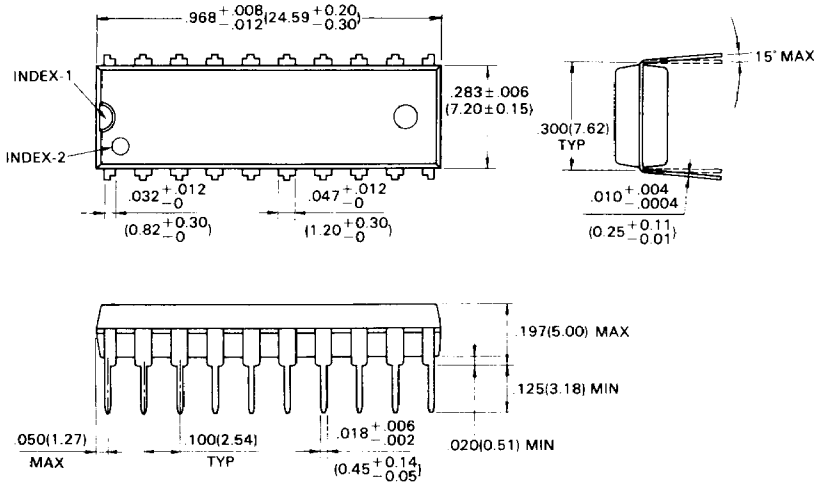
The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
4) Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 5.2 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix : –P)

20–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20P–M03)

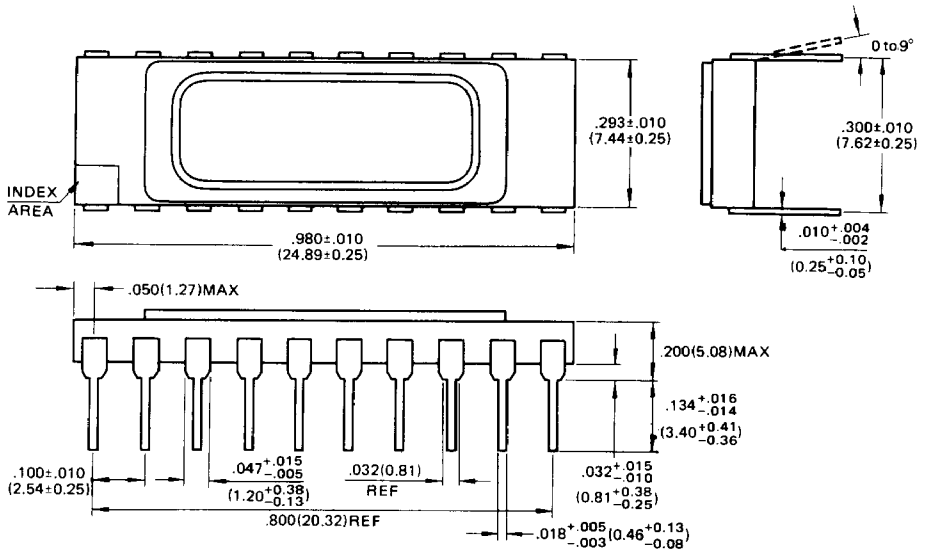


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)

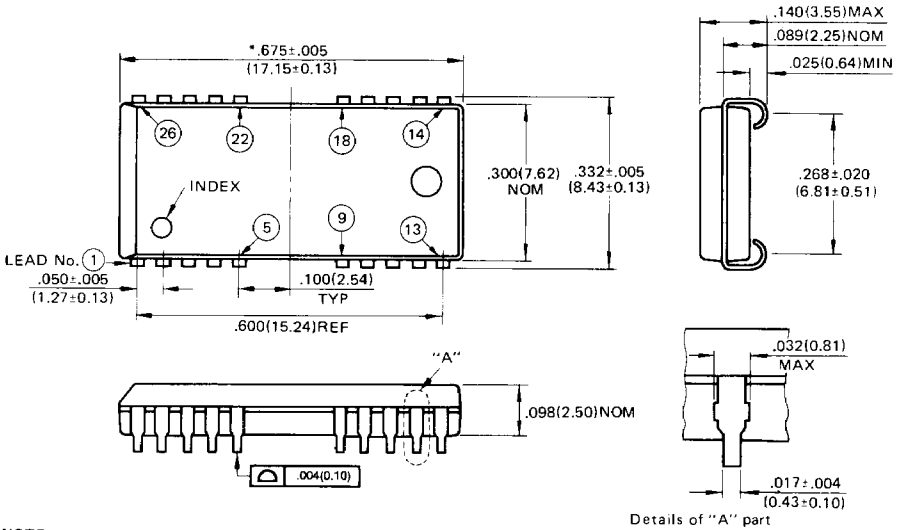


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)



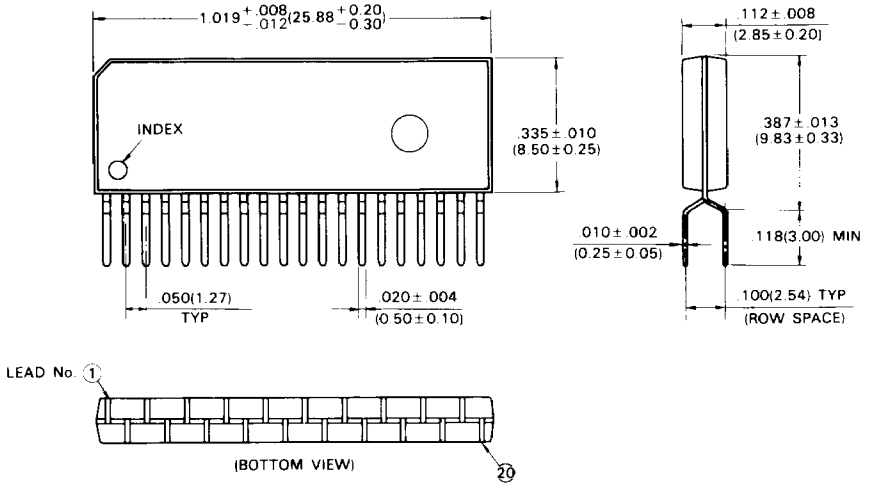
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



Dimensions in
inches (millimeters)