ADVANCE INFO.

AE0.1

MEMORY

CMOS

4 x 1M x 16 BIT DOUBLE DATA RATE SDRAM

MB81P641647A-10/-12

CMOS 4-BANK 1,048,576-WORD x 16 BIT
Synchronous Dynamic Random Access Memory
with Double Data Rate

■ DESCRIPTION

The Fujitsu MB81P641647A is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) containing 67,108,864 memory cells accessible in an 16-bit format. The MB81P641647A features a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81P641647A is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints. The MB81P641647A uses Double Data Rate (DDR) where data bandwidth is twice of fast speed compared with regular SDRAMs.

The MB81P641647A is ideally suited for Enterprise Systems, Servers, Workstations, Personal Computers, High Performance Graphic Adapters, Hardware Accelerators, Buffers, and other applications where large memory density and high bandwidth are required and where a simple interface is needed.

The MB81P641647A adopts new I/O interface circuitry, SSTL_2 interface, which is capable of extremely fast data transfer of quality under terminated bus environment.

■ PRODUCT LINE

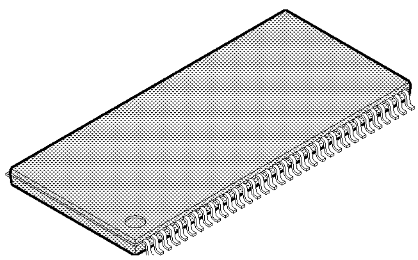
Parameter		MB81P641647A	
		-10	-12
Clock Frequency	CL = 2.0	100 MHz max	83 MHz max
	CL = 2.5	125 MHz max	100 MHz max
Burst Mode Cycle Time	CL = 2.0	5 ns min	6 ns min
	CL = 2.5	4 ns min	5 ns min
$\overline{RAS}$ Cycle Time		80 ns max	90 ns max
DQS Access Time From Clock		0.1*t_{CK} max	0.1*t_{CK} max
Operating Current (Two banks active)		260 mA max	240 mA max
Precharge Power Down Current		1 mA max	

■ FEATURES

- Double Data Rate
- Bi-directional Data Strobe Signal
- Quad independent bank operation
- Burst read/write operation
- Programmable burst type, burst length, and CAS latency
- Byte write control by DML/U
- Active and Precharge Power Down Mode
- 4096 Auto-refresh cycle in 64 ms
- Dual Self-refresh entry functions
  - Standard Self-refresh Command
  - Delayed Self-refresh Command
- SSTL_2 I/O for all signals
- V_{CC}: +3.3V Supply ± 0.3V tolerance
- V_{CCQ}: +2.5V Supply ± 0.2V tolerance

■ PACKAGE

Plastic 66-pin TSOP Package



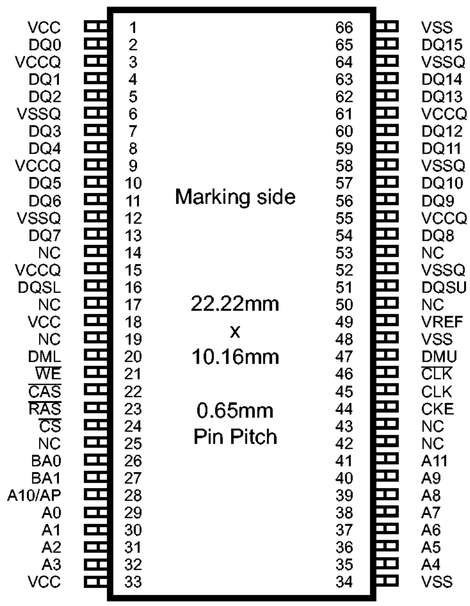
(FPT-66P-M01)

Package and Ordering Information

• 66-pin plastic (400mil) TSOP-II, order as MB81P641647A-xxFN

■ PIN ASSIGNMENTS AND DESCRIPTIONS

66-Pin TSOP:
<FPT-66P-Mxx>
(TOP VIEW)

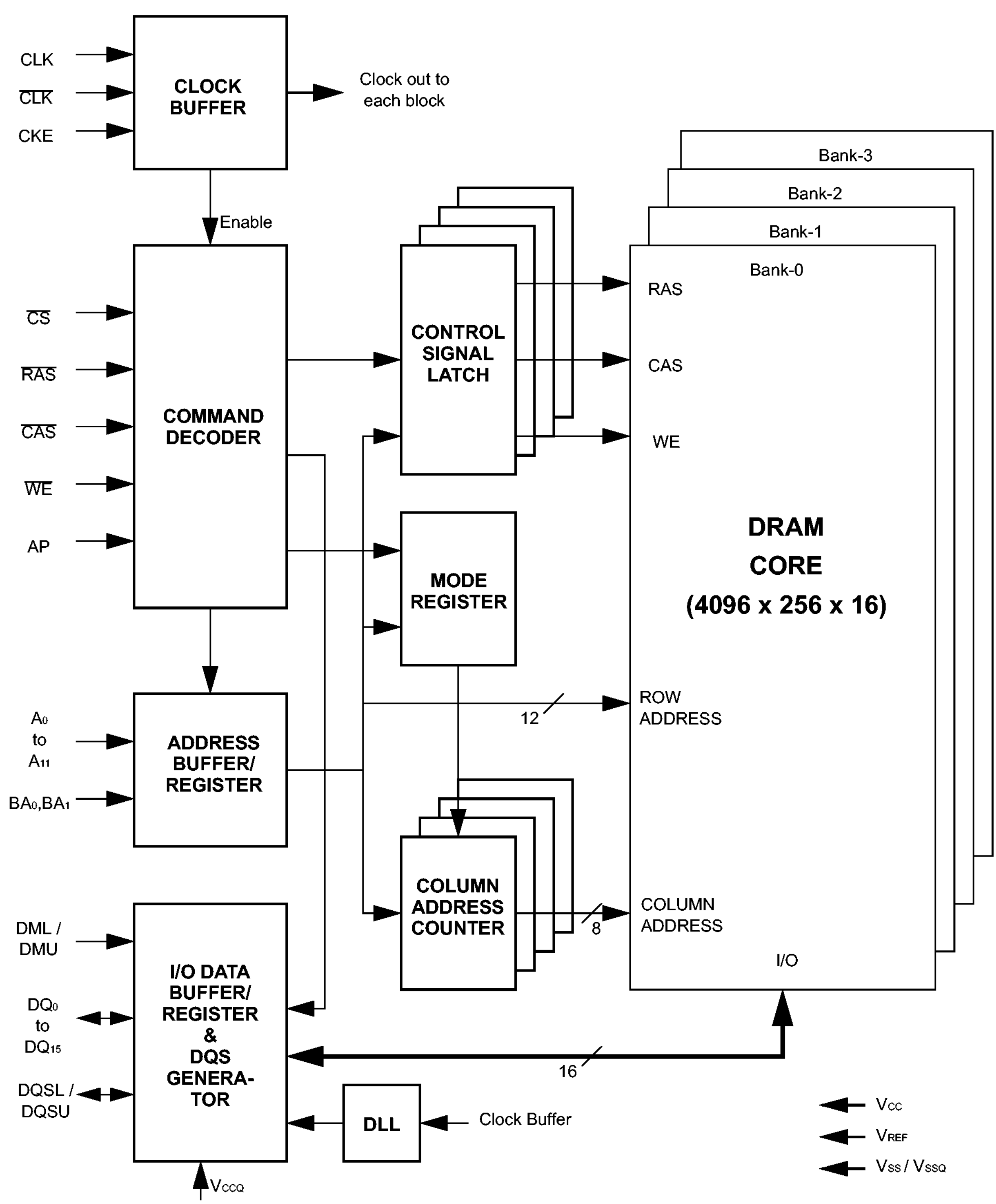


Pin Number	Symbol	Function
1, 18, 33	V_{CC}	Core Supply Voltage
3, 9, 15, 55, 61	V_{CCQ}	I/O Supply Voltage
6, 12, 34, 48, 52, 58, 64, 66	V_{SS}, V_{SSQ} *	Ground
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ_0 to DQ_{15}	Data I/O • Lower Byte: DQ_0 to DQ_7 • Upper Byte: DQ_8 to DQ_{15}
16	DQSL	Data Strobe for Lower Byte
51	DQSU	Data Strobe for Upper Byte
20	DML	Data Mask for Lower Byte
47	DMU	Data Mask for Upper Byte
21	$\overline{WE}$	Write Enable
22	$\overline{CAS}$	Column Address Strobe
23	$\overline{RAS}$	Row Address Strobe
24	$\overline{CS}$	Chip Select
26, 27	BA_0, BA_1	Bank Address
28	AP	Auto Precharge Enable
28, 29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 41	A_0 to A_{11}	Address Input • Row: A_0 to A_{11} • Column: A_0 to A_7
44	CKE	Power Down
45	CLK	Clock Input
46	$\overline{CLK}$	Clock Input
49	V_{REF}	Input Reference Voltage
14, 17, 19, 25, 42, 43, 50, 53	NC	No Connection

Note: *. These pins are connected internally in the chip and must be connected to the same ground level.

■ BLOCK DIAGRAM

Fig. 1 – MB81P641647A BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Note *1

COMMAND TRUTH TABLE

Note *2, and *3

Function	Notes	Symbol	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AP	BA_{0-1}	A_{11-9}	A_{8-0}
Device Deselect	*4	DESL	H	H	X	X	X	X	X	X	X
No Operation	*4	NOP	H	L	H	H	H	X	X	X	X
Burst Stop	*5	BST	H	L	H	H	L	X	X	X	X
Read	*6	READ	H	L	H	L	H	L	V	X	V
Read with Auto-precharge	*6	READA	H	L	H	L	H	H	V	X	V
Write	*6	WRIT	H	L	H	L	L	L	V	X	V
Write with Auto-precharge	*6	WRITA	H	L	H	L	L	H	V	X	V
Bank Active ($\overline{RAS}$)	*7	ACTV	H	L	L	H	H	V	V	V	V
Precharge Single Bank	*8	PRE	H	L	L	H	L	L	V	X	X
Precharge All Banks	*8	PALL	H	L	L	H	L	H	X	X	X
Mode Register Set	*8,*9	MRS	H	L	L	L	L	L	L	L	V

Notes: *1. V = Valid, L = Logic Low, H = Logic High, X = either L or H, Hi-Z = High Impedance.
*2. All commands are assumed to be valid state transitions.
*3. All inputs for command are latched on the rising edge of clock.
*4. NOP and DESL commands have the same effect on the part.
Unless specifically noted, NOP will represent both NOP and DESL command in later descriptions.
*5. BST is effective after READ command is issued.
*6. READ, READA, WRIT and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to STATE DIAGRAM in page 18.
*7. ACTV command should only be issued after corresponding bank has been precharged by PRE or PALL command.
*8. Either PRE or PALL command and MRS command are required after power up.
*9. MRS command should only be issued after all banks have been precharged (PRE or PALL command), and DQs are in Hi-Z. Refer to STATE DIAGRAM.

■ FUNCTION TRUTH TABLE (continued)

DML/DMU TRUTH TABLE (Effective during Write mode)

Function	Command	CKE	DML	DMU
Data Write for Lower Byte	—	H	L	X
Data Write for Upper Byte	—	H	X	L
Data Mask for Lower Byte	MASKL	H	H	X
Data Mask for Upper Byte	MASKU	H	X	H

CKE TRUTH TABLE

Current State	Function	Notes	Command	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AP	BA_{0-1}	A_{11-0}	Q_{0-7}
				n-1	n								
Idle	Auto-refresh	*10	REF	H	H	L	L	L	H	X	X	X	—
Idle	Self-refresh Entry	*10 *11	SELF	H	L	L	L	L	H	X	X	X	Hi-Z
Self-refresh	Self-refresh Exit		SELFX	L	H	L	H	H	H	X	X	X	Hi-Z
Idle, Active	Power Down Entry	*12	PDEN	H	L	L	H	H	H	X	X	X	Hi-Z
				H	L	H	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Exit		PDEX	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z

Notes:*10. The REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). In case of SELF command, it should also be issued after the last read data have been appeared on DQ. Refer to STATE DIAGRAM.

*11. CKE must bring to Low level together with or within 2 clock cycle from REF command.

*12. The PDEN command should only be issued after the last read data have been appeared on DQ and after the I_{DPL} is satisfied from last write data input.

■ FUNCTION TRUTH TABLE (continued)

OPERATION COMMAND TABLE (Applicable to single bank) Note *13

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*14
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*15
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Bank Active after t_{RCD}	
	L	L	H	L	BA, AP	PRE	NOP	
	L	L	H	L	BA, AP	PALL	NOP	*14
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*16
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after I_{MRD})	*16
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*14
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Precharge	
	L	L	H	L	BA, AP	PALL	Precharge	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

■ FUNCTION TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Bank Active)	
	L	H	H	L	X	BST	Terminate Burst -> Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge	
	L	L	H	L	BA, AP	PALL	Terminate Burst, Precharge	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Write Recovering)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Write Recovering)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP	*19
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge	*17
	L	L	H	L	BA, AP	PALL	Terminate Burst, Precharge	*14, *17
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

■ FUNCTION TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	CS	RAS	CAS	WE	Address	Command	Function	Notes
Read With Auto-Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*15
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Illegal	*15
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write with Auto Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Write Recovering with Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Write Recovering with Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Illegal	*15
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

■ FUNCTION TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Precharging	H	X	X	X	X	DESL	NOP (Idle after t_{RP})	
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})	
	L	H	H	L	X	BST	NOP (Idle after t_{RP})	*14
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*15
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	NOP	*15
	L	L	H	L	BA, AP	PALL	NOP	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})	
	L	H	H	H	X	NOP	NOP (Bank Active after t_{RCD})	
	L	H	H	L	X	BST	NOP (Bank Active after t_{RCD})	*14
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*15
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Illegal	*18
	L	L	H	L	BA, AP	PRE	Illegal	*15
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

■ FUNCTION TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	CS	RAS	CAS	WE	Address	Command	Function	Notes
Write Recovering	H	X	X	X	X	DESL	NOP (Bank Active after I_{WRD})	
	L	H	H	H	X	NOP	NOP (Bank Active after I_{WRD})	
	L	H	H	L	X	BST	NOP (Bank Active after I_{WRD})	*14
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*15
	L	H	L	L	BA, CA, AP	WRIT/WRITA	New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Illegal	*15
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write Recovering with Auto-precharge	H	X	X	X	X	DESL	NOP (Idle after I_{DAL})	
	L	H	H	H	X	NOP	NOP (Idle after I_{DAL})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*15
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AP	PRE	Illegal	*15
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after t_{RC})	
	L	H	H	X	X	NOP/BST	NOP (Idle after t_{RC})	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF/ MRS	Illegal	

■ FUNCTION TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after l_{MRD})	
	L	H	H	H	X	NOP	NOP (Idle after l_{MRD})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	Illegal	

Abbreviations: RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

Notes:*13. All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle.
*14. Entry may affect other banks.
*15. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
*16. Illegal if any bank is not idle.
*17. Must mask preceding data that don‘t satisfy l_{DPL}.
*18. Legal if other bank specified in BA is idle state and t_{RRD} is satisfied for that bank.
*19. Must mask preceding data that don‘t satisfy l_{WRD}.

■ FUNCTION TRUTH TABLE (Continued)

COMMAND TRUTH TABLE FOR CKE

Current State	CKE (n-1)	CKE (n)	CS	RAS	CAS	WE	Address	Function	Notes
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery -> Idle after t_{PDEX} + t_{RC})	
	L	H	L	H	H	H	X	Exit Self-refresh (Self-refresh Recovery -> Idle after t_{PDEX} + t_{RC})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	H	X	Idle after t_{RC}	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Power Down Exit -> Return to original state after t_{PDEX}	
	L	H	L	H	H	H	X	Power Down Exit -> Return to original state after t_{PDEX}	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	

■ FUNCTION TRUTH TABLE (continued)

COMMAND TRUTH TABLE FOR CKE (continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
All Banks Idle	H	H	H	X	X	X	X	NOP	
	H	H	L	H	X	X	V	Refer to the Command Truth Table.	
	H	H	L	L	H	X	V	Refer to the Command Truth Table.	
	H	H	L	L	L	H	X	Auto-refresh	
	H	H	L	L	L	L	V	Mode Register Set	*20
	H	L	H	X	X	X	X	Power Down Entry	*21
	H	L	L	H	H	H	X	Power Down Entry	*21
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh Entry	*21
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	
Bank Active	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	H	X	X	X	X	Power Down Entry	*21
	H	L	L	H	H	H	X	Power Down Entry	*21
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	X	X	X	Illegal	
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	

■ FUNCTION TRUTH TABLE (continued)

COMMAND TRUTH TABLE FOR CKE (continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Bank Activating, Read, Write, Write Recovering, Precharging	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*22
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*22
Refresh	H	L	H	L	L	L	X	Delayed Self-Refresh	*23
	H	L	L	H	H	H	X	Delayed Self-Refresh	*23
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	

Notes:*20. Refer to MODE REGISTER TABLE.
*21. PDEN and SELF command should only be issued after the last read data have been appeared on DQ.
*22. The Clock Suspend mode is not supported on this device and it is illegal if CKE is brought to Low during the Burst Read or Write mode.
*23. This device enters the Delayed Self-Refresh mode, if CKE is brought to Low within 2 clock cycles from 2 clock cycles from REF-command.
And this device enters the Precharge Power Down mode, if CKE is brought to Low over 2 clock cycles from 2 clock cycles from REF-command.

■ STATE DIAGRAM

MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

First command \ Second command (same bank)	MRS	ACTV	READ	READA	WRIT	WRITA	BST	PRE	PALL *2	REF	SELF
MRS	l_{MRD}	l_{MRD}					l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}
ACTV			t_{RCD}	l_{RCD} *4	t_{RCD}	l_{RCD} *4	1	t_{RAS}	t_{RAS}		
READ			1	1 *4	l_{RWD} *3	l_{RWD} *3, 4	1	1 *4	1 *4		
READA	BL/2 + t_{RP} *5, 6	BL/2 + t_{RP}						BL/2 + t_{RP} *4	BL/2 + t_{RP} *4	BL/2 + t_{RP} *6	BL/2 + t_{RP} *5, 6
WRIT			l_{WRD} *7	l_{WRD} *4, 7	1	1 *4		l_{DPL} *4,7	l_{DPL} *4,7		
WRITA	l_{WAL} *6	l_{WAL}						l_{WAL} *4	l_{WAL} *4	l_{WAL} *6	l_{WAL} *6
BST			1	1	l_{BSNC} *3	l_{BSNC} *3	1	1 *4	1 *4		
PRE	t_{RP} *5, 6	t_{RP}					1	1	1 *4	t_{RP} *6	t_{RP} *5, 6
PALL	t_{RP} *5	t_{RP}					1	1	1	t_{RP}	t_{RP} *5
REF	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

Notes:
*1. BL/2 = t_{CK} * BL / 2. (Example: In case of BL = 4, BL/2 means 2 clocks.)
*2. Assume PALL command does not affect any operation on the other bank(s).
*3. Assume no I/O conflict.
*4. t_{RAS} must be satisfied.
*5. Assume all outputs are in High-Z state.
*6. Assume all other banks are in idle state.
*7. l_{DPL} and l_{WRD} are specified from last data input and assumed preceding pair of write data are masked by DML/DMU input.

(Shaded cells:) Illegal or Inapplicable Command

■ STATE DIAGRAM (continued)

MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTIPLE BANK OPERATION

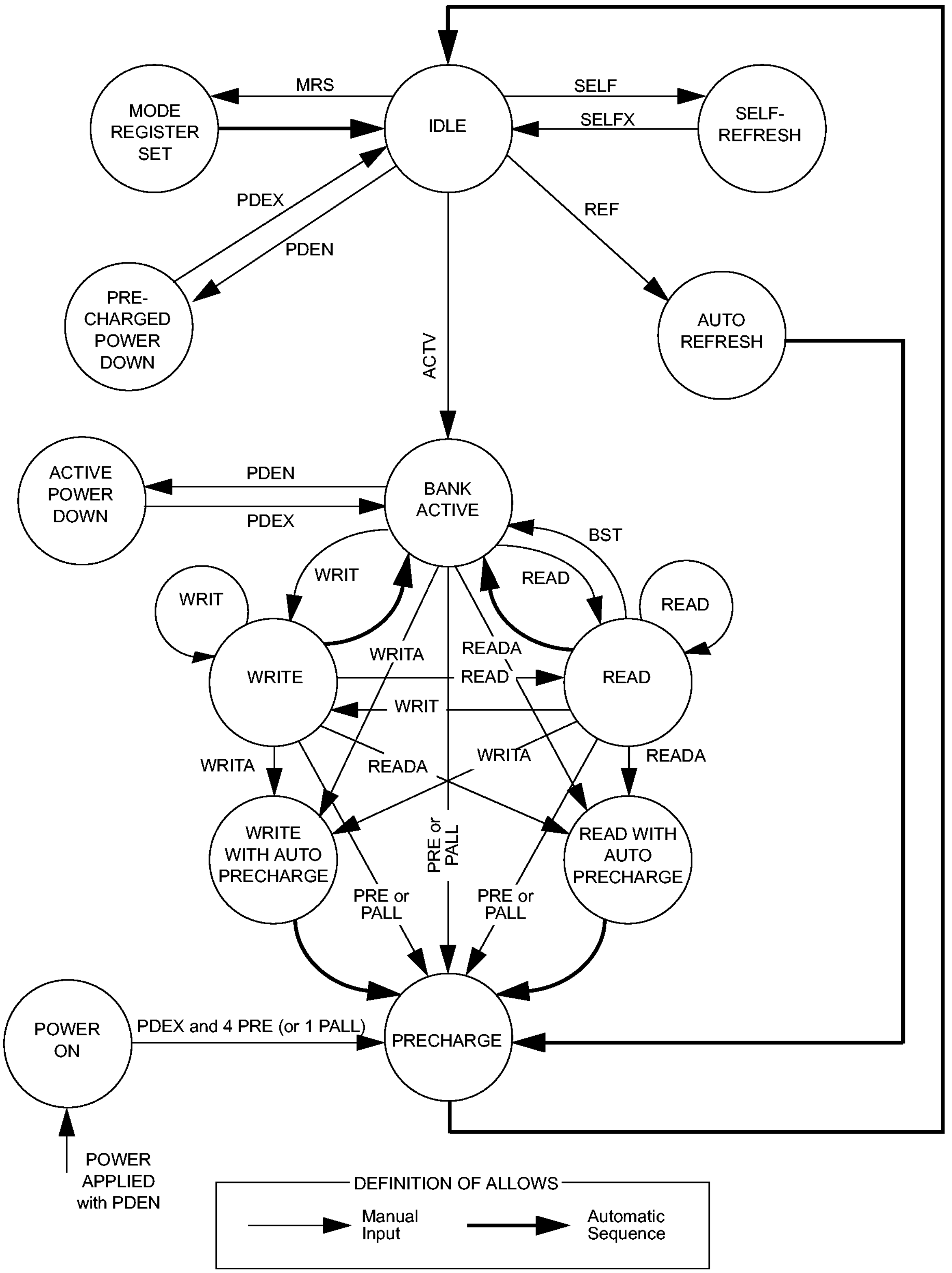
First command \ Second command (other bank) *10	MRS	ACTV	READ	READA	WRIT	WRITA	BST	PRE *9	PALL *2, 9	REF	SELF
MRS	l_{MRD}	l_{MRD}					l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}
ACTV		t_{RRD} *6	1 *8, 11	1 *8, 11	1 *8, 11	1 *8, 11	1 *11	1	t_{RAS}		
READ		1 *6, 12	1 *8	1 *8	l_{RWD} *3, 8	l_{RWD} *3, 8	1	1	1 *4		
READA	BL/2 + t_{RP} *5, 6	1 *6, 12	1 *8, 4	1 *8, 4	l_{RWD} *3, 4, 8	l_{RWD} *3, 4, 8		1	BL/2 + t_{RP}	BL/2 + t_{RP} *6	BL/2 + t_{RP} *5, 6
WRIT		1 *6, 12	l_{WRD} *7,8	l_{WRD} *7,8	1 *8	1 *8		1	l_{DPL} *4,7		
WRITA	l_{WAL} *6	1 *6, 12	BL/2 + l_{WRD} *4, 8	BL/2 + l_{WRD} *4, 8	1 *4, 8	1 *4, 8		1	l_{WAL}	l_{WAL} *6	l_{WAL} *6
BST		1 *6, 12	1 *8, 11	1 *8, 11	l_{BSNC} *3, 8, 11	l_{BSNC} *3, 8, 11		1	1 *4		
PRE	t_{RP} *5, 6	1 *6, 12	1 *8, 11	1 *8, 11	1 *3, 8, 11	1 *3, 8, 11	1 *11	1	1 *4	t_{RP} *6	t_{RP} *5, 6
PALL	t_{RP} *5	t_{RP}					1	1	1	t_{RP}	t_{RP} *5
REF	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

Notes: *1. BL/2 = t_{CK} * BL / 2. (Example: In case of BL = 4, BL/2 means 2 clocks.)
*2. Assume PALL command does not affect any operation on the other bank(s).
*3. Assume no I/O conflict.
*4. t_{RAS} must be satisfied.
*5. Assume all outputs are in High-Z state.
*6. Assume the other bank(s) is in idle state.
*7. l_{DPL} and l_{WRD} are specified from last data input and assumed preceding pair of write data are masked by DML/DMU input.
*8. Assume the other bank(s) is in active state and t_{RCD} is satisfied.
*9. Assume the other bank(s) is in active state and t_{RAS} is satisfied.
*10. Second command have to follow the minimum clock latency or delay time of single bank operation in other bank (second command is asserted.)
*11. Assume other banks are not in READA/WRITA state.
*12. t_{RRD} is satisfied.

(shaded box) Illegal or Inapplicable Command.

■ STATE DIAGRAM (continued)

Fig. 2 – STATE DIAGRAM (Simplified for Single Bank Operation)



■ FUNCTIONAL DESCRIPTION

DDR, Double Data Rate Function

The regular SDRAM read and write cycle have only used the rising edge of external clock input. When clock signal goes to High from Low at the read mode, the read out data will be available at every rising clock edge after the specified latency up to burst length. The MB81P641647A DDR SDRAM features a twice of data transfer rate within a same clock period by transferring data at every rising and falling clock edge. Refer to Figure 3 in Page 24.

CLOCK (CLK, $\overline{CLK}$)

The MB81P641647A adopts differential clock scheme. CLK is a master clock and its rising edge is used to latch all command and address inputs. $\overline{CLK}$ is a complementary clock input.
The MB81P641647A implements Delay Locked Loop (DLL) circuit. This internal DLL tracks the signal cross point between CLK and $\overline{CLK}$ and generate some clock cycle delay for the output buffer control at Read mode.
The internal DLL circuit requires some Lock-on time for the stable delay time generation. In order to stabilize the delay, a constant stable clock input for I_{PCD} period is required during the Power-up initialization and a constant stable clock input for I_{SCD} period is also required after Self-refresh exit as specified I_{SCD} prior to the any command.

CLOCK ENABLE (CKE)

CKE is a synchronous input signal and enables two power down modes.
When all banks are in idle state, CKE controls Precharged Power Down (PPD) and Self-refresh mode. The PPD and Self-refresh is entered when CKE is brought to Low and exited when it returns to High.
During the Power Down and Self-refresh mode, both CLK and $\overline{CLK}$ are disabled after specified time.
CKE does not have a Clock Suspend function unlike CKE pin of regular SDRAMs, and it is illegal to bring CKE into Low if any read or write operation is being performed. For the detail, refer to Timing Diagrams.
When any bank is in active state and not being accessed, CKE controls Active Power Down (APD) mode and it will disable all other input and output signals except for the CLK, $\overline{CLK}$ and CKE itself.
It is recommended to maintain CKE to be Low until V_{CC} gets in the specified operating range in order to assure the power-up initialization.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address input. When $\overline{CS}$ is High, all command signals are negated but internal operation such as burst cycle will not be suspended.

COMMAND INPUTS ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

As well as regular SDRAMs, each combination of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SDRAM operation. Refer to FUNCTION TRUTH TABLE in page 5.

■ FUNCTIONAL DESCRIPTION (continued)

BANK ADDRESS (BA_0, BA_1)

The MB81P641647A has four internal banks and each bank is organized as 1M words by 16-bit.
Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and Precharge Single Bank(PRE) command.

ADDRESS INPUTS (A_0 to A_{11})

Address input selects an arbitrary location of a total of 1,048,576 words of each memory cell matrix within each bank. A total of twenty address input signals are required to decode such a matrix. DDR SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), twelve Row addresses are initially latched as well as two bank addresses and the remainder of eight Column addresses are then latched by a Column address strobe command of either a read command (READ or READA) or write command (WRIT or WRITA).

DATA STROBE (DQSL, DQSU)

DQSL and DQSU are bi-directional signal and represent lower and upper byte respectively. During Read operation, DQSL and DQSU provide the read data strobe signal that is intended to use input data strobe signal at the receiver circuit of the controller(s). It turns Low before first data is coming out and toggle High to Low or Low to High till end of burst read. Refer to Figure 3 for the timing example.
The CAS Latency is specified to the first Low to High transition of this DQSL/U output.
During the write operation, DQSL/U are used to latch write data and Data Mask signals. As well as the behavior of read data strobe, the first rising edge of DQSL/U input latches first input data and following falling edge of DQSL/U signal latches second input data. This sequence shall be continued till end of burst count. Therefore, DQSL/U must be provided from controller that drives write data.
Note that DQSL/U input signal should not be tristated from High at the end of write mode.

DATA INPUTS AND OUTPUTS (DQ_0 to DQ_{15})

Input data is latched by DQSL/U input signal and written into memory at the clock following the write command input.
Output data is obtained together with DQSL/U output signals at programmed read CAS latency.
The polarity of the output data is identical to that of the input. Data is valid after DQSL/U output signal transitions (t_{QSQ}) as specified in Data Valid Time (t_{DV}).

WRITE DATA MASK (DML, DMU)

DML and DMU are active High enable inputs and represent lower and upper byte respectively. The both of DML and DMU have a data input mask function, and are also sampled by DQSL/U input signal together with input data. During write cycle, DML and DMU provide byte mask function. When DMx = High is latched by a DQSL/U signal edge, data input at the same edge of DQSL/U is masked.

During read cycle, the DML and DMU inactive and does not have any effect on read operation.
Refer to DML/DMU TRUTH TABLE in page 6.

■ FUNCTIONAL DESCRIPTION (continued)

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access and MB81P641647A read and write operations are burst oriented. The burst mode is implemented by keeping the same Row address and by automatic strobing Column address in every single clock edge till programmed burst length(BL). Access time of burst mode is specified as t_{ACQ}. The internal column address counter operation is determined by a mode register which defines burst type(BT) and burst count length(BL) of 2, 4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 2, the following combinations will be required.

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	**Burst Stop Command (BST)**
		2nd Step	Write Command after I_{BSNC}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	1st Step	**Data Mask Input**
		2nd Step	Read Command after I_{WRD} from last data input
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	1st Step	**Data Mask Input**
		2nd Step	Precharge Command after I_{DPL} from last data input

The burst type can be selected either sequential or interleave mode. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to the least significant address(= 0). The interleave mode is a scrambled decoding scheme for A_0 to A_2 depending on the burst length. If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode	Interleave
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

■ FUNCTIONAL DESCRIPTION (continued)

BURST STOP COMMAND (BST)

The Burst Stop command (BST) terminates the burst read operation except for a case that Auto-precharge option is asserted. When the BST command is issued during the burst read operation, the all output buffers, DQs and DQSL/U, will turn to High-Z state after some latencies that to be matched with programmed CAS latency and internal bank state remains active state.
In a case of terminating the burst write operation, the BST command should not be issued at any time during burst write operation. Refer to previous page for the write interrupt and termination rule.

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

The DDR SDRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the precharge operation (PRE or PALL). With the precharge operation, DDR SDRAM will automatically be in standby state after specified precharge time (t_{RP}).
The precharged bank is selected by combination of AP and bank address (BA) when precharge command is issued. If AP = High, all banks are precharged regardless of BA (PALL command). If AP = Low, a bank to be selected by BA is precharged (PRE command).
The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command issue. This auto-precharge is entered by AP = High when a Read (READ) or Write (WRIT) command is issued.
Applying BST is illegal if the Auto-precharge option is used.
Refer to FUNCTION TRUTH TABLE.

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The MB81P641647A Auto-refresh command (REF) automatically generates Bank Active and Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be issued within every 16 μs period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh operation until cancelled by SELFX.
The Self-refresh mode is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once MB81P641647A enters the self-refresh mode, all inputs except for CKE can be either logic high or low level state and outputs will be in a High-Z state. During Self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

DELAYED SELF-REFRESH ENTRY

The MB81P641647A also supports Delayed Self-refresh Entry. The entry timing is the same as standard self-refresh but CKE timing, and CKE can be brought to Low within 2 clock cycles from REF command.
The all other timing relations and constraints are the same as standard self-refresh entry.

SELF-REFRESH EXIT (SELFX)

To exit Self-refresh mode, CKE must bring to High for at least 2 clock cycles together with NOP condition.
Refer to Timing Diagram for the detail procedure. It is recommended to issue at least one Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.

WARNING: A stable clock for I_{SCD} period with a constant duty cycle must be supplied prior to applying any read command to insure the DLL is locked against the latest device conditions.

■ FUNCTIONAL DESCRIPTION (continued)

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS Latency, and Test Mode Entry (This Test Mode Entry must not be used). Refer to MODE REGISTER TABLE in page 25.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all banks are in idle state and all DQS are in High-Z. The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization.

Refer to POWER-UP INITIALIZATION below.

Note: The MB81P641647A does not support the DLL Reset function on A_8 of MRS field. However they will be ignored regardless of its input.
The Extended Mode Register Set command (EMRS) and its DLL Enable function of EMRS field is also not supported by MB81P641647A.

POWER-UP INITIALIZATION

The MB81P641647A internal condition at and after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply V_{CC} before or at the same time as V_{CCQ} and attempt to maintain all input signals to be Low state (or at least CKE to be Low state).
2. Apply V_{CCQ} before or at the same time as V_{REF} and V_{TT}.
3. Apply V_{REF} and V_{TT}. (V_{TT} is applied to the system).
4. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200μs.
5. After the minimum of 200μs stable power and clock, apply NOP condition and take CKE to be High state.
6. Issue Precharge All Banks (PALL) command or Precharge Single Bank (PRE) command to every banks. An additional clock input for l_{PCD}*1 period is required to lock the DLL *2
7. Apply minimum of 2 Auto-refresh command (REF).*3
8. Program the mode register by Mode Register Set command (MRS).*3

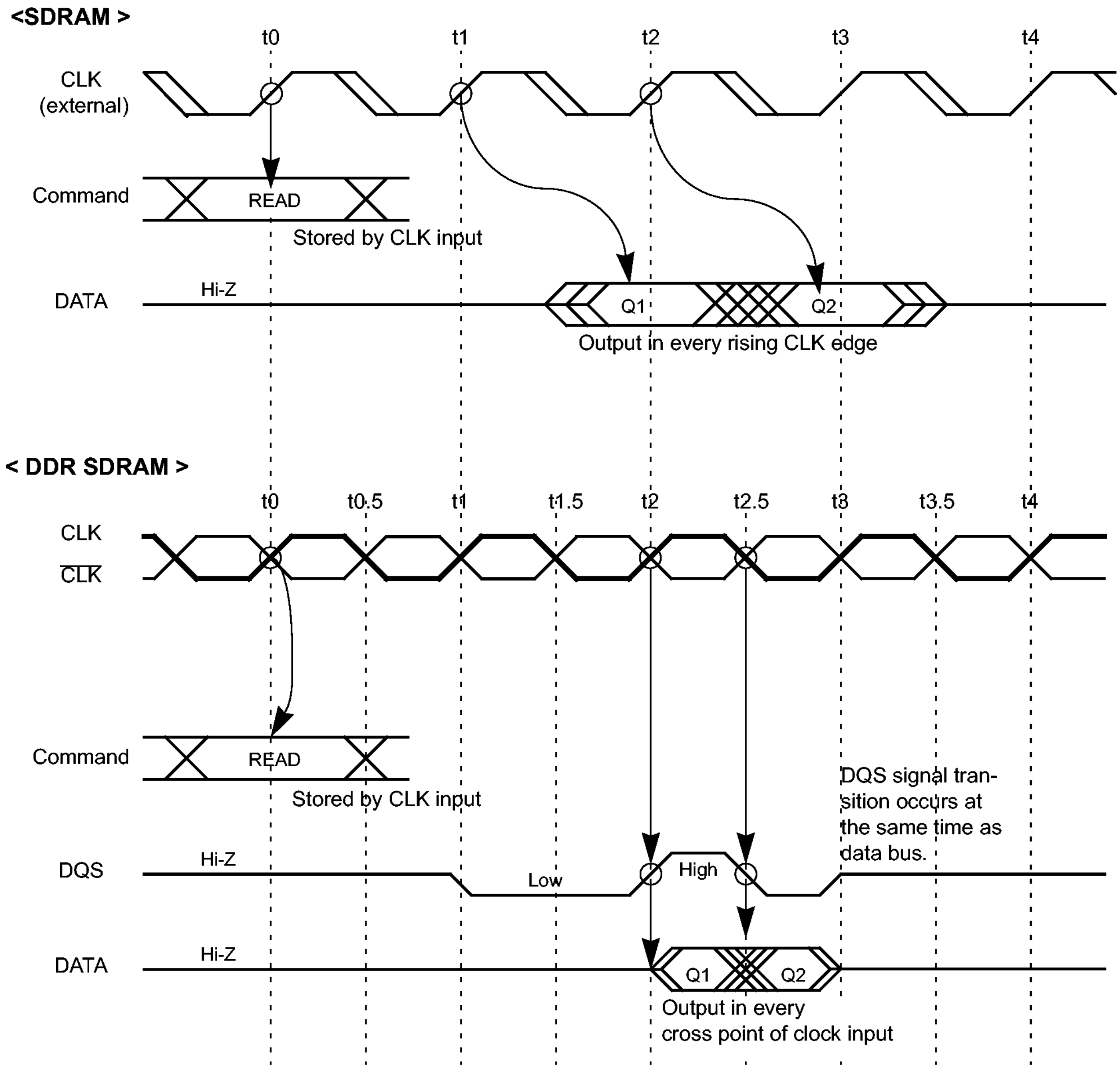
Notes: *1. The l_{PCD} depends on operating clock cycle time. The l_{PCD} is counted from precharge last bank (step-6) to MRS command (step-8).
*2. The MB81P641647A does not support JEDEC standard EMRS and DDR Reset function on MRS. However, those sequence can be issued prior to step 6.
*3. The Mode Register Set command (MRS) can be issued before 2 Auto-refresh command (REF).

POWER-DOWN

The MB81P641647A uses multiple power supply voltage. It is required to follow the reversed sequence of above Power On Sequence to the each power supply, V_{CC}, V_{CCQ}, V_{REF} and V_{TT}, or must turn all power supplies off at once.

■ FUNCTIONAL DESCRIPTION (continued)

Fig. 3 – SDRAM READ TIMING EXAMPLE (@ CL=2 & BL=2)



■ MODE REGISTER TABLE

MODE REGISTER SET

BA_1	BA_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS FIELD
0*1	0*1	RESERVED *2			DR*3	TE	CL			BT	BL			MODE REGISTER

A_6	A_5	A_4	CAS Latency (CL)
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A_2	A_1	A_0	Burst Length (BL)	
			BT = 0	BT = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

A_7	Test Mode Entry (TE)
0	Normal Operation
1	Test Mode (Used for Supplier Test Mode)

A_3	Burst Type (BT)
0	Sequential (Wrap round, Binary up)
1	Interleave (Wrap round)

EXTENDED MODE REGISTER SET (Note *4)

BA_1	BA_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS FIELD
0*5	1*5	RESERVED *2											DE*6	EXTENDED MODE REGISTER

Notes:
*1. A combination of $BA_1 = BA_0 = 0$ (Low) selects standard Mode Register.
*2. The RESERVED field must be set as 0.
*3. DR (DLL Reset) on A_8 in MRS is currently not used and must be always set as 0.
*4. The Extended Mode Register Set is not supported.
*5. A combination of $BA_1 = 0$ and $BA_0 = 1$ (High) selects Extended Mode Register.
*6. DE (DLL Enable) on A_0 in EMRS is currently not used and must be always set as 0.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING below.)

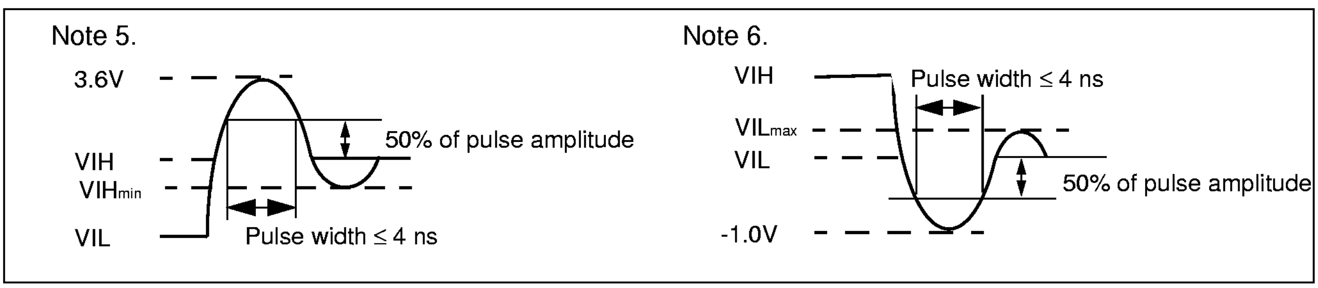
Parameter	Symbol	Value	Unit
Voltage of V_{CC} Supply Relative to V_{SS}	V_{CC}, V_{CCQ}	-0.5 to +4.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS (See WARNING below.)

(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{CC}	3.0	3.3	3.6	V
		V_{CCQ}	2.3	2.5	2.7	V
		V_{SS}, V_{SSQ}	0	0	0	V
Input Reference Voltage	*1	V_{REF}	V_{CCQ} * 0.48	V_{CCQ} * 0.5	V_{CCQ} * 0.52	V
Termination Voltage	*2	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
Single Ended SSTL DC Level Input High Voltage	*3	$V_{IH (DC)}$	V_{REF} + 0.18	—	V_{CCQ} + 0.3	V
Single Ended SSTL DC Level Input Low Voltage	*3	$V_{IL (DC)}$	- 0.3	—	V_{REF} - 0.18	V
Single Ended SSTL AC Level Input High Voltage	*3	$V_{IH (AC)}$	V_{REF} + 0.35	—	—	V
Single Ended SSTL AC Level Input Low Voltage	*3	$V_{IL (AC)}$	—	—	V_{REF} - 0.35	V
Differential DC Level Input Voltage Range	*3	$V_{IN (DC)}$	- 0.3	—	V_{CCQ} + 0.3	V
Differential DC Level Differential Input Voltage	*3	$V_{SWING (DC)}$	0.36	—	V_{CCQ} + 0.6	V
Differential AC Level Differential Input Voltage	*3	$V_{SWING (AC)}$	0.7	—	—	V
Differential AC Level Input Crosspoint Voltage	*3	$V_{X (AC)}$	V_{CCQ}/2 - 0.2	V_{CCQ}/2	V_{CCQ}/2 + 0.2	V
Differential Input Signal Offset Voltage	*4	$V_{ISO (AC)}$	V_{CCQ}/2 - 0.2	V_{CCQ}/2	V_{CCQ}/2 + 0.2	V
Termination Resistor (SSTL I/Os)	*2	R_T	—	50	—	Ω
Ambient Temperature		T_A	0	—	70	°C



Notes: *1. V_{REF} is expected to track variations in the DC level of V_{CCQ} of the transmitting device. Peak-to-Peak noise level on V_{REF} may not exceed +/- 2% of the supplied DC value.

*2. V_{TT} is used for SSTL_2 bus and is not applied to the device. V_{TT} is expected to be set equal to V_{REF} and must be track variations in the DC level of V_{REF}.

*3. Applicable when signal(s) is terminated to the V_{TT} of SSTL_2 bus.

*4. V_{ISO} means {$V_{IN(CLK)}$ + $V_{IN(\overline{CLK})}$} / 2. Refer to Differential Input Signal Definition.

*5. Overshoot limit: V_{IH} (max) = 3.6V for pulse width <= 4 ns acceptable, pulse width measured at 50% of pulse amplitude.

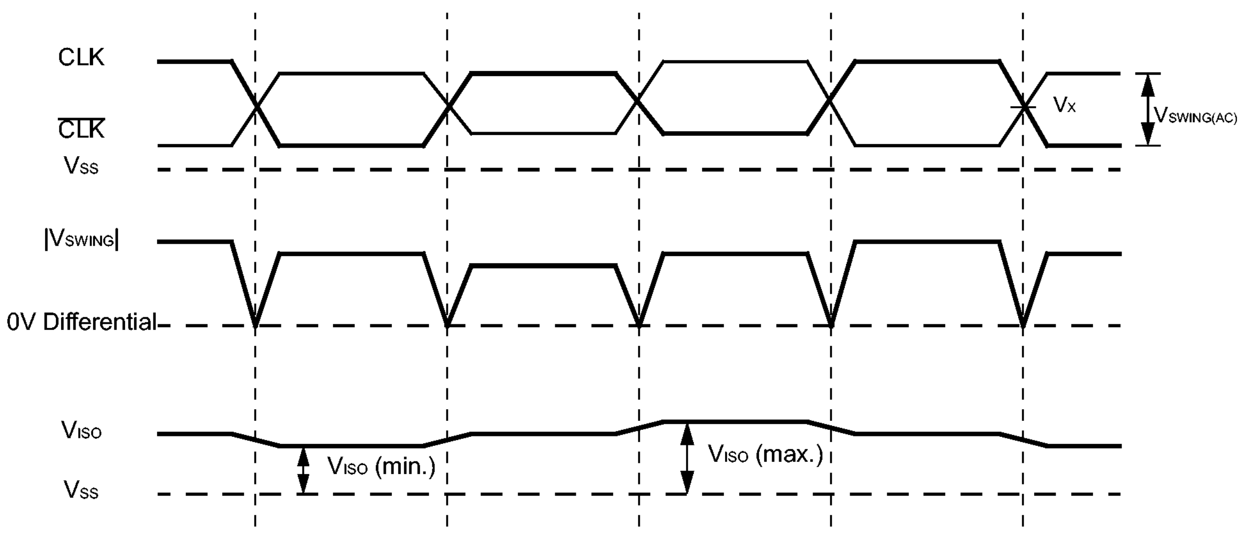
*6. Undershoot limit: V_{IL} (min) = V_{CC} -1.0V for pulse width <= 4 ns acceptable, pulse width measured at 50% of pulse amplitude.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges. Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ RECOMMENDED OPERATING CONDITIONS (Continued)

Differential Input Signal Definition

Fig. 4 – Differential Input Signal Offset Voltage (For Clock Input)



■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, Address & Control	C_{IN1}	2	4	pF
Input Capacitance, CLK & $\overline{CLK}$	C_{IN2}	2	4	pF
Input Capacitance, DML/DMU	C_{IN3}	4	7	pF
I/O Capacitance	$C_{I/O}$	4	7	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note *1,*2,*3

Parameter		Symbol	Condition	Value Min.	Value Max.	Unit
Output Minimum Source DC Current		$I_{OH(DC)}$	V_{CCQ} = 2.3V, V_{OH} = V_{CCQ}-0.43V	-15.2	—	mA
Output Minimum Sink DC Current		$I_{OL(DC)}$	V_{CCQ} = 2.3V, V_{OL} = +0.35V	15.2	—	mA
Input Leakage Current (any input)		I_{LI}	0 V ≤ V_{IN} ≤ V_{CC}; All other pins not under test = 0 V	-10	10	µA
Output Leakage Current		I_{LO}	0 V ≤ V_{IN} ≤ V_{CC}; Data out disabled	-10	10	µA
V_{REF} Current		I_{REF}		-10	10	µA
Operating Current (Average Power Supply Current)	MB81P641647A-10	I_{CC1}	Burst Length = 2 t_{CK} = min, t_{RC} = min for BL = 2 One bank active, Address change up to 3 times during t_{RC} (min) 0 V ≤ V_{IN} ≤ V_{IL} (max), V_{IH} (min) ≤ V_{IN} ≤ V_{CC}	—	220	mA
	MB81P641647A-12				185	
Precharge Standby Current (Power Supply Current)		I_{CC2N}	CKE = V_{IH}, t_{CK} = min All banks idle, NOP commands only, Input signals (except to CMD) are changed one time during 20 ns 0 V ≤ V_{IN} ≤ V_{IL} (max), V_{IH} (min) ≤ V_{IN} ≤ V_{CC}	—	65	mA
Precharge Power Down Current (Power Supply Current)		I_{CC2P}	CKE = V_{IL}, t_{CK} = min All banks idle 0 V ≤ V_{IN} ≤ V_{CC}	—	1	mA
Active Standby Current (Power Supply Current)		I_{CC3N}	CKE = V_{IH}, t_{CK} = min Any bank active, NOP commands only, Input signals (except to CMD) are changed one time during 20 ns 0 V ≤ V_{IN} ≤ V_{IL} (max), V_{IH} (min) ≤ V_{IN} ≤ V_{CC}	—	75	mA
Active Power Down Current (Power Supply Current)		I_{CC3P}	CKE = V_{IL}, t_{CK} = min Any bank active 0 V ≤ V_{IN} ≤ V_{CC}	—	30	mA

■ DC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Note *1,*2,*3

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Burst mode Current (Average Power Supply Current)	MB81P641647A-10	I_{CC4}	Burst Length = 4 All-banks active, Gapless data t_{CK} = min 0 V ≤ V_{IN} ≤ V_{IL} (max), V_{IH} (min) ≤ V_{IN} ≤ V_{CC}	—	390	mA
	MB81P641647A-12				340	
Refresh Current (Average Power Supply Current)	MB81P641647A-10	I_{CC5}	Auto-refresh; t_{CK} = min, t_{RC} = min 0 V ≤ V_{IN} ≤ V_{IL} (max), V_{IH} (min) ≤ V_{IN} ≤ V_{CC}	—	260	mA
	MB81P641647A-12				240	
Self-refresh Current (Average Power Supply Current)		I_{CC6}	Self-refresh; CKE = V_{IL}, 0 V ≤ V_{IN} ≤ V_{CC}	—	2	mA

Notes: *1. All voltages referenced to V_{SS}.

*2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.

*3. I_{CC} depends on the output termination or load conditions, clock cycle rate, and number of address and command change within certain period.
The specified values are obtained with the output open and no termination register.

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note *1,*2,*3

AC PARAMETERS (CAS LATENCY DEPENDENT)

Parameter	Symbol		- 10		- 12		Unit
			Min.	Max.	Min.	Max.	
Clock Period	t_{CK}	CL = 2.5	8.0	12.0	10.0	14.0	ns
		CL = 2.0	10.0	14.0	12.0	14.0	

Parameter	Notes	Symbol	t_{CK} = 8ns		t_{CK} = 10ns		t_{CK} = 12ns		t_{CK} = 14ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Setup Time (Except for DQS, DM and DQs)	*4	t_{IS}	1.2	—	1.5	—	1.8	—	2.1	—	ns
Input Hold Time (Except for DQS, DM and DQs)	*4	t_{IH}	1.2	—	1.5	—	1.8	—	2.1	—	ns
DM and Data Input Setup Time	*5	t_{DS}	0.6	—	0.8	—	0.9	—	1.2	—	ns
DM and Data Input Hold Time	*5	t_{DH}	0.6	—	0.8	—	0.9	—	1.2	—	ns
DQS First Input Setup Time (Input Preamble Setup Time)	*4	t_{DSPRES}	0	—	0	—	0	—	0	—	ns
Last Data Output to CKE High Level Hold Time	*4	t_{QCKEH}	0	—	0	—	0	—	0	—	ns
Input Transition Time		t_T	0.5	1.2	0.5	1.5	0.5	1.8	0.5	2.1	ns
Precharge Power Down Exit and Self-refresh Exit Time	*4	t_{PDEX}	3.2	—	4.0	—	4.8	—	5.6	—	ns
Time between Refresh	*6	t_{REF}	—	64	—	64	—	64	—	64	ms
Time between Auto-refresh Command	*6	t_{AREF}	—	15.6	—	15.6	—	15.6	—	15.6	us

■ AC CHARACTERISTICS (continued)

AC PARAMETERS (FREQUENCY DEPENDANT) Note *7

Parameter	Notes	Symbol	Min.	Max.	Unit
Clock High Time	*4	t_{CH}	0.45 * t_{CK}	—	ns
Clock Low Time	*4	t_{CL}	0.45 * t_{CK}	—	ns
DQS Low to High Input Transition Setup Time from CLK	*4, *8	t_{DQSS}	0.75 * t_{CK}	1.25 * t_{CK}	ns
DQS Low Input Pulse Width		t_{DSL}	0.4 * t_{CK}	—	ns
DQS High Input Pulse Width		t_{DSH}	0.4 * t_{CK}	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	*4	t_{DSPREH}	0.25 * t_{CK}	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)		t_{DSPRE}	0.4 * t_{CK}	0.6 * t_{CK}	ns
DQS Last Low Input Hold Time (Input Postamble Hold Time)		t_{DSPST}	0.4 * t_{CK}	—	ns
DQS Access Time from Clock	*4	t_{QSCK}	- 0.1 * t_{CK}	0.1 * t_{CK}	ns
DQS Output Valid Time		t_{QSV}	0.3 * t_{CK}	—	ns
DQS Output in Low-Z (Output Preamble Setup Time)	*4, *9	t_{QSLZ}	- 0.1 * t_{CK}	—	ns
DQS First Low Output Hold Time (Output Preamble Hold Time)	*4	t_{QSPRE}	0.9 * t_{CK}	1.1 * t_{CK}	ns
DQS Last Low Output Hold Time (Output Postamble Hold Time)	*4, *10	t_{QSPST}	0.4 * t_{CK}	0.6 * t_{CK}	ns
DQS Last Low Output in High-Z from CLK or $\overline{CLK}$	*10	t_{QSHZ}	—	0.1 * t_{CK}	ns
DQ Access Time from CLK & $\overline{CLK}$	*4	t_{ACC}	- 0.1 * t_{CK}	0.1 * t_{CK}	ns
DQ Access Time from DQS	*5	t_{QSQ}	- 0.075 * t_{CK}	0.075 * t_{CK}	ns
DQ Output Data Valid Time		t_{DV}	0.3 * t_{CK}	—	ns
DQ Output in Low-Z	*4, *9	t_{LZ}	- 0.1 * t_{CK}	—	ns
DQ Output in High-Z	*4, *10	t_{HZ}	- 0.1 * t_{CK}	0.1 * t_{CK}	ns
Last Data Input to CKE High Level Hold Time		t_{DCKEH}	t_{CK}	—	ns

■ AC CHARACTERISTICS

EXAMPLE OF FREQUENCY DEPENDANT AC PARAMETERS (@ Minimum t_{CK})

Parameter	Notes	Symbol	t_{CK} = 8ns		t_{CK} = 10ns		t_{CK} = 12ns		t_{CK} = 14ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock High Time		t_{CH}	3.6	—	4.5	—	5.4	—	6.3	—	ns
Clock Low Time		t_{CL}	3.6	—	4.5	—	5.4	—	6.3	—	ns
DQS Low to High Input Transition Setup Time from CLK		t_{DQSS}	6.0	10.0	7.5	12.5	9.0	15.0	10.5	17.5	ns
DQS Low Input Pulse Width		t_{DSL}	3.2	—	4.0	—	4.8	—	5.0	—	ns
DQS High Input Pulse Width		t_{DSH}	3.2	—	4.0	—	4.8	—	5.0	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)		t_{DSPREH}	2.0	—	2.5	—	3.0	—	3.5	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)		t_{DSPRE}	3.2	4.8	4.0	6.0	4.8	7.2	5.6	8.4	ns
DQS Last Low Input Hold Time (Postamble Hold Time)		t_{DSPST}	3.2	—	4.0	—	4.8	—	5.6	—	ns
DQS Access Time from Clock		t_{QSCK}	-0.8	0.8	-1.0	1.0	-1.2	1.2	-1.4	1.4	ns
DQS Output Valid Time		t_{QSV}	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Output in Low-Z (Output Preamble)		t_{QSLZ}	-0.8	—	-1.0	—	-1.2	—	-1.4	—	ns
DQS First Low Output Hold Time (Output Preamble)		t_{QSPRE}	7.2	8.8	9.0	11.0	10.8	13.2	12.6	15.4	ns
DQS Last Low Output Hold Time (Output Postamble)		t_{QSPST}	3.2	4.8	4.0	6.0	4.8	7.2	5.6	8.4	ns
DQS Last Low Output in High-Z from CLK or $\overline{CLK}$		t_{QSHZ}	—	0.8	—	1.0	—	1.2	—	1.4	ns
DQ Output Access Time from CLK & $\overline{CLK}$		t_{ACC}	-0.8	0.8	-1.0	1.0	-1.2	1.2	-1.4	1.4	ns
DQ Output Access Time from DQS		t_{QSQ}	-0.6	0.6	-0.8	0.8	-0.9	0.9	-1.1	1.1	ns
DQ Output Data Valid Time		t_{DV}	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQ Output in Low-Z		t_{LZ}	-0.8	—	-1.0	—	-1.2	—	-1.4	—	ns
DQ Output in High-Z		t_{HZ}	-0.8	0.8	-1.0	1.0	-1.2	1.2	-1.4	1.4	ns
Last Data Input to CKE High Level Hold Time		t_{DCKEH}	8.0	—	10.0	—	12.0	—	14.0	—	ns

■ AC CHARACTERISTICS

BASE VALUES FOR CLOCK COUNT/LATENCY (Note *11)

Parameter	Notes	Symbol	MB81P641647A -10		MB81P641647A -12		Unit
			Min.	Max.	Min.	Max.	
$\overline{RAS}$ Cycle Time	*12	t_{RC}	80	—	90	—	ns
$\overline{RAS}$ Active Time		t_{RAS}	50	100000	60	100000	ns
$\overline{RAS}$ Precharge Time		t_{RP}	30	—	30	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	30	—	30	—	ns
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		t_{RRD}	20	—	24	—	ns

LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81P641647A -10	MB81P641647A -12	Unit
BST Command to Output in High-Z	CL = 2.5	l_{BSH}	2.5	2.5	tCK
	CL = 2.0		2.0	2.0	tCK
BST Command to New Command Input *13	CL = 2.5	l_{BSNC}	3.0	3.0	tCK
	CL = 2.0		2.0	2.0	tCK
DM to Input Data Delay		l_{DQD}	0	0	tCK
Read Command to Write Command Delay (minimum)	CL = 2.5	l_{RWD}	BL / 2 + 3	BL / 2 + 3	tCK
	CL = 2.0		BL / 2 + 2	BL / 2 + 2	tCK
Last Input Data to Read Command Delay (minimum)	*14	l_{WRD}	1.5	1.5	tCK
Last Input Data to Precharge Command Lead Time (minimum)	*14	l_{DPL}	1.5	1.5	tCK
Write with AutoPrecharge Command to Active command Delay (minimum)	*14	l_{WAL}	BL / 2 + 2 + t_{RP}	BL / 2 + 2 + t_{RP}	tCK
Precharge to Output in High-Z	CL = 2.5	l_{ROH}	2.5	2.5	tCK
	CL = 2.0		2.0	2.0	tCK
Mode Register Access to Next Command Input Delay (min)		l_{MRD}	2	2	tCK
$\overline{CAS}$ to $\overline{CAS}$ Delay (minimum)		l_{CCD}	1	1	tCK
$\overline{CAS}$ Bank Delay (minimum)		l_{CBD}	1	1	tCK
Precharge Power Down Exit to Next Command Input Delay (minimum)		l_{PDEXP}	2	2	tCK
Active Power Down Exit to Next Command Input Delay (minimum)		l_{PDEXA}	1	1	tCK
Minimum Stable Clock Input After Self-refresh Exit Before Any Command Input*15		l_{SCD}	200	200	tCK
Minimum Stable Clock Input for DLL Lock-on in Power-up Initialization sequence.	$t_{CK} \leq 12$ns	l_{PCD}	300	300	tCK
	$t_{CK} \leq 14$ns		400	400	tCK
CKE Low to Command/Address Input Inactive		l_{CKE}	1	1	tCK

■ AC CHARACTERISTICS (continued)

Notes: *1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure and stable clock input with constant clock period and with 50% duty cycle.

*2. Access Times assume input slew rate of 1ns/volt between V_{REF}+0.35V to V_{REF}-0.35V, where V_{REF} is V_{CCQ}/2, with SSTL_2 output load conditions. Refer to AC TEST LOAD CIRCUIT in page 35.

*3. V_{REF} = 1.25V is a typical reference level for measuring timing of input signals.
Transition times are measured between V_{IH} (min) and V_{IL} (max) unless otherwise noted.
Refer to AC TEST CONDITIONS in page 35.

*4. This parameter is measured from the cross point of CLK and $\overline{CLK}$ input.

*5. This parameter is measured from signal transition point of DQSL/U input crossing V_{REF} level.

*6. Total of 4096 REF command must be issued within t_{REF} (max). t_{AREF} specifies the time between one REF command to next REF command except for a condition where CKE = Low during Self-refresh mode.

*7. Frequency dependent AC parameters are scalable by actual clock period (t_{CK}) and affected by an abrupt change of duty cycle, jitters on clock input, T_A and level of V_{CC} and V_{CCq}. The internal DLL circuit can adjust delay time to change and following level change of V_{CC} and V_{CCq}, (change rate of $T_A \leq 0.1$ °C / 20 ns, change rate of V_{CC} and V_{CCq}, $\leq$ 1mV / 10 ns.
If change rate is bigger than these value, frequency dependent AC parameters affected by jitters causing by these change.)

*8. More than 2 signal edge of DQSL/U should not be input within 1 clock (t_{CK}) cycle.

*9. Low-Z (Low Impedance State) is specified and measured at V_{TT} +/- 400mV.

*10. t_{QSPST}, t_{QSHZ} and t_{HZ} are specified where output buffer is no longer driven.

*11. All base values are measured from the cross point of the rising edge of CLK and falling edge of $\overline{CLK}$ at the command input to the cross point of same clock input condition for the next command input.
All clock counts (= latency) are calculated by a simple formula:

clock count equals base value divided by clock period (round off to a whole number).

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round off a whole number)}$$

*12. Actual clock count of t_{RC} (= l_{RC}) will be sum of clock count of t_{RAS} (= l_{RAS}) and t_{RP} (= l_{RP}).

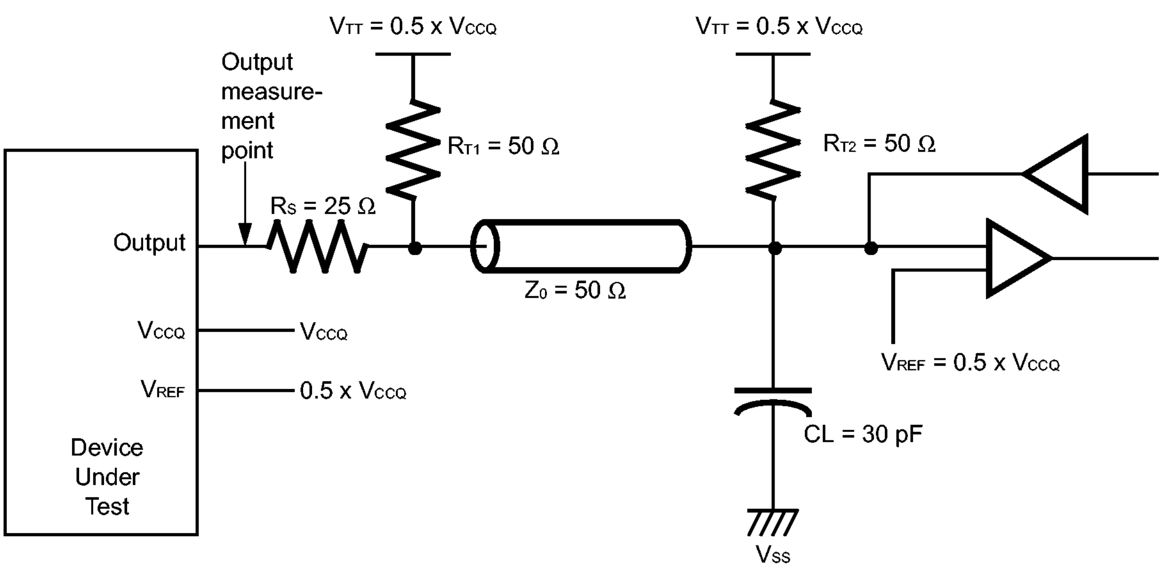
*13. Assume BST is effective to read operation (issued prior to the end of burst read).

14. Assume t_{DQSS} = 1 t_{CK}. If actual t_{DQSS} is within specified minimum and maximum range, those parameters can be assumed t_{DQSS} = 1* t_{CK}.

*15. Applicable also if device operating conditions such as supply voltages, case temperature, and/or clock frequency (t_{CK} difference must be 2 ns and under) is changed during any operation.
Applicable also if any device operating conditions are changed from the previoous operating conditions (at power -down entry) to the present operating conditions (at the power-down exit).

■ AC CHARACTERISTICS (continued)

Fig. 5 – AC TEST LOAD CIRCUIT (SSTL_2, Class II)



Note: AC characteristics are measured in this condition. This load circuit is not applicable for DC Test.

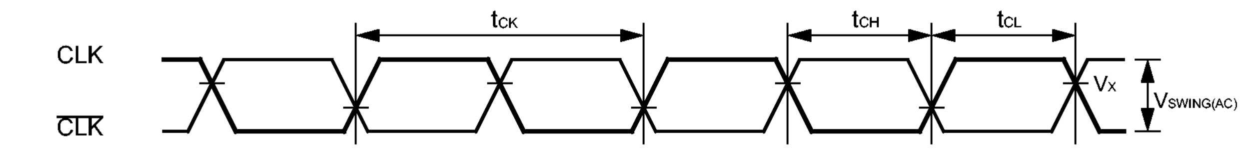
AC TEST CONDITIONS

Parameters	Symbol	Value	Unit
Single-end Input			
Input High Level	V_{IH}	1.6	V
Input Low Level	V_{IL}	0.9	V
Input Reference Level	V_{REF}	1.25	V
Input Slew Rate	SLEW	1.0	V/ns
Differential Input (CLK and $\overline{CLK}$)			
Input Reference Level	Vr	1.25	V
Input Level	V_{SWING}	1.5	V
Input Slew Rate	SLEW	1.0	V/ns

V_X means the actual cross point between CLK and $\overline{CLK}$ input.

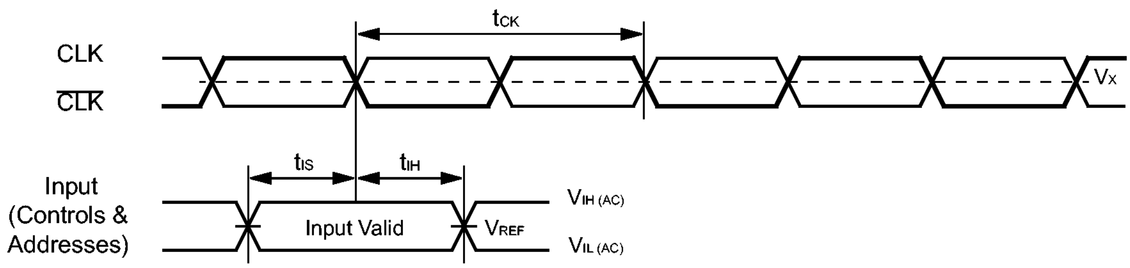
■ AC CHARACTERISTICS (continued)

Fig. 6 – AC TIMING of CLK & $\overline{CLK}$



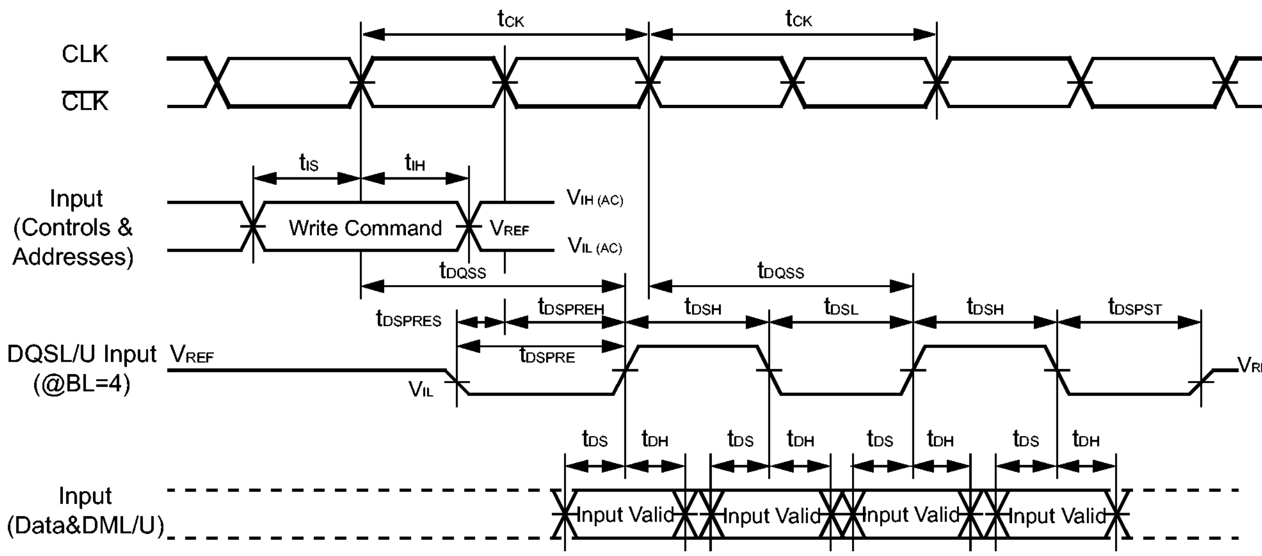
Note: Reference level for AC timings of clock are the cross point of CLK and $\overline{CLK}$ as specified in V_X.

Fig. 7 – AC TIMING of Command Input & Address



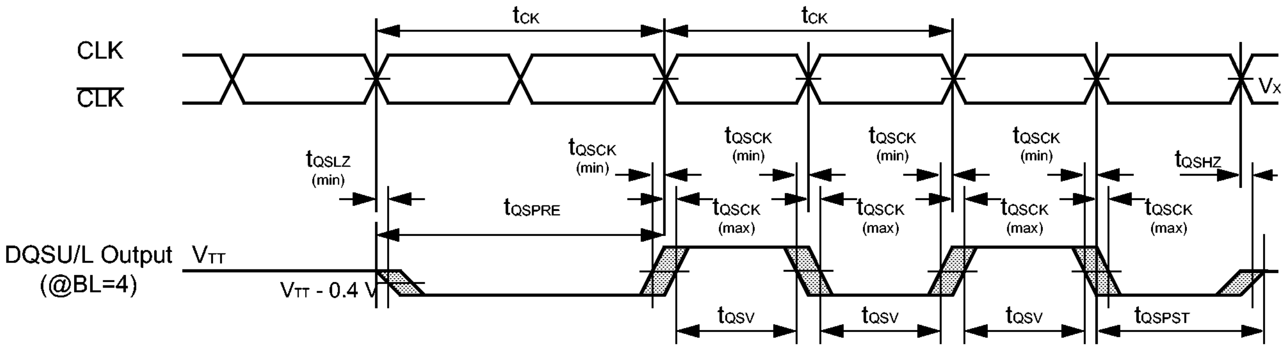
Note: The cross point of CLK and $\overline{CLK}$ (V_X) is used for command and address input.
The reference level of single ended input is V_{REF}.

Fig. 8 – AC TIMING of Write Mode (Data Strobe, Write Data and Data Mask Input)



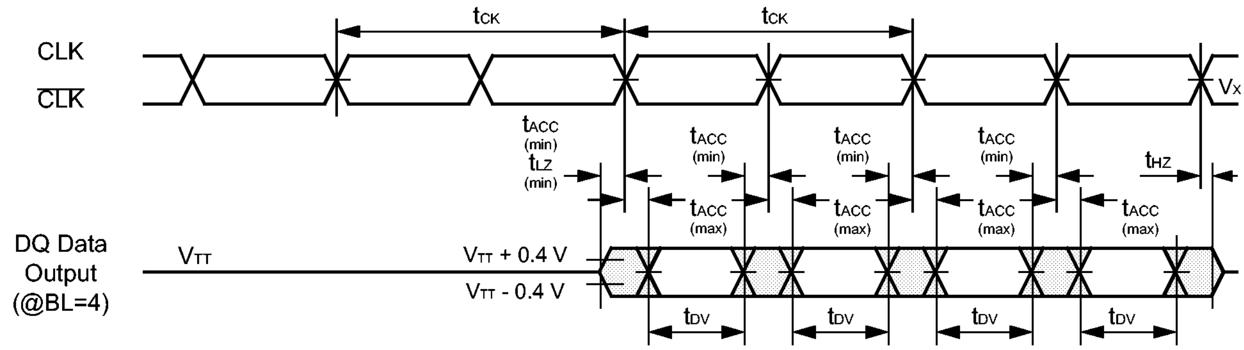
■ AC CHARACTERISTICS (continued)

Fig. 9 – AC TIMING of Read Mode (Clock to DQSL/U Output Delay Time)



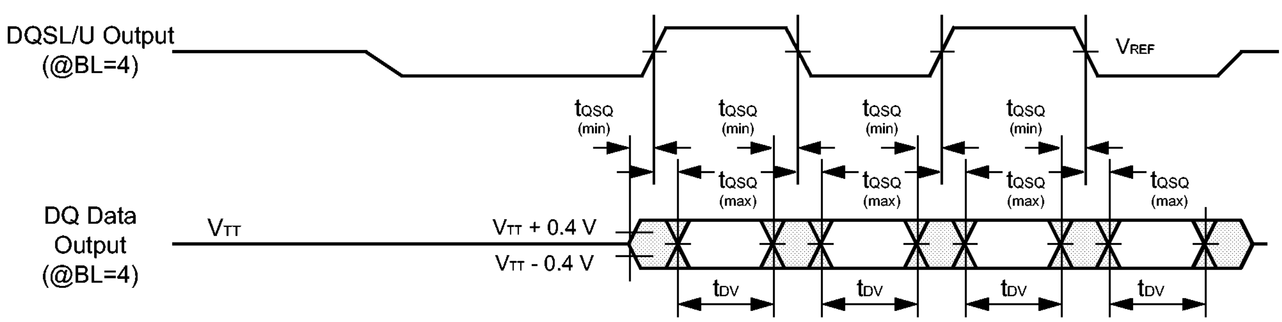
Note: DQS Access time (t_{QSCK}) is measured from the cross point of clock (V_X) and V_{REF}.
The end of t_{QSPST} and t_{QSHZ} specification is defined at where output buffer is no longer driven.

Fig. 10 – AC TIMING of Read Mode (Clock to Data Output Delay Time)



Note: Access time (t_{ACC}) is measured from the cross point of clock (V_X) and V_{REF}.
The end of t_{HZ} specification is defined at where output buffer is no longer driven.

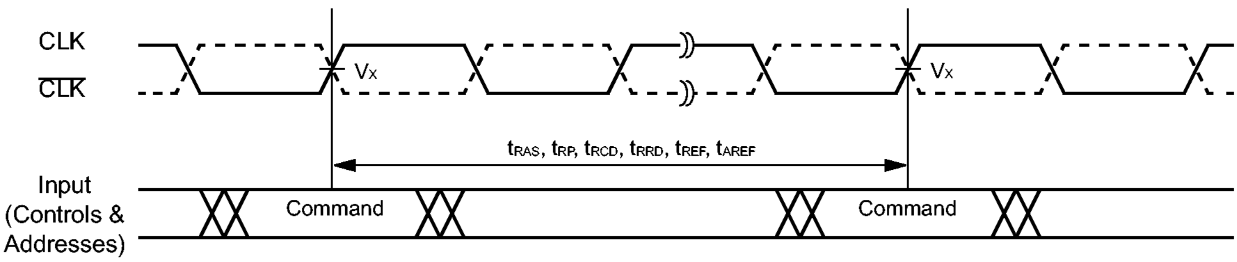
Fig. 11 – AC TIMING of Read Mode (DQSL/U Output to Data Output Delay Time)



Note: DQSU/L Output Edge to Data Output Edge Skew Time (t_{QSQ}) is measured from V_{TT} to V_{TT}.

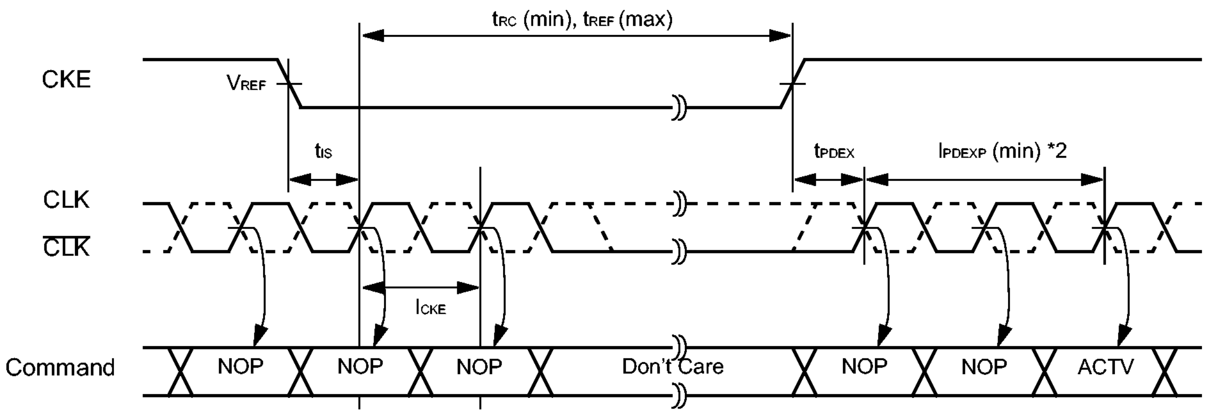
■ AC CHARACTERISTICS (continued)

Fig. 12 – AC TIMING, PULSE WIDTH



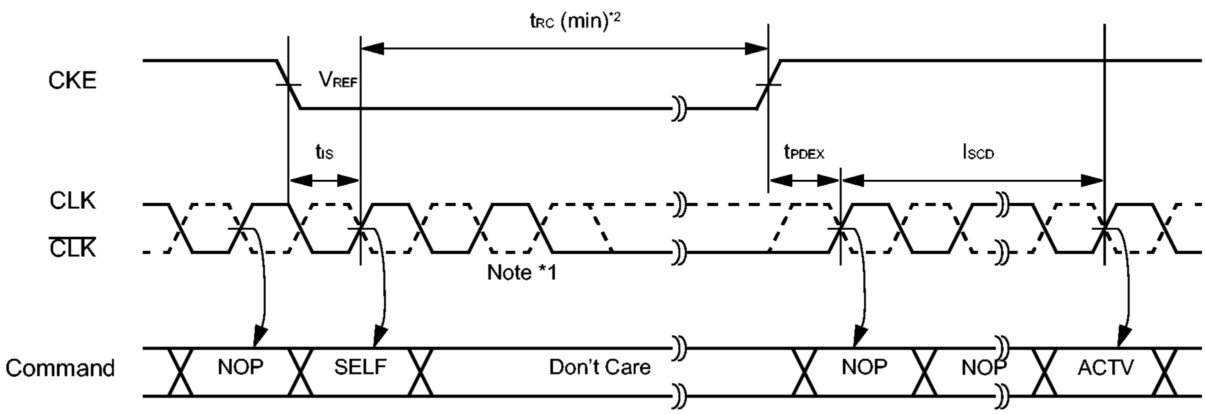
Note: All parameters listed above are measured from the cross point at rising edge of the CLK and falling edge of $\overline{CLK}$ of one command input to next command input.

Fig. 13 – AC TIMING of Precharge Power Down Mode



Note: 1. Minimum 2 clock cycles is required for complete power down on clock buffer.
2. If either any supply voltage or clock input condition is changed from the previous operating condition (other than PDEN and REF), I_{SCD} must be met prior to any command input.

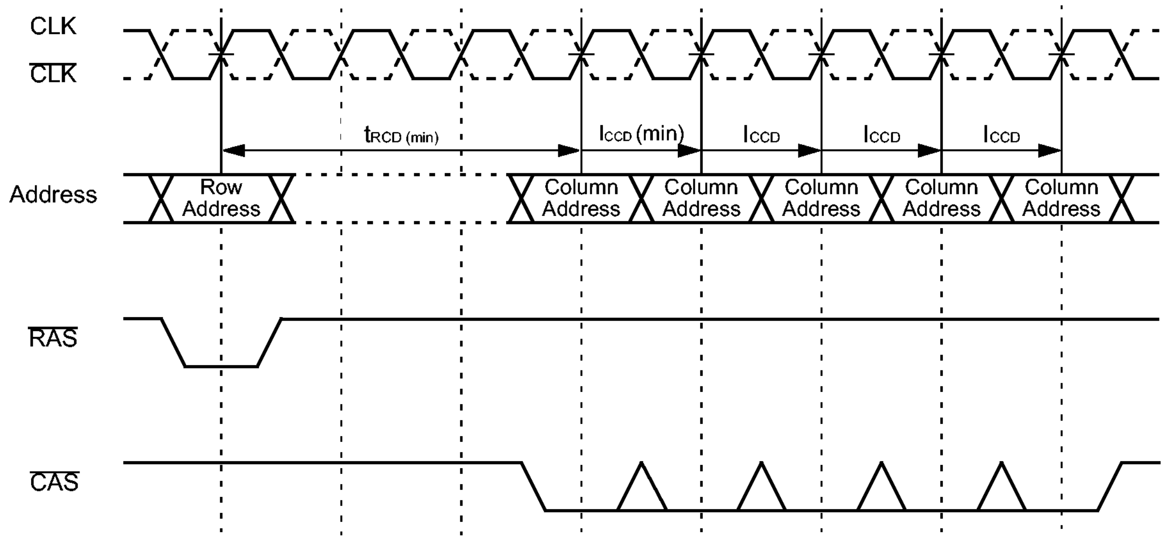
Fig. 14 – AC TIMING of Self-refresh Mode



Note: 1. Minimum 2 clock cycles is required for complete power down on clock buffer.
2. CKE must maintain High level and clock must be provided during the I_{SCD} period. I_{SCD} must be satisfied before any command input.

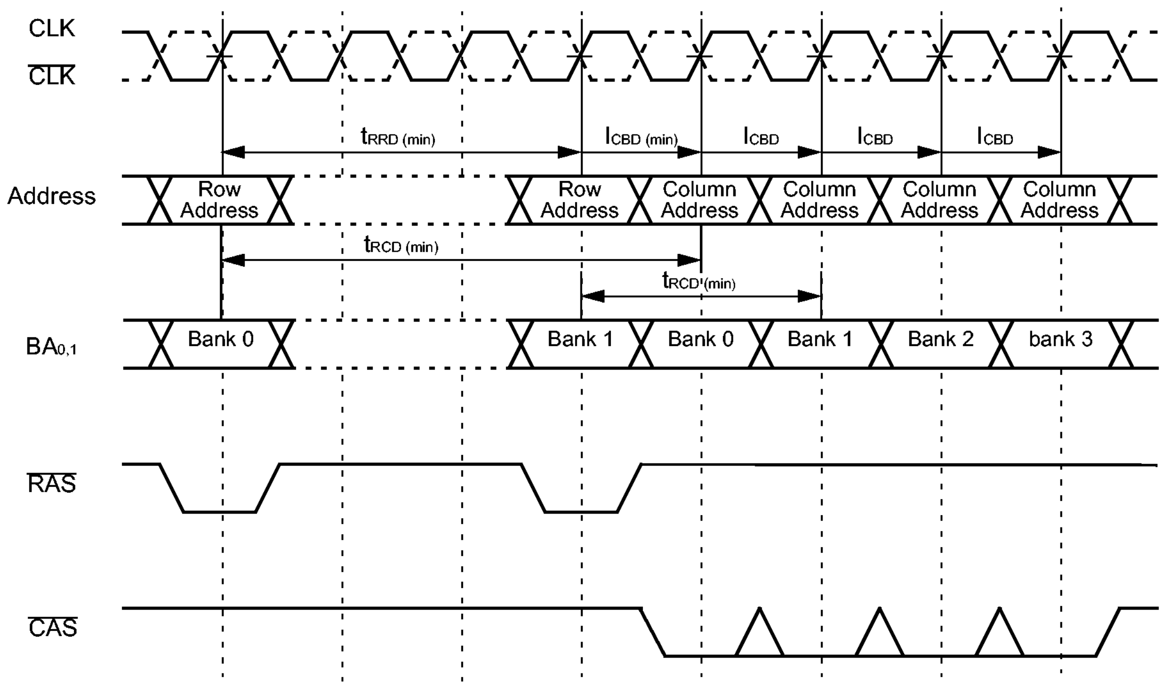
■ TIMING DIAGRAMS

TIMING DIAGRAM – 1 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY

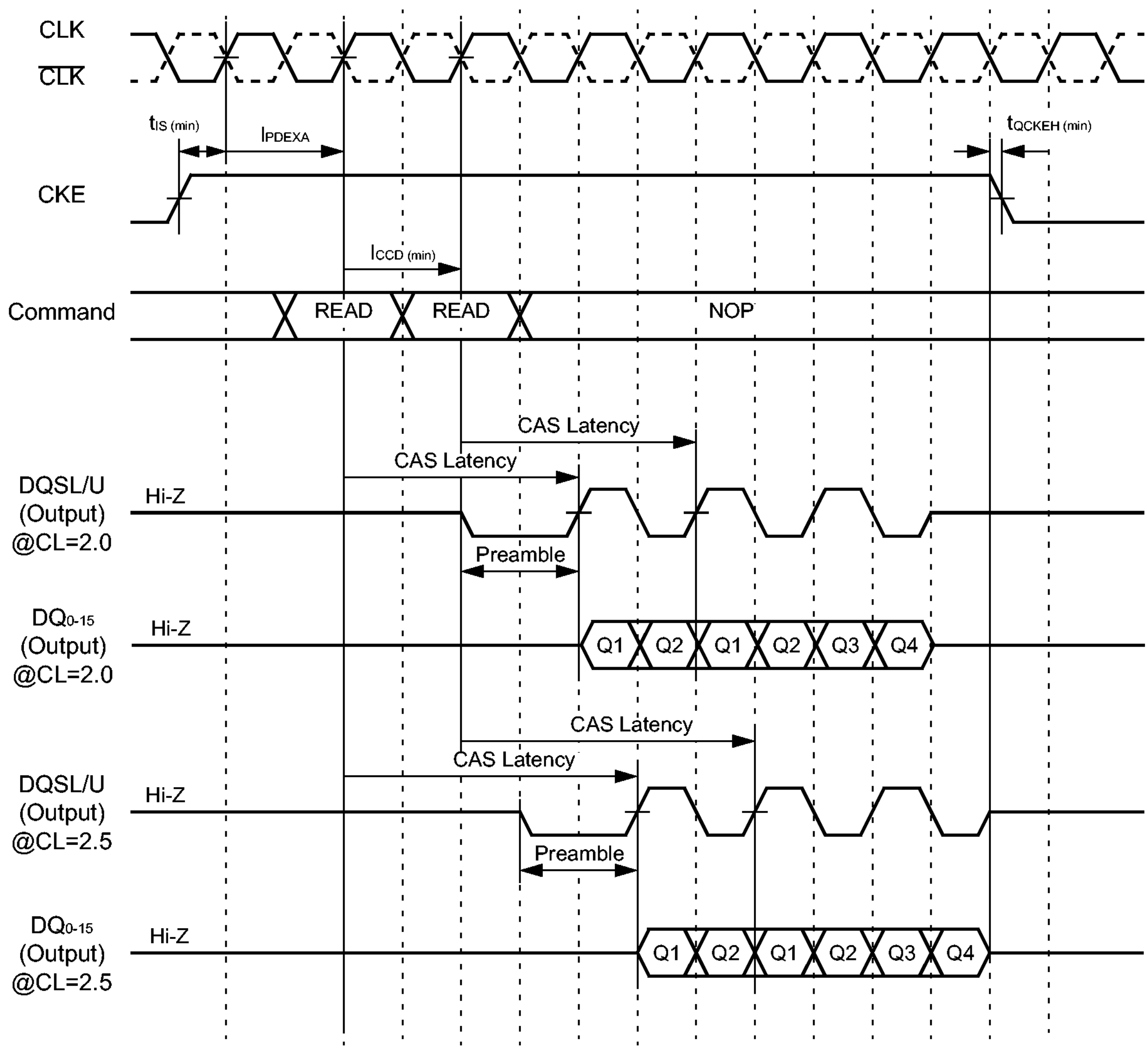


Note: lCCD, CAS to CAS address delay, is applicable to the same bank access and it can be one or more clock period.

TIMING DIAGRAM – 2 : DIFFERENT BANK ADDRESS INPUT DELAY

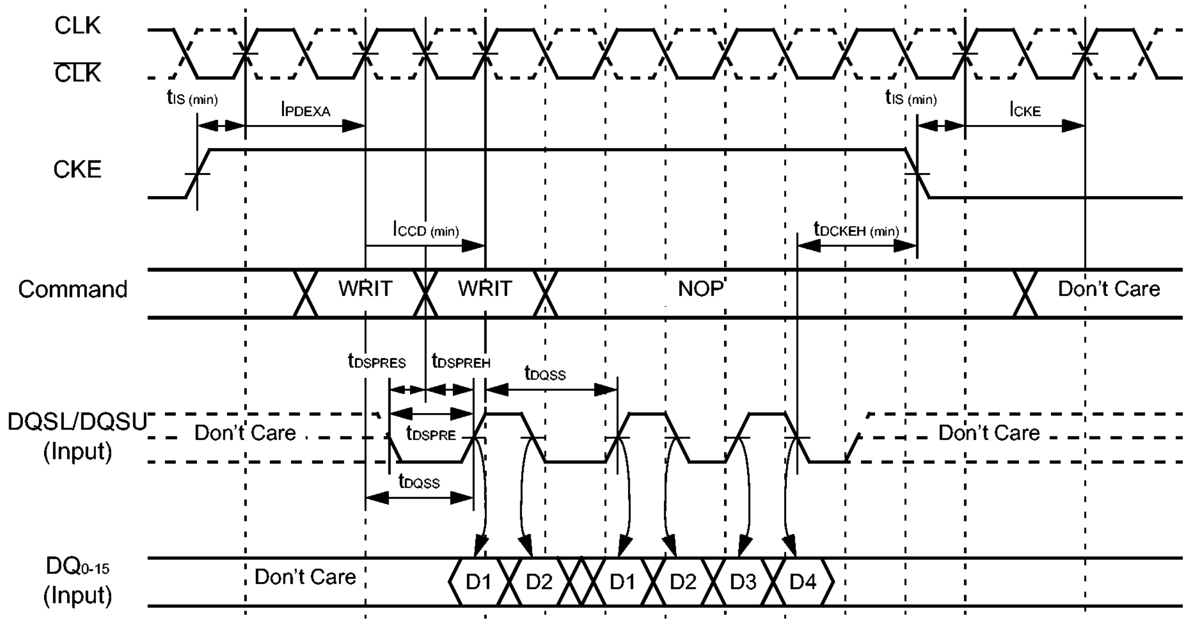


TIMING DIAGRAM – 3 : READ (EXAMPLE @ BL = 4)



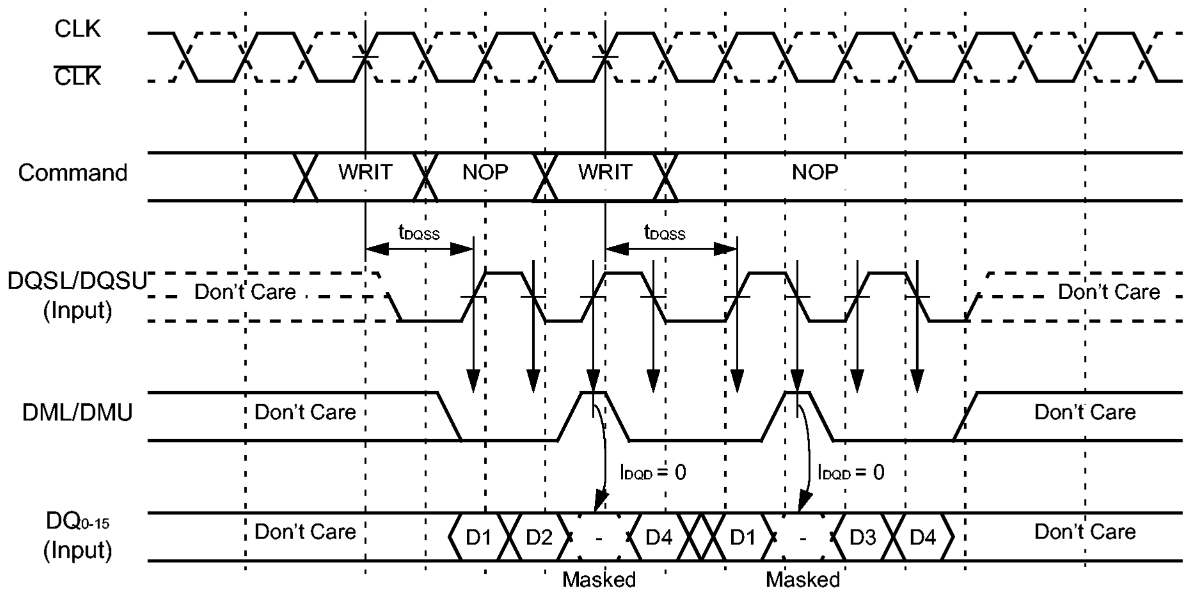
Note: CAS Latency is defined from Read command to first rising edge of DQSL/DQSU output.
Preamble is 1*t_{CK} length and starts driving Low level.

TIMING DIAGRAM – 4 : WRITE (EXAMPLE @ BL = 4)



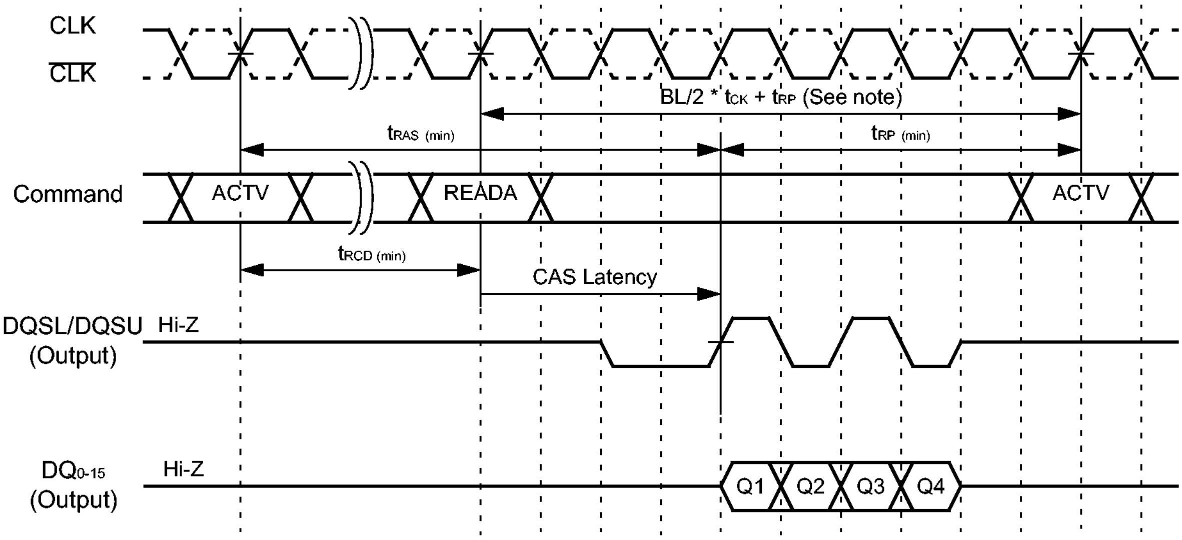
Note: DQSL/DQSU Setup Time, t_{DQSS}, must be within a range of 0.75*t_{CK} to 1.25*t_{CK} from write command

TIMING DIAGRAM – 5 : DML/U, WRITE DATA MASK (EXAMPLE @ BL = 4)



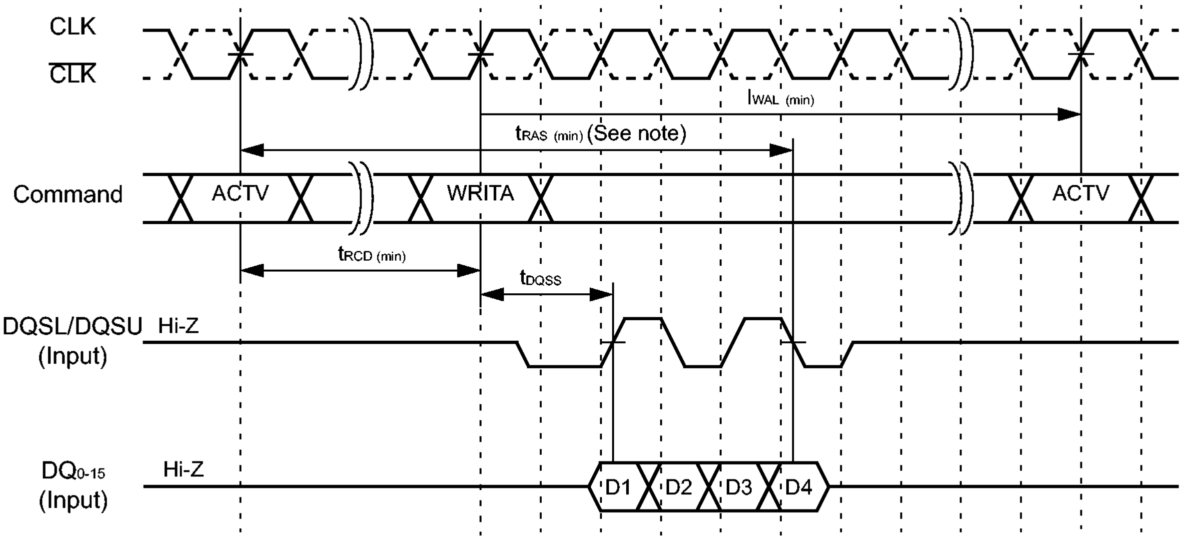
Note: DML/DMU are latched by DQSL/DQSU Input respectively together with Data Input after write

TIMING DIAGRAM – 6 : READ WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4 Applied to same bank)



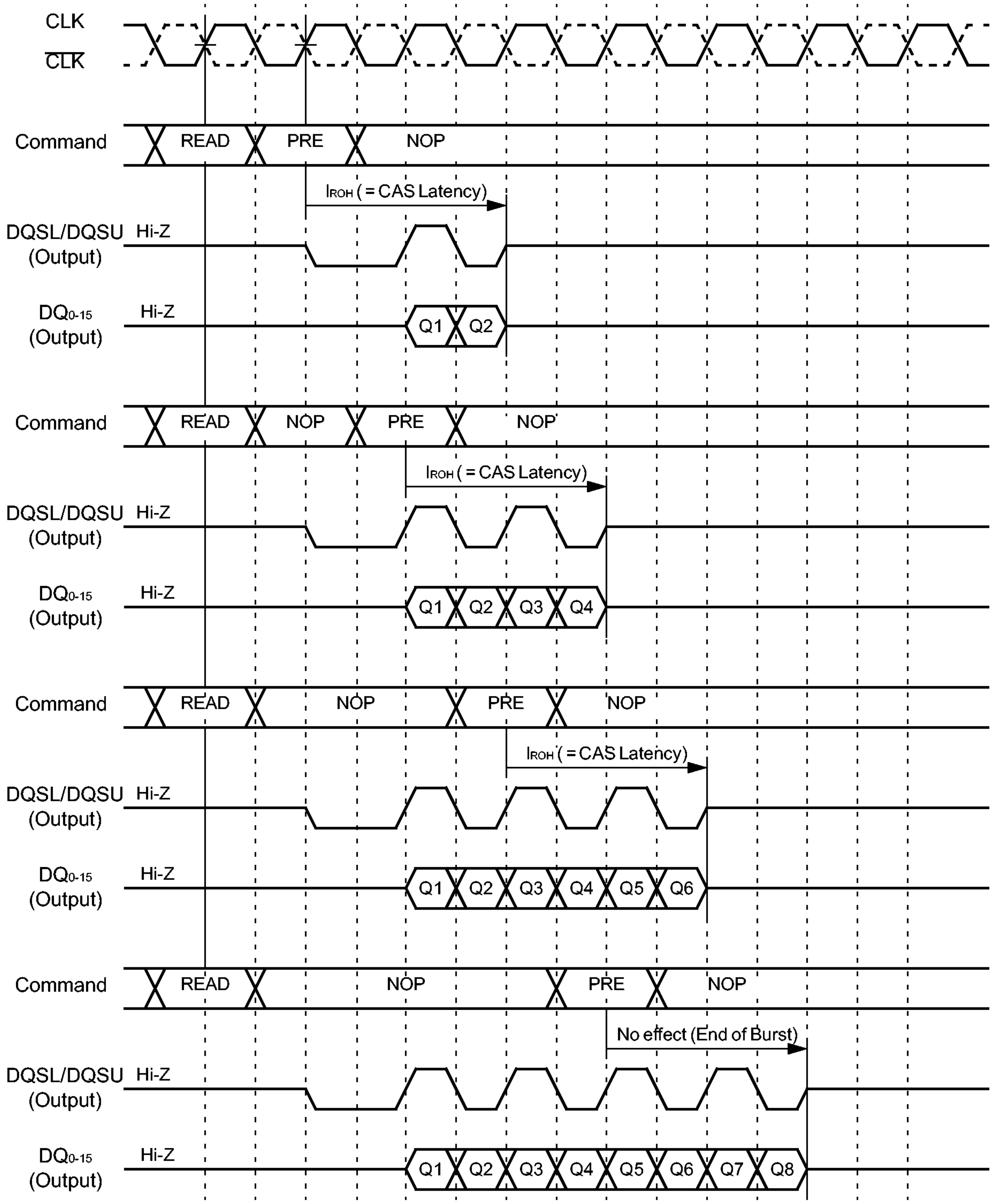
Note: Internal precharge operation at Read with Auto-precharge command (READA) is started BL/2 clock later from READA command.
If BL=2, the READA command should not be issued no earlier than 1 clock (BL/2 = 1) before t_{RAS} (min).

TIMING DIAGRAM – 7 : WRITE WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4 Applied to same bank)



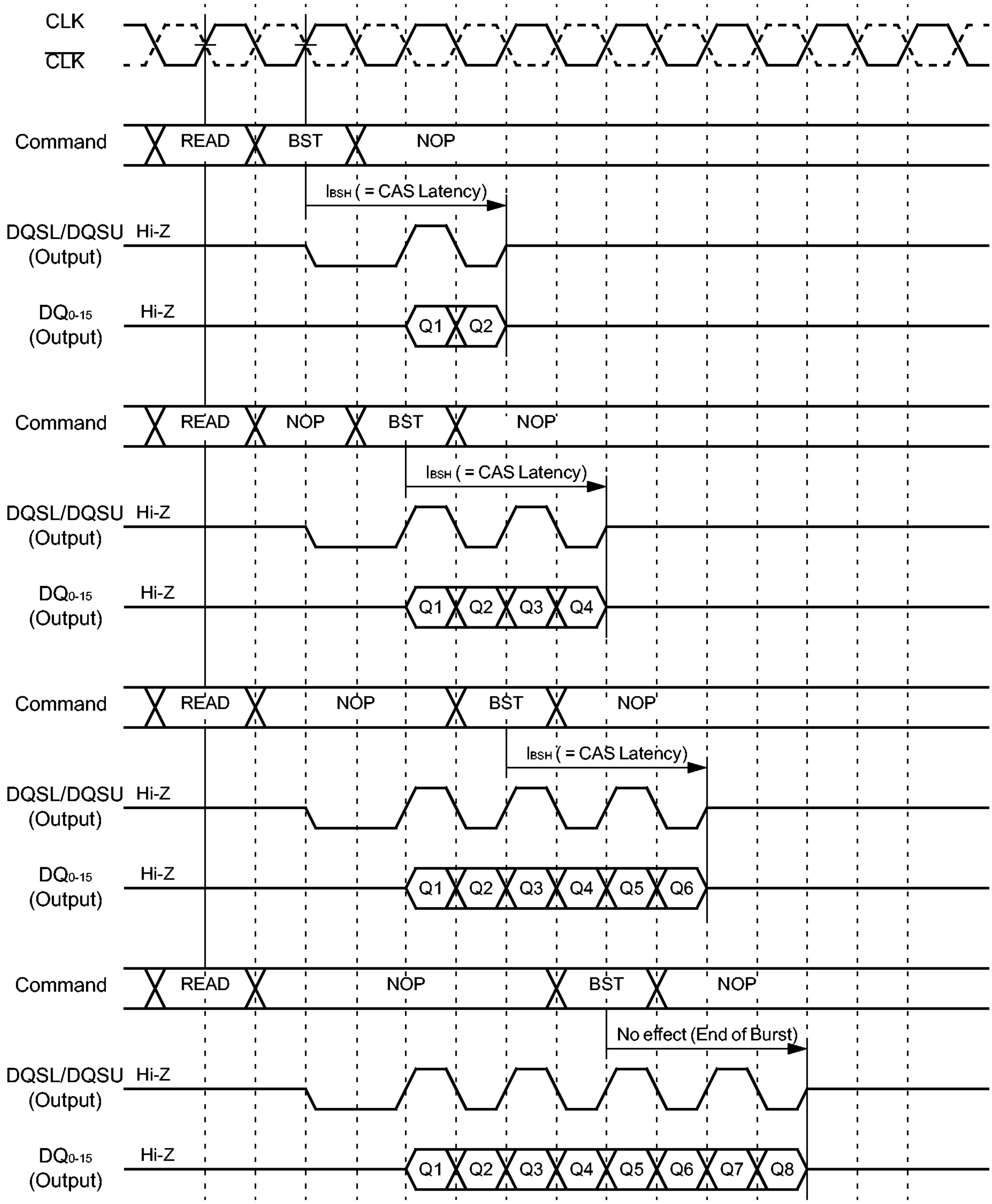
Note: Write with Auto-precharge command (WRITA) must be issued after t_{RCD} is satisfied and be considered to meet t_{RAS} requirement applied to end of burst length (BL) regardless of where it is masked or not.

TIMING DIAGRAM – 8 : READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 8)



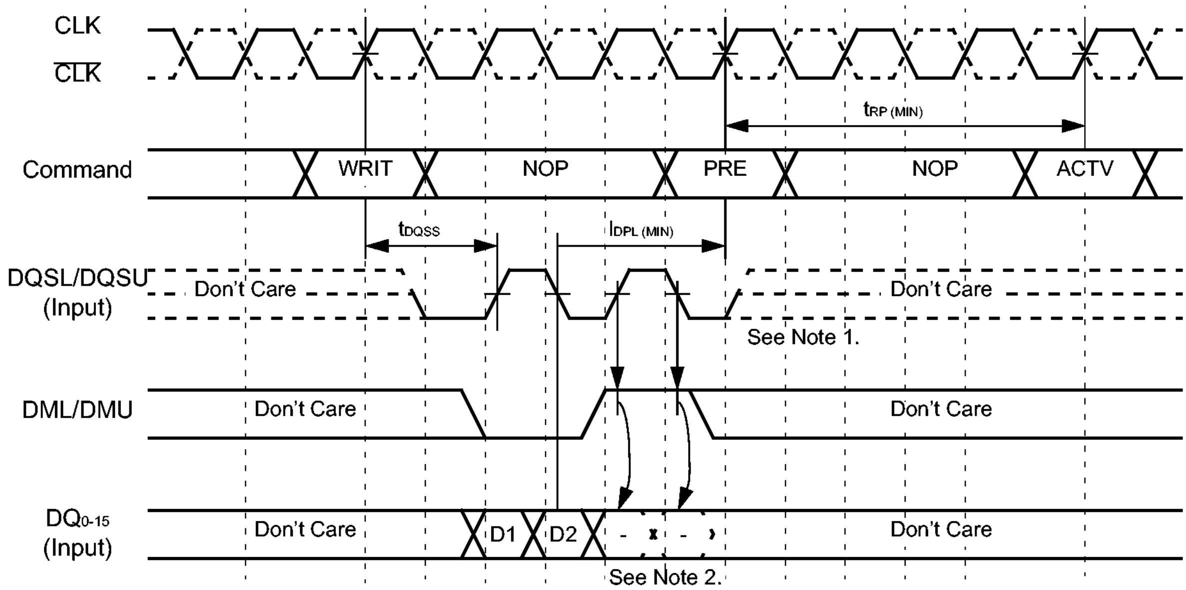
Note: l_{ROH} is the same as CAS Latency (CL). In case of CL =2.5, the l_{ROH} is 2.5 clock.

TIMING DIAGRAM – 9 : READ INTERRUPTED BY BURST STOP
(EXAMPLE @ CL = 2, BL = 8)



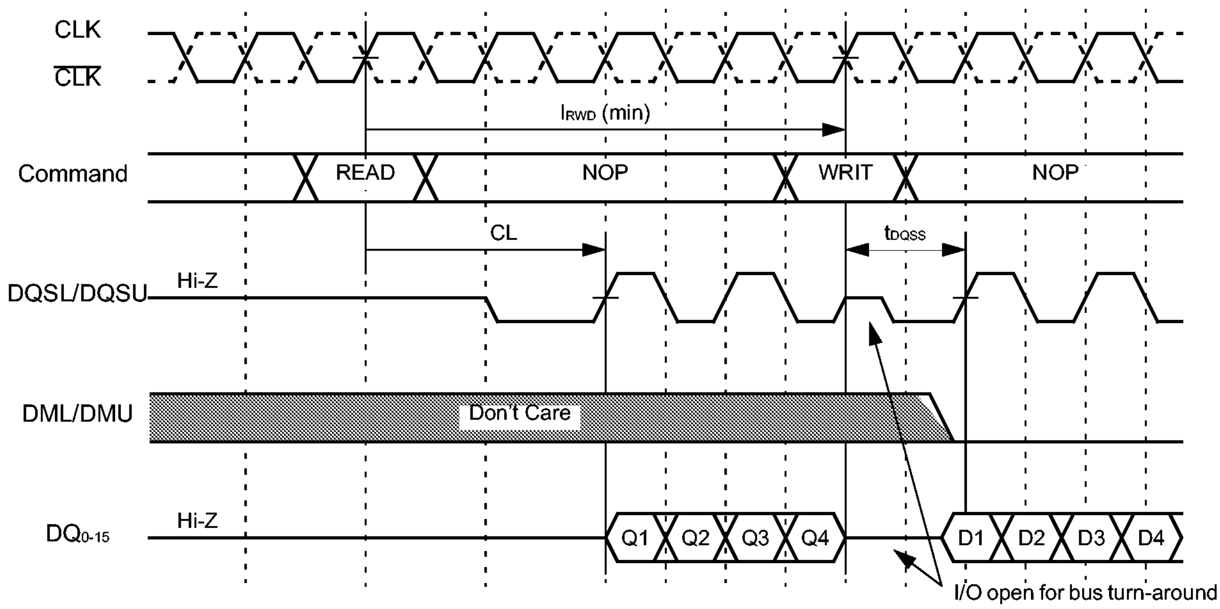
Note: lBSH is the same as CAS Latency (CL). In case of CL =2.5, the lBSH is 2.5 clock.

TIMING DIAGRAM – 10 : WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4)



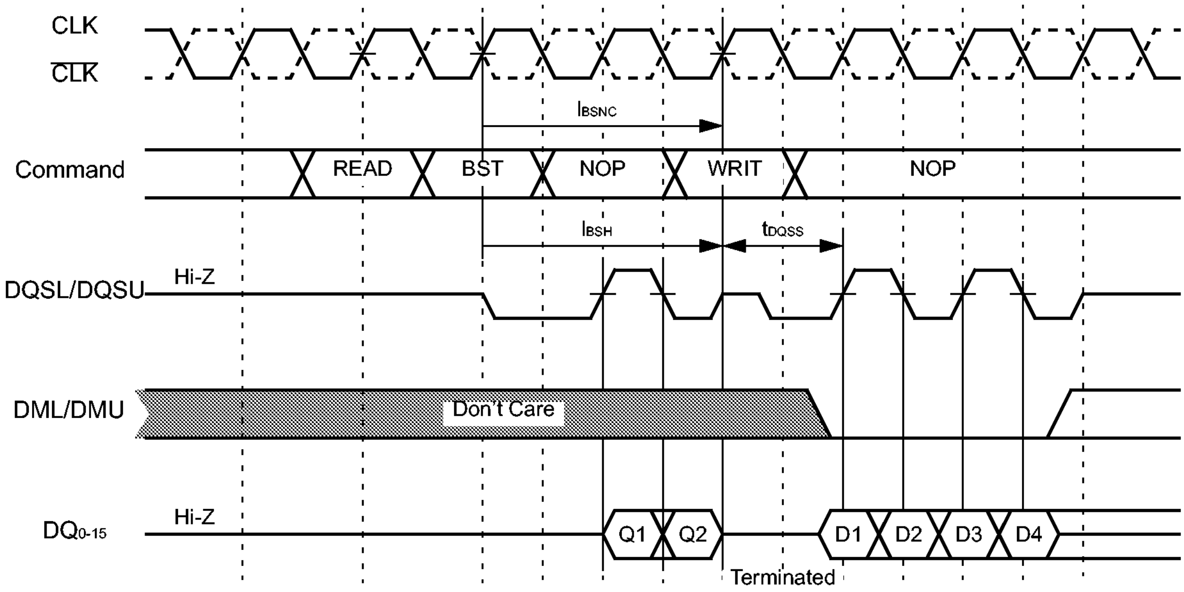
Note: 1. DQSL/DQSU Input are not required from when Precharge command is issued.
2. This pair of write data must be masked prior to Precharge command.

TIMING DIAGRAM – 11 : READ TO WRITE (EXAMPLE @ CL = 2, BL = 4)



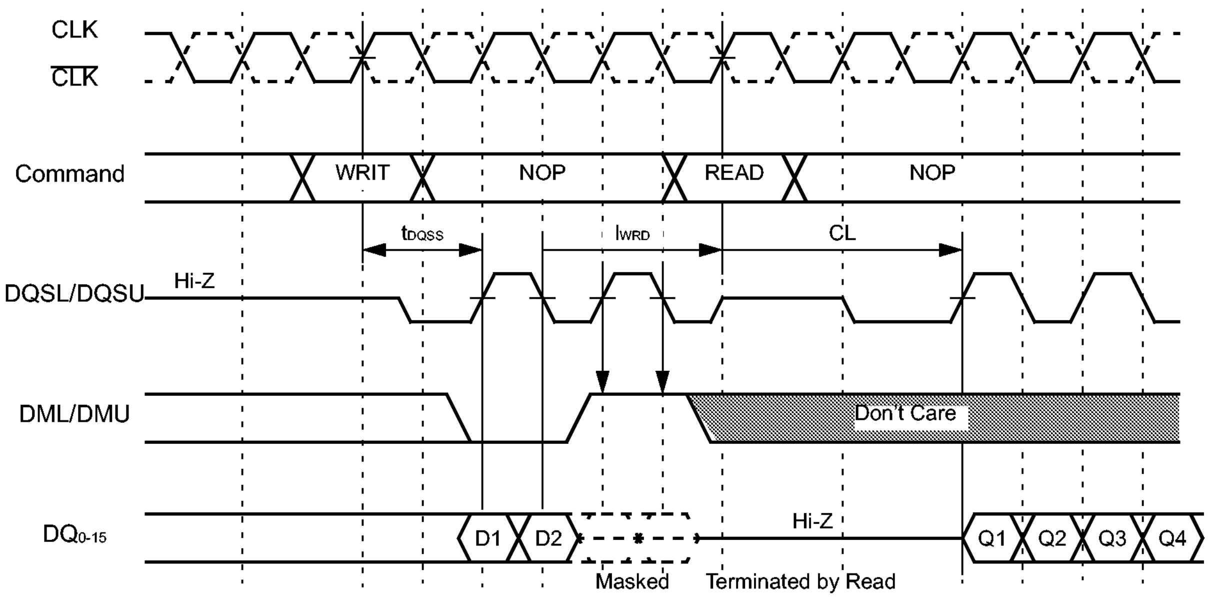
Note: lRWD defines a minimum delay from Read to Write command input applied to the same bank.

TIMING DIAGRAM – 12 : READ TO WRITE (EXAMPLE @ CL = 2, BL = 4)



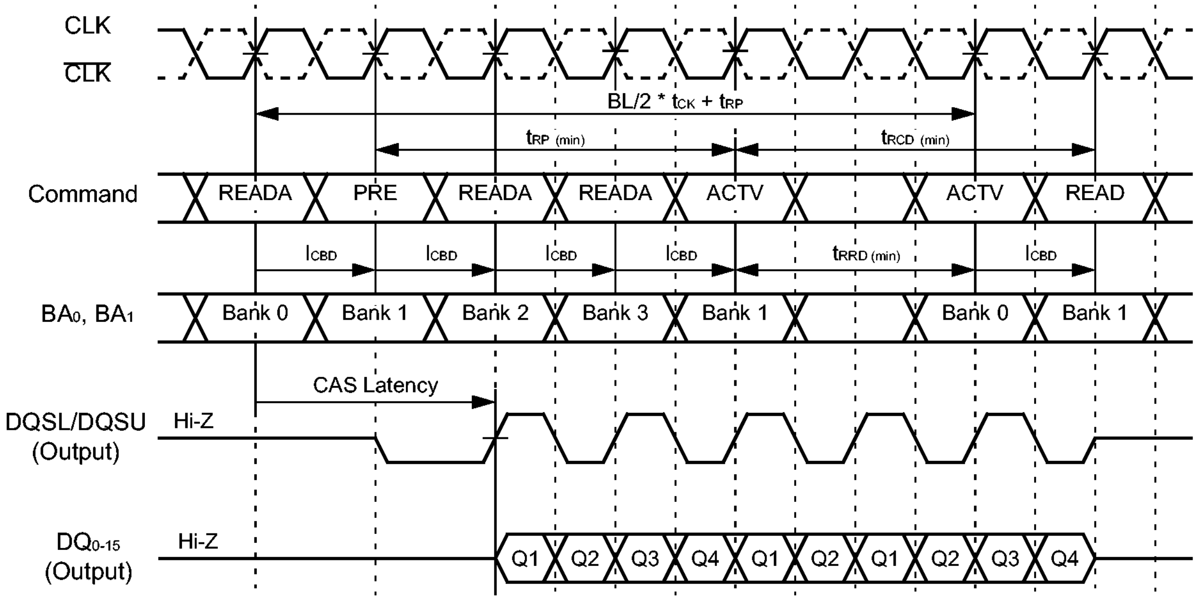
Note: DML/DMU are latched by DQSL/DQSU Input respectively after Write command together with

TIMING DIAGRAM – 13 : WRITE TO READ (EXAMPLE @ CL = 2, BL = 8)



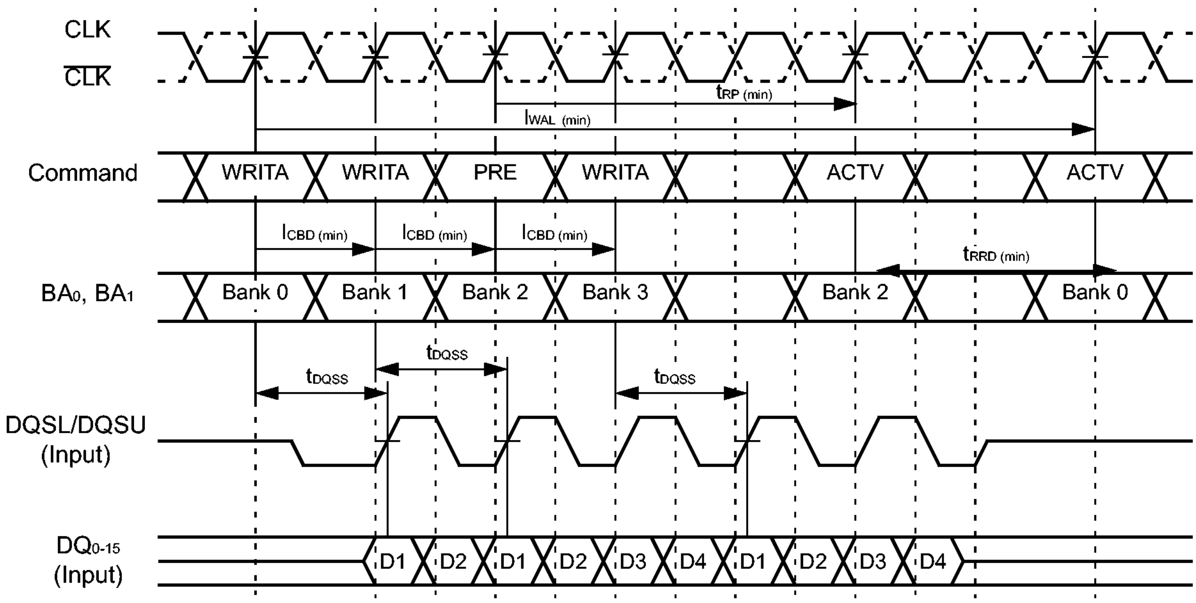
Note: Read command must be issued after l_{WRD} is satisfied and proceeding pair of data must be masked.

TIMING DIAGRAM – 14 : READ WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4, Multiple Bank Operation)



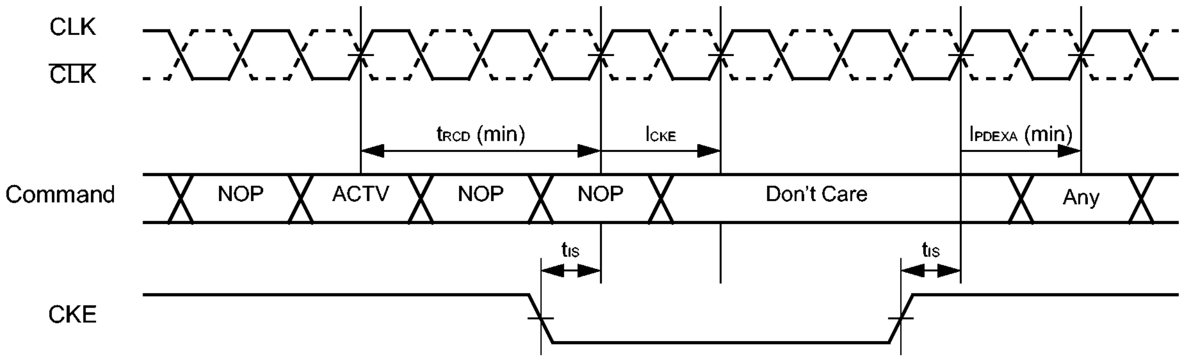
Note: Back to back Read with Auto-precharge (READA) command to the different bank in active state is possible. However, any new command to the same bank applied READA command can only be issued after BL/2*t_{CK}+t_{RP}.

TIMING DIAGRAM – 15 : WRITE WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4, Multiple Bank Operation)



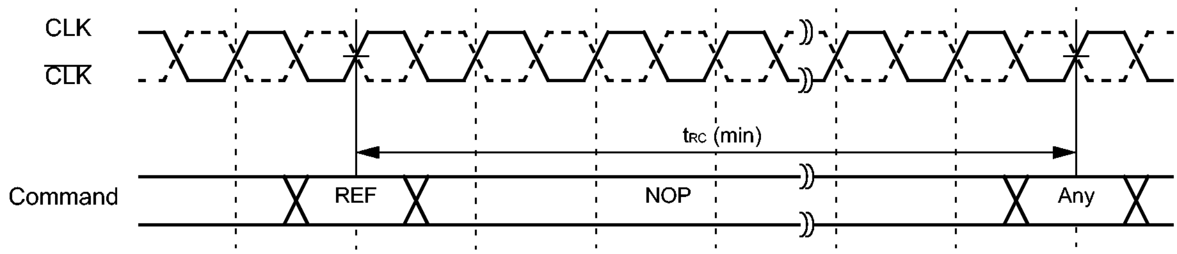
Note: Back to back Write with Auto-precharge (WRITA) command to the different bank in active state is possible. However, any new command to the same bank applied WRITA command can only be issued after l_{DAL}.

TIMING DIAGRAM – 16 : ACTIVE POWER DOWN ENTRY & EXIT

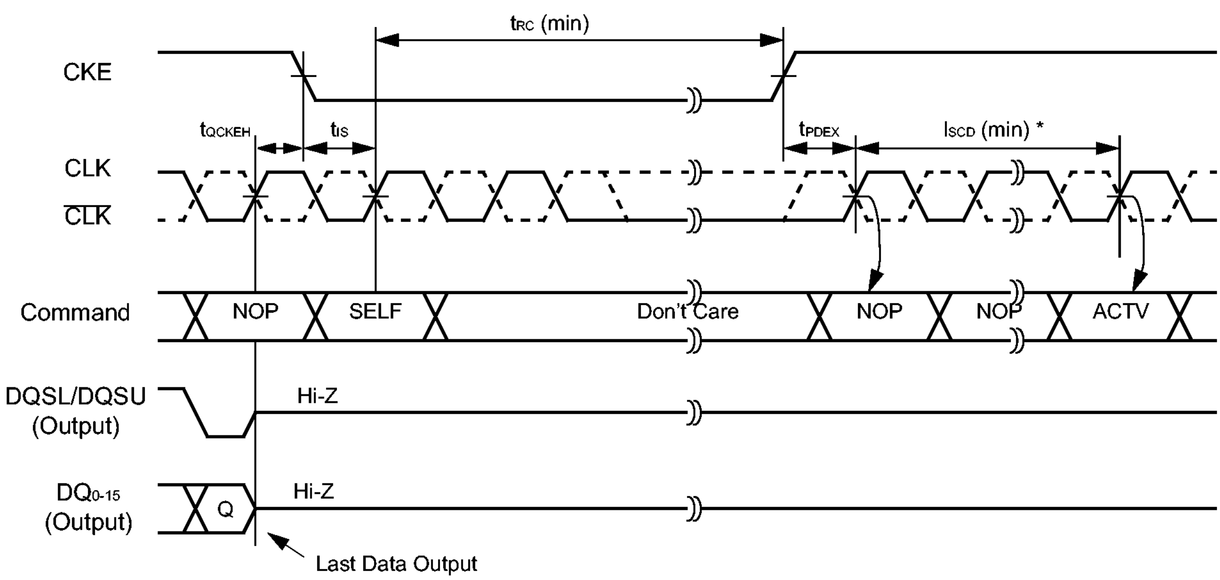


Note: Active power down mode can be entered after t_{RCD} is satisfied and while device is not being accessed.

TIMING DIAGRAM – 17 : AUTO-REFRESH ENTRY AND EXIT

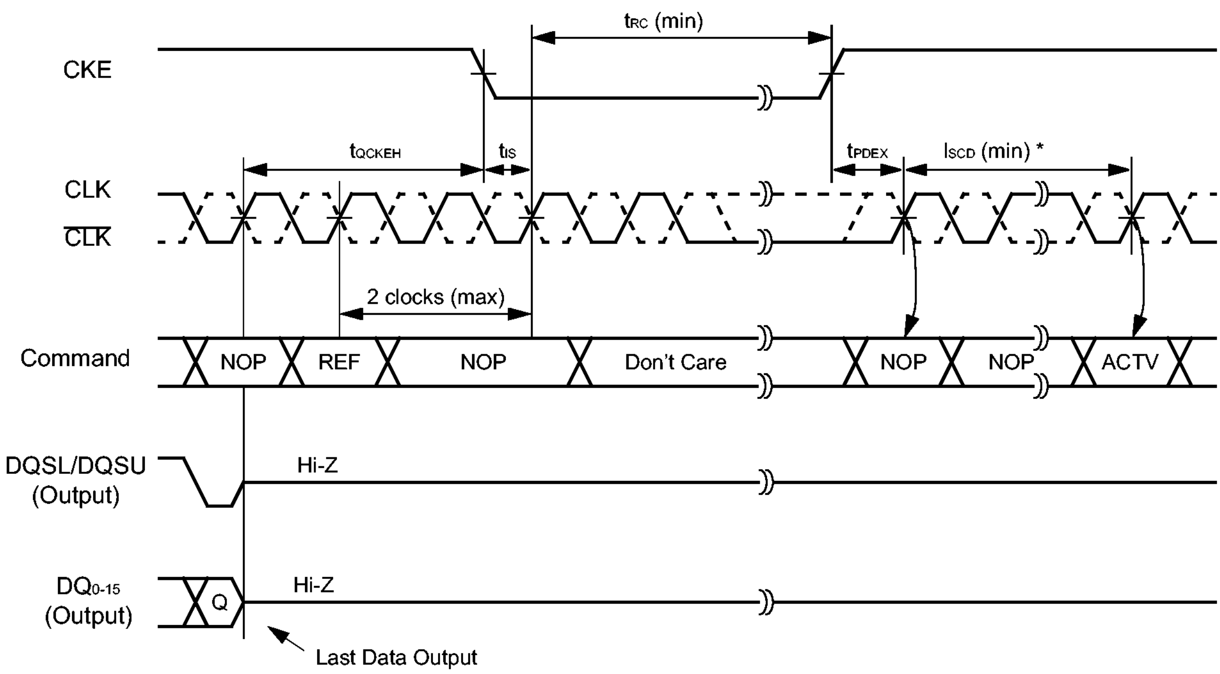


TIMING DIAGRAM – 18 : REGULAR SELF-REFRESH ENTRY AND EXIT



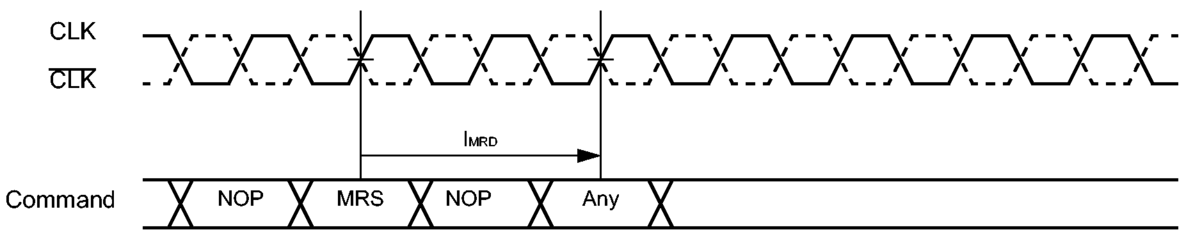
Note: CKE must maintain High level and Clock must be provided during the l_{SCD} period.
After Self-refresh exit, a stable clock must be provided for at least specified l_{SCD} period before any command is issued.

TIMING DIAGRAM – 19 : DELAYED SELF-REFRESH ENTRY AND EXIT



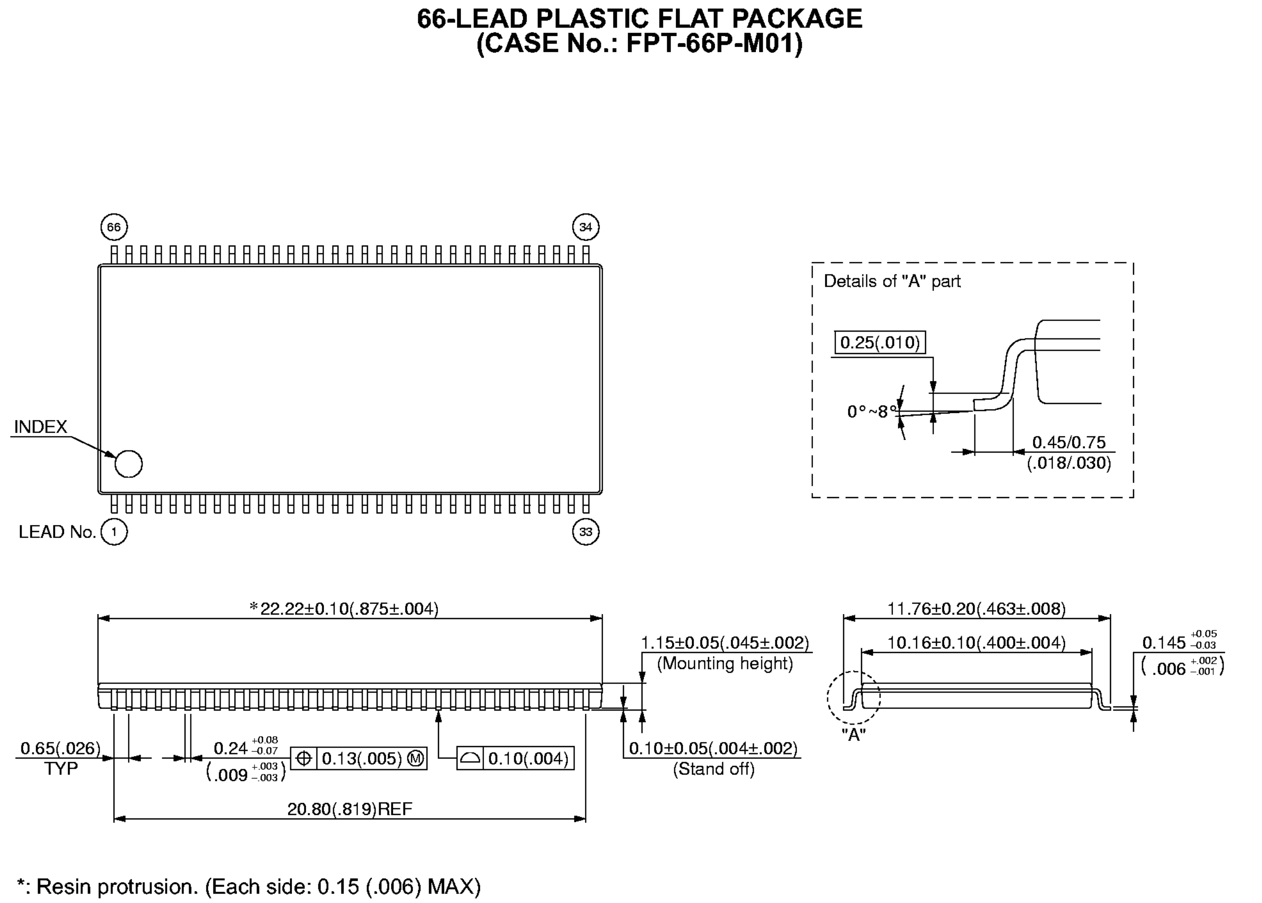
Note: Delayed Self-refresh mode can be entered if CKE is brought to Low within 2 clock cycles after the Auto-refresh command. If the assertion of CKE does not satisfy the 2 clock cycles, the device may enter either active power down or precharge power down mode.
CKE must maintain High level and Clock must be provided during the l_{SCD} period.
After Self-refresh exit, a stable clock must be provided for at least specified l_{SCD} period before any command is issued.

TIMING DIAGRAM – 20 : MODE REGISTER SET



Note: MRS command must be issued after the last data is appeared on each DQ.

■ PACKAGE DIMENSIONS



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