

7492, LS92 Counters

Divide-By-Twelve Counter Product Specification

Logic Products

DESCRIPTION

The '92 is a 4-bit, ripple-type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7492	28MHz	28mA
74LS92	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7492N, N74LS92N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

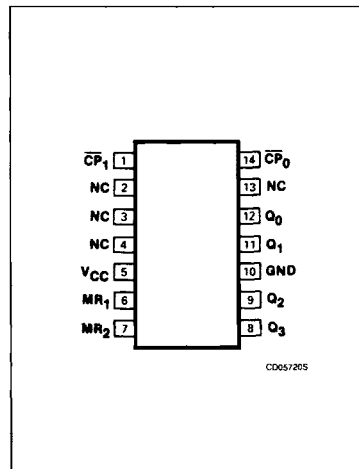
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
MR	Master reset inputs	1ul	1LSul
CP ₀	Input	2ul	6LSul
CP ₁	Input	4ul	8LSul
Q ₀ - Q ₃	Outputs	10ul	10LSul

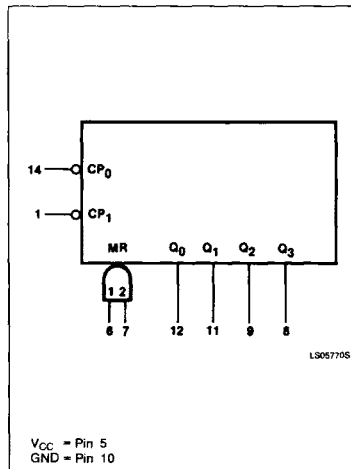
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

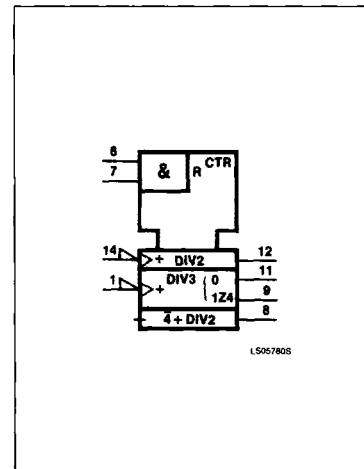
PIN CONFIGURATION



LOGIC SYMBOL



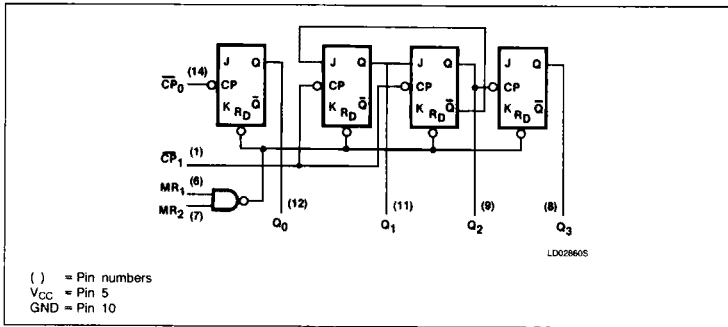
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count and Q_3 produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The \overline{CP}_1 input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

NOTE:

Output Q_0 connected to input \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

NOTE:

V_{IN} is limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs only on the 74LS92.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		7492			74LS92			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V All inputs '92			1.0				mA	
		V _I = 7.0V MR inputs					0.1		mA	
		V _I = 5.5V	\overline{CP}_0 input					0.2		mA
			\overline{CP}_1 input					0.4		mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	MR inputs		40				μ A	
			\overline{CP}_0 input		80				μ A	
			\overline{CP}_1 input		160				μ A	
		V _I = 2.7V	MR inputs					20		μ A
			\overline{CP}_0 input ⁵					40		μ A
			\overline{CP}_1 input ⁵					80		μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	MR inputs		-1.6			-0.4	mA	
			\overline{CP}_0 input		-3.2			-2.4	mA	
			\overline{CP}_1 input		-6.4			-3.2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-55	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX				51		9	15	mA	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS92 only is 80 μ A for \overline{CP}_0 and 160 μ A for \overline{CP}_1 inputs.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT	
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$			
		Min	Max	Min	Max		
f_{MAX}	$\overline{\text{CP}}_0$ input count frequency	Waveform 1	10		32	MHz	
f_{MAX}	$\overline{\text{CP}}_1$ input count frequency	Waveform 1	10		16		
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ input to Q_0 output	Waveform 1			16 18	ns	
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ input to Q_1 output	Waveform 1			16 21	ns	
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ input to Q_2 output	Waveform 1			16 21	ns	
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ input to Q_3 output	Waveform 1			32 35	ns	
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ input to Q_3 output	Waveform 1		100 100		48 50	ns
t_{PHL}	$\overline{\text{MR}}$ input to any output	Waveform 2				40	ns

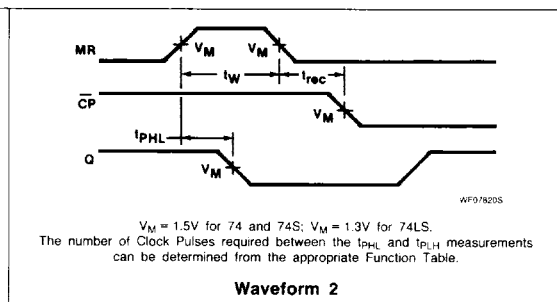
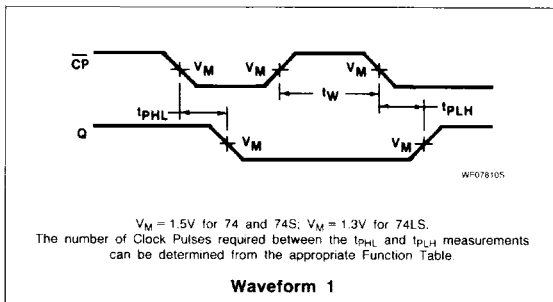
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_w	$\overline{\text{CP}}_0$ pulse width	Waveform 1	50		15	ns
t_w	$\overline{\text{CP}}_1$ pulse width	Waveform 1	50		30	ns
t_w	$\overline{\text{MR}}$ pulse width	Waveform 2	50		15	ns
t_{rec}	Recovery time, $\overline{\text{MR}}$ to $\overline{\text{CP}}$	Waveform 2			25	ns

AC WAVEFORMS

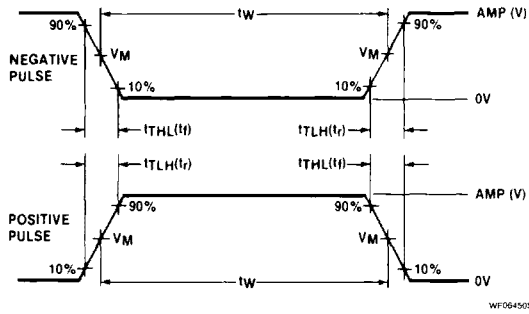
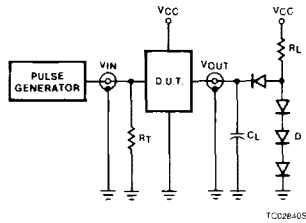


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TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns