

T6K53

Four-Grayscale Dot Matrix Graphic LCD Driver with Built-in RAM

The T6K53 is a single-chip, STN color LCD driver with built-in RAM which can control up to 4096 colors. The T6K53 has 160 output common drivers and 384 output segment drivers. The T6K53 is capable of driving a graphics display with up to 128 RGB colors and up to 160 dots.

The MPU interface allows efficient command setting and high-speed access to the display RAM via a 16-bit parallel interface by means of the High-Speed RAM Write function. The T6K53 has two grayscale modes: Fixed-Palette Mode (with 16 predetermined gray levels) and Selected Palette Mode. In Selected Palette Mode the T6K53 enables high-quality display characteristics by allowing selection of any 16 gray levels from an LCD's 32 available levels.

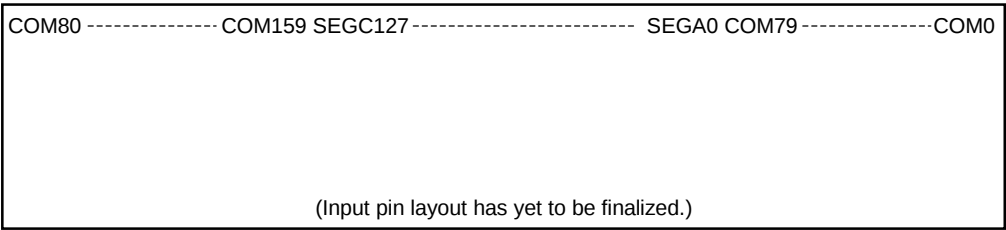
The T6K53 LCD driver can be driven using a single power supply, since it incorporates a voltage regulator, a voltage-dividing resistance, an LCD driver op-amp, a DC-DC converter (with 3 to 8 holds) and a contrast (electronic volume) control circuit. Since the T6K53 supports various display functions (e.g. a partial display function and Area Scroll Mode), it is suitable for applications which require a long battery lifetime, such as Web-capable mobile phones.

Unit: mm		
T6K53	Lead Pitch	
	IN	OUT
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.		
TCP (Tape Carrier Package)		

Features

- Driver output : 128 RGB (384 outputs) × 160 COM
 - Display RAM : 128 × 160 × 12 = 245,760 bits
 - Grayscale function : 4096 colors can be displayed with R = 16 levels, G = 16 levels and B = 16 levels
PWM grayscale system (with 16-level fixed palette)
 - Word length : 8 bits/16 bits
 - Display modes : Normal Display Mode ... Full display
Partial Display Mode ... Partial display
Standby Mode ... Clock stopped
 - MPU interfaces : 8-bit/16-bit switching, 68/80 Series parallel interface and serial interface
 - RAM access cycle : 100 ns or lower
 - Oscillator : Built-in CR oscillator (with built-in oscillation CR). External clock pulses can be input.
 - Operating voltage : $V_{DD} = 1.7 \text{ V to } 3.3 \text{ V}$, $V_{IN} = 2.7 \text{ V to } 3.3 \text{ V}$
 - Display operating voltage : 20.0 V max
 - Built-in display power supply circuits: DC-DC converter ... $V_{IN} \times 8$ (max) booster
OP Amp ... V_{LC1} , V_{LC2} , V_{LC3} and V_{LC4}
Regulator ... $0.0\%/^{\circ}\text{C} \pm 0.02\%$
 - CMOS process : STD $0.35 \mu\text{m} + 22 \text{ V}$
 - Package : COF
 - Low power consumption : $I_{SS} = 300 \mu\text{A}$ (typ.) ... target value
- Usage conditions
 $V_{DD} = 3.0 \text{ V}$, display voltage = 20.0 V, no LCD load, $T_a = 25^{\circ}\text{C}$,
 $f_{\text{Frame}} = 70 \text{ Hz}$, $f_{\text{osc}} = 168 \text{ kHz}$ (with internal oscillator used), no data access

Pin Assignment

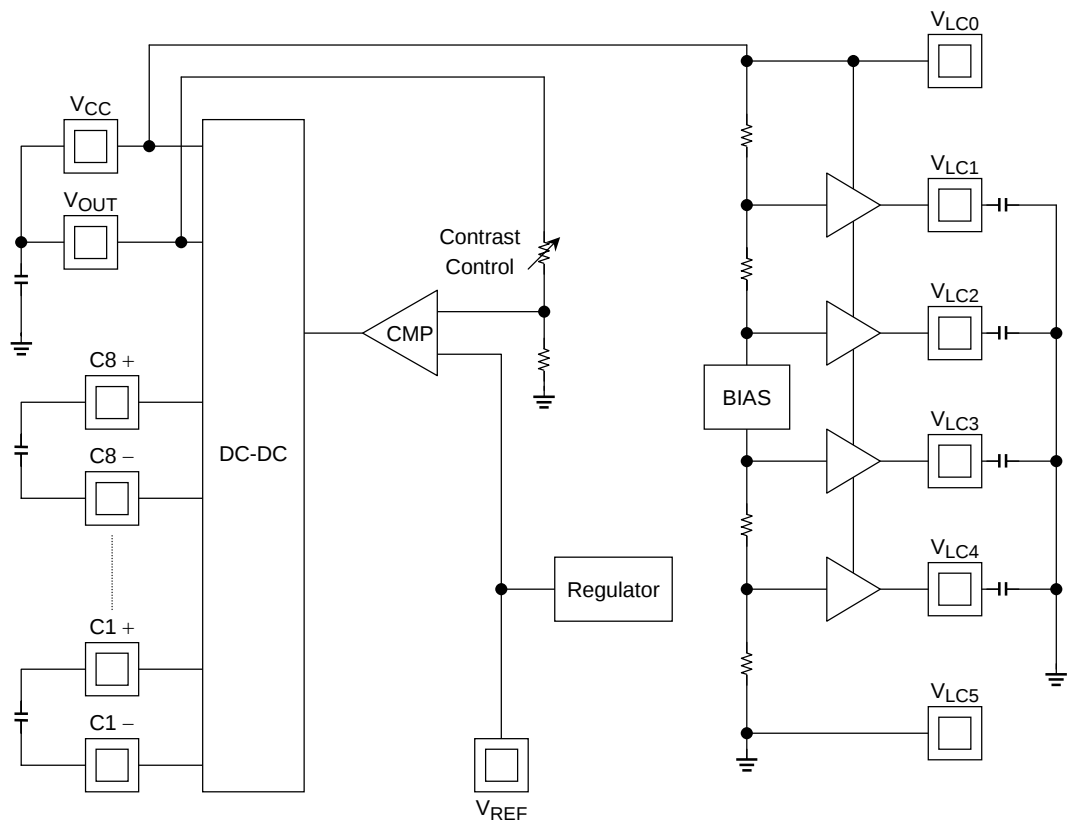


Pin Functions

Pin name	I/O	Functions
SEGA0 to SEGA127	O	LCD drive segment signal output (red or blue): Can be selected using SWP.
SEGB0 to SEGB127	O	LCD drive segment signal output (green)
SEGC0 to SEGC127	O	LCD drive segment signal output (red or blue): Can be selected using SWP.
COM0 to COM159	O	LCD drive common signal output
DB0 to DB15	I/O	Data bus
/CS1	I	Chip Select signal input 1 Data write...Data is written on the rising edge of /CS1 Data read...Data is read while /CS1 is Low.
CS2	I	Chip Select signal input 2 Data write...Data is written on the falling edge of CS2. Data read...Data is read while CS2 is High.
RS	I	Register set / instruction data select signal input • If RS is High, DB0 to DB15 are read as register number. • If RS is Low, DB0 to DB15 are read as instruction data.
/WR (R/W)	I	Write Select signal input (Read/Write select signal input) • If the 80 Series MPU is selected, data is written when /WR is Low. • If the 68 Series MPU is selected, whether Read or Write is in effect is indicated.
/RD (E)	I	Read Select signal input • If the 80 Series MPU is selected, data is output on DB0 to DB7 while /RD is Low. • If the 68 Series MPU is selected, this pin is used as an enable signal input (E).
MPU	I	68/80 Series MPU parallel interface select signal input • If MPU is High, the 68 Series MPU parallel interface is selected. • If MPU is Low, the 80 Series MPU parallel interface is selected.
WLS	I	Data Bus Width Select signal input • 8-Bit Bus Mode if WLS is Low. • 16-Bit Bus Mode if WLS is High.
/RST	I	Reset signal • A reset occurs if /RST is Low.
OSC1	I/O	Built-in oscillation monitoring Internal Oscillation Mode: Output External Oscillation Mode: Input
EXP	I	External Power Supply Mode Internal Power Supply Mode if EXP is Low. External Power Supply Mode if EXP is High. In External Power Supply Mode, DCDC and AMP will remain OFF regardless of command settings.
P/S	I	Input for Parallel/Serial Interface Select signal The serial interface is selected if P/S is Low. The parallel interface is selected if P/S is High.
SCK	I	Serial interface clock input
SI	I	Serial interface data input
SO	O	Serial interface data output
V _{REF}	—	LV regulator output
C11 + to C17 –	—	Booster capacitor connection
V _{OUT}	—	Booster output. Usually connected to V _{CC} .
V _{CC}	—	Power supply for LCD drive voltage generation
V _{LC5} , V _{LC4} , V _{LC3} , V _{LC2} , V _{LC1}	—	LCD drive voltage output
V _{DD} , V _{SS}	—	Supply voltage

LCD Power Supply Configuration

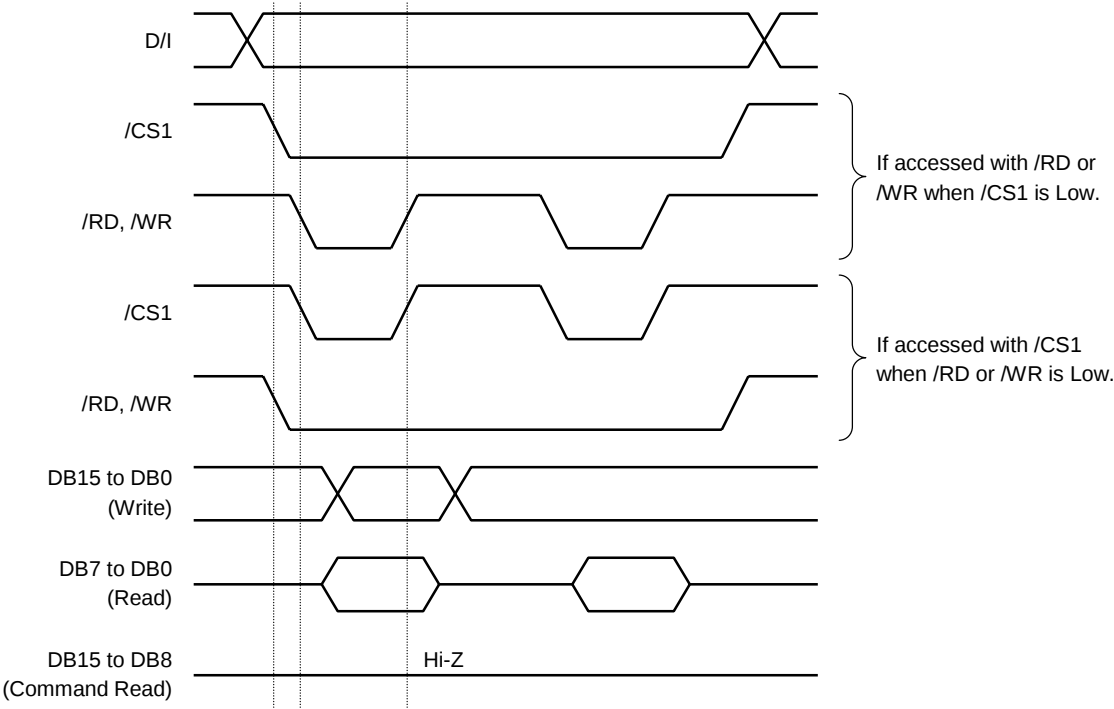
Draft power supply circuit (preliminary)



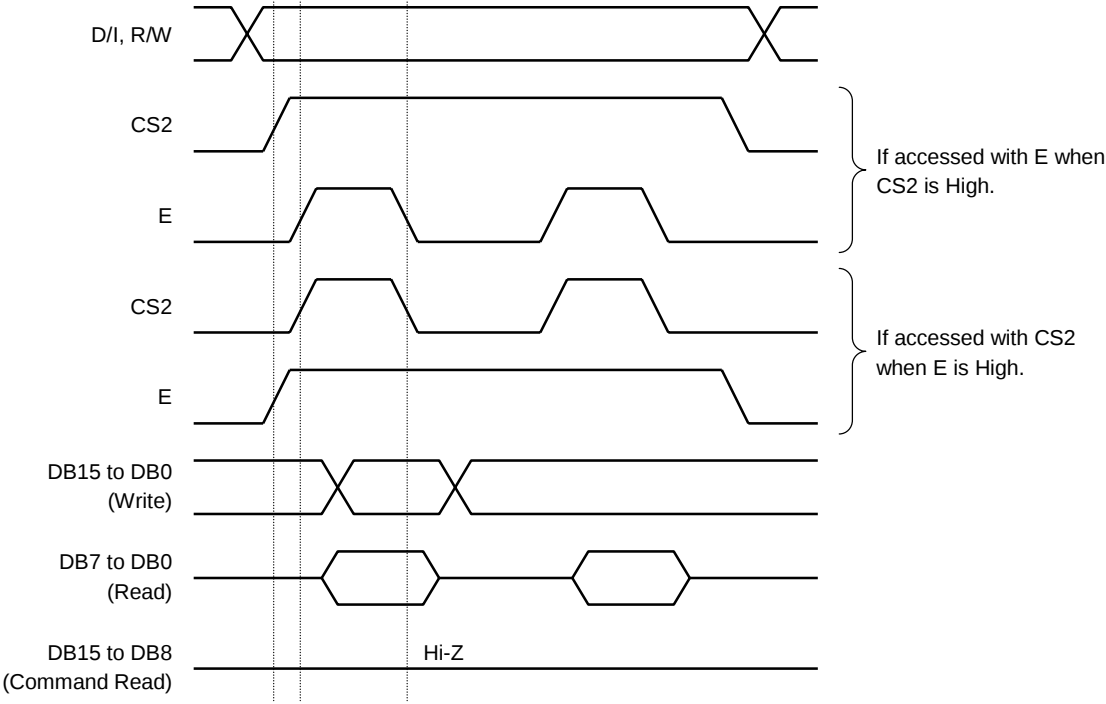
Signal Timing

MPU interface

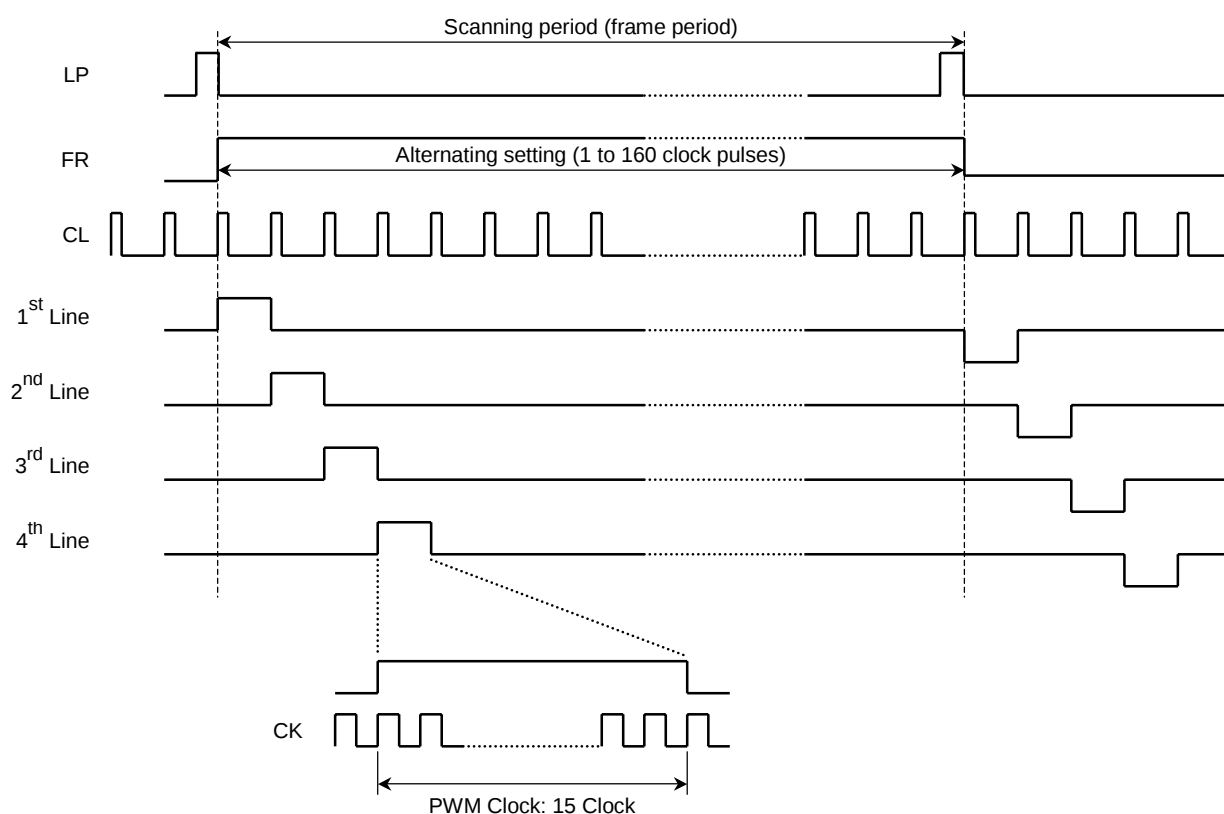
80 Series MPU



68 Series MPU



Display Control Section Signal



LP: Signal for indicating frames

FR: Alternating signal. Display waveforms are made to alternate in sync with this signal.

CL: Shift clock, used to synchronize display data output with row output.

CK: Minimum clock used as a reference for driving the LCD. It is used to control pulse levels.

Functions

MPU interfaces

The MPU interfaces can be connected directly to the data bus of the 8-bit/16-bit MPU for data transfer. The MPU pin can be used to select either the 80 and 68 Series MPU interface for the 8-bit/16-bit MPU.

MPU	MPU type	/CS1	CS2	/RD	/WR	Data bus
H	68 Series MPU	L	CS	E	R/W	DB0 to DB15
L	80 Series MPU	/CS	H	/RD	/WR	DB0 to DB15

Data identification

The contents of the data bus are identified using a combination of the RS, /RD and /WR signals.

RS	68 Series	80 Series		Function
		/RD	/WR	
L	L	H	L	Register No. set
L	H	L	H	Status read
H	H	L	H	Display data read
H	L	H	L	Command and display data write

16-bit access to display RAM

The T6K53 supports 16-bit data access. Data on the 16-bit data bus (DB0 to DB15) can be used to access display RAM.

The WLS bit is used to specify 16-Bit Access Mode as the data bus mode.

WLS	Data bus width	DB0 to DB7	DB8 to DB15
1	16-Bit Access Mode	DB0 to DB7	DB8 to DB15
0	8-Bit Access Mode	DB0 to DB7	High or Low input

Note that even in 16-Bit Access Mode, the internal registers are accessed in 8-Bit Mode (DB0 to DB7). Therefore, 16-Bit Access Mode is only valid for display RAM access.

Data bus mode and display RAM address

The MPU sets up display RAM addresses using X- and Y-addresses which are in pixel units. When the data bus mode is switched, address conversion is handled automatically.

The following paragraphs describe display RAM addresses for each data bus mode.

(1) 8-Bit Mode

In this mode, a single pixel's data is transferred using two 8-bit data accesses. Hence, 8-bit MPU data accesses are used.

The transfer format is as follows: the first access sets the 8 low-order bus bits to the value of the 8 low-order DD bits, and the second access sets the 4 high-order bus bits to the value of the 4 high-order DD bits.

For example, if a data transfer is interrupted after the fifth access (by an access to another command register), the access will be resumed using the 4 high-order bits of 002H (unless the Y-Adr has been reset). To restart data access from the point at which it was interrupted, set the Y-Adr to 002H.

Pixel	First pixel												Second pixel											
Y-Adr	000H												001H											
DD bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bus bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Data Access	Second				First								Fourth				Third							

- Start Y-Adr: When 000H

Pixel	First pixel		Second pixel		Third pixel		Fourth pixel		Fifth pixel	
Y-Adr	000H		001H		002H		003H		004H	
Data Access	Second	First	Fourth	Third	Sixth	Fifth	Eighth	Seventh	Tenth	Ninth

- Start Y-Adr: When 002H

Pixel	Third pixel		Fourth pixel		Fifth pixel		Sixth pixel		Seventh pixel	
Y-Adr	002H		003H		004H		005H		006H	
Data Access	Second	First	Fourth	Third	Sixth	Fifth	Eighth	Seventh	Tenth	Ninth

Pixel : Display pixel
 Y-Adr : Y-Address
 DD bit : Display data bit
 Bus bit : Data bus bit
 Data Access: Number of accesses

(2) 16-Bit Mode

This mode transfers one-pixel data with one 16-bit data access. So the data access of the 16-bit MPU is used.

The 12 low-order bus bits (D11 to D0) correspond to the DD bits.

Pixel	First pixel												Second pixel											
Y-Adr	000H												001H											
DD bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bus bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Access	First												Second											

- Start Y-Adr: When 000H

Pixel	First pixel	Second pixel	Third pixel	Fourth pixel	Fifth pixel
Y-Adr	000H	001H	002H	003H	004H
Data Access	First	Second	Third	Fourth	Fifth

- Start Y-Adr: When 002H

Pixel	Third pixel	Fourth pixel	Fifth pixel	Sixth pixel	Seventh pixel
Y-Adr	002H	003H	004H	005H	006H
Data Access	First	Second	Third	Fourth	Fifth

Pixel : Display pixel

Y-Adr : Y-address

DD bit : Display data bit

Bus bit : Data bus bit

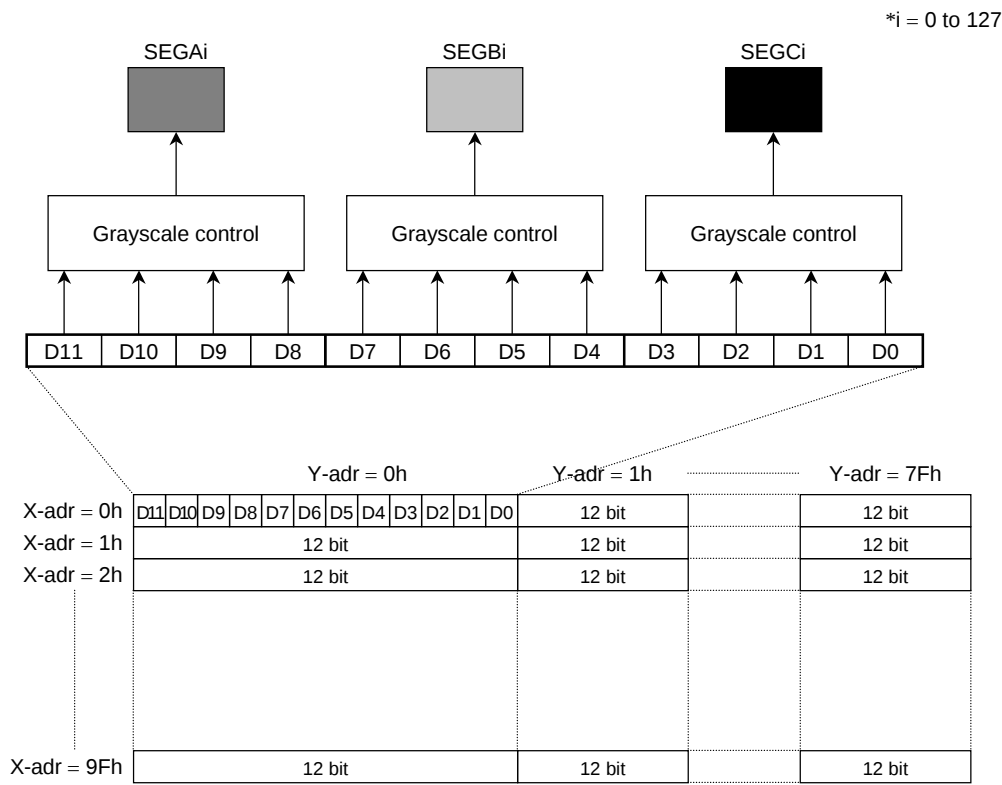
Data Access: Number of accesses

Display RAM

The T6K53 incorporates a bitmap display RAM consisting of 160 pixels × 128 RGB levels. The display RAM section consists of 12 bits × 128 (= 1536 bits) in the Y-address direction and 160 bits in the X-address direction.

The grayscale is controlled via 4-bit segment by driver outputs which correspond to the 16 grayscale levels. Hence, three RGB segment driver outputs service one pixel, using four bits each for the R, G and B levels for a total of 12 bits supporting 4096 display colors (16 levels × 16 levels × 16 levels).

The MCU sets up each RAM address in pixel units by Y-address/X-address pairing, as shown below:



Display RAM Addresses

Data in the RAM area can be accessed continuously.

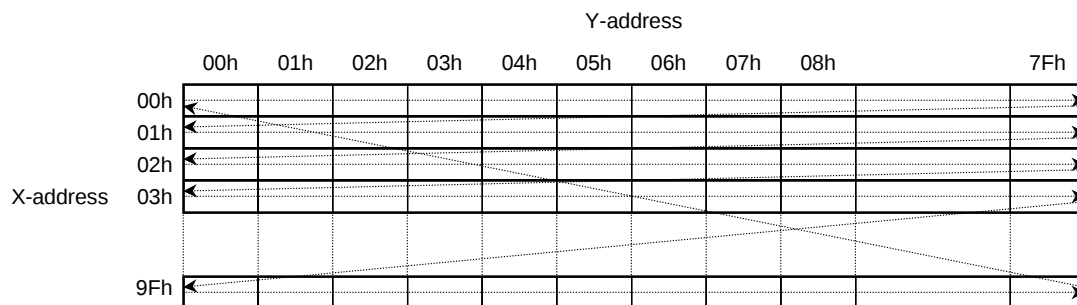
If data access is performed in the address area (X-address = 00H to 9FH and Y-address = 00H to 7FH) in Y-Address Count Mode, the Y-address changes from 00H to 01H. If data access is performed while the Y-address = 7FH, the Y-address will become 00H and the X-address will be incremented to 01H.

If a data access is performed when the Y-address = 7FH and the X-address = 9FH, the Y-address and the X-address will both be set to 00H.

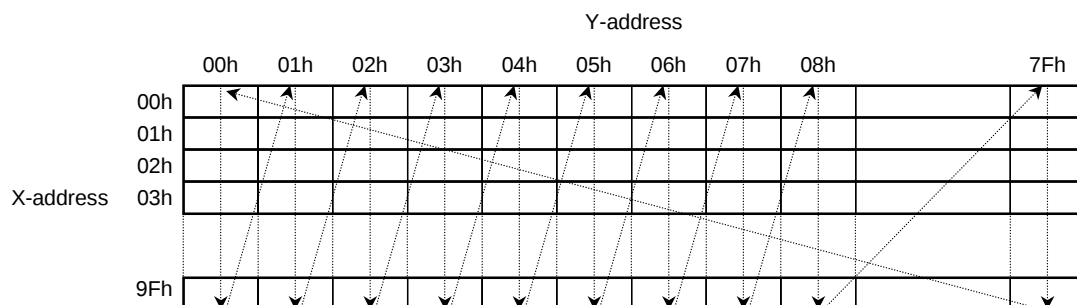
If a data access is performed in X-Address Count Mode, the X-address will be incremented from 00H to 01H.

Every time a data access is performed when the X-address = 9FH, the X-address will wrap around to 00H and the Y-address will be set to 01H. If a data access is performed when the Y-address = 7FH and the X-address = 9FH, the Y-address and the X-address will both be set to 00H.

Y-Address Count Mode (Y-adr area = 00H to 7FH and X-adr area = 00H to 9FH)

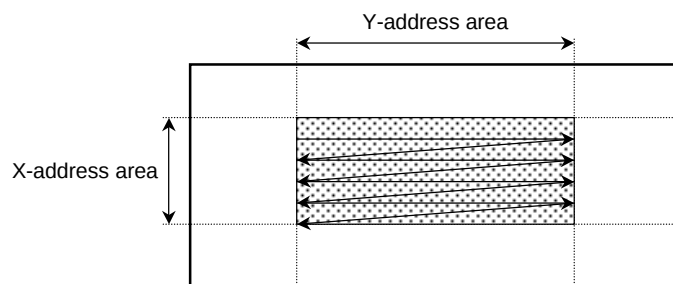


X-Address Count Mode (Y-adr area = 00H to 7FH and X-adr area = 00H to 9FH)



Setting Up the Display Ram Access Area

Setting up the RAM access area using the Y-address control circuit and the X-address control circuit allows only part of the RAM address area to be accessed.



Y-address control circuit

In Y-Address Count Mode, setting up the addresses for the Y-address area (Y-start and Y-end) causes the Y-address to be incremented from the Y-start address to the Y-end address and then to wrap around back to the Y-start address. When the Y-address wraps around, the X-address is also incremented by one.

X-address control circuit

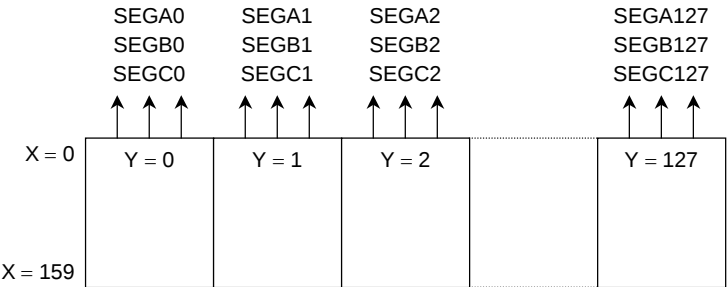
In X-Address Count Mode, setting up the addresses for the X-address area (X-start and X-end) causes the X-address to be incremented from the X-start address to the X-end address and then to wrap around back to the X-start address. When the X-address wraps around, the Y-address is also incremented by one.

Display Direction

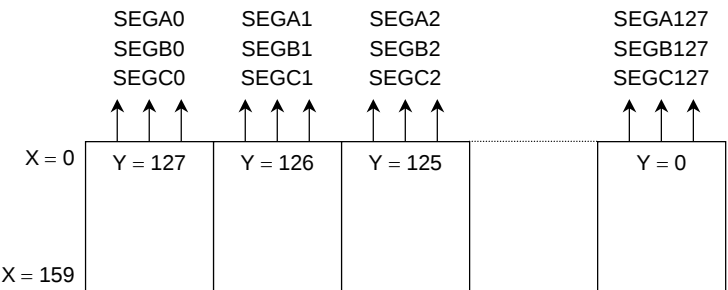
SDR

The S DR pin is used to set up the direction of segment display.
This is implemented by inverting the Y-address when the display data is written.

If SDR is Low



If SDR is High



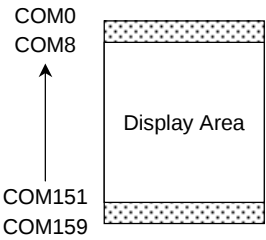
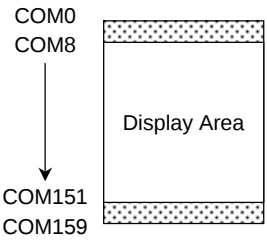
CDR

The CDR pin is used to change the direction of COM scanning.
The two COM scanning directions (↓↑) are shown below.

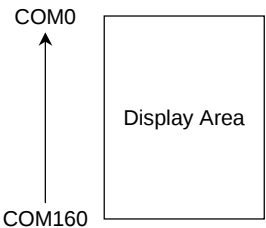
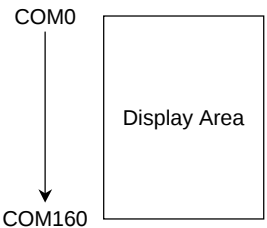
CDR = L

CDR = H

For 1/144 duty



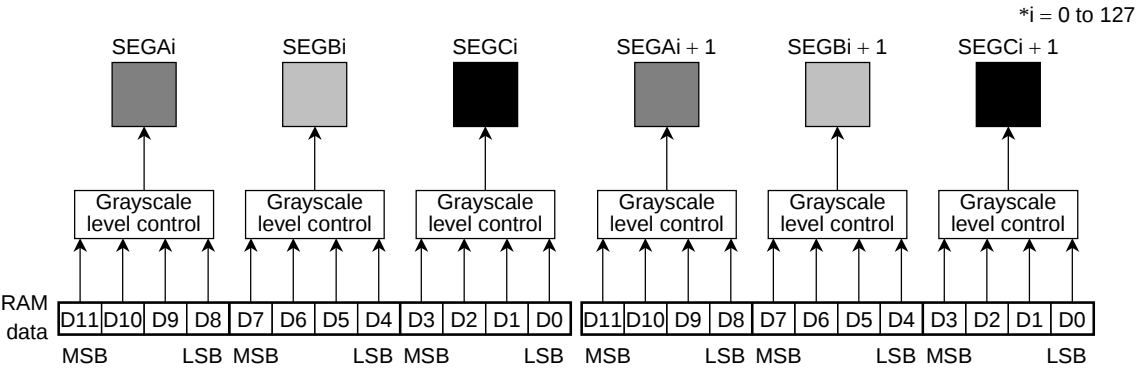
For 1/160 duty



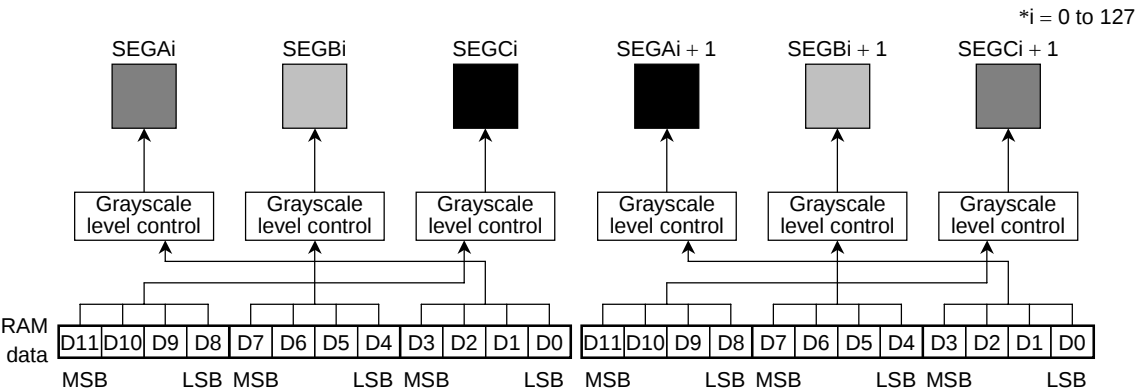
SWP

The SWP pin is used to change the RGB assignments for the SEG outputs (Ai, Bi and Ci). This function implements R-B swapping in the grayscale control circuits.

SWP = 0



SWP = 1



	SEGAi	SEGBi	SEGCi	
SWAP = 0	Red	Green	Blue	Color
	D11 to D8	D7 to D4	D3 to D0	Corresponding bits
SWAP = 1	Blue	Green	Red	Color
	D3 to D0	D7 to D4	D11 to D8	Corresponding bits

Relationship between SDR-/SWP-based display RAM and output

SDR	SWP													
0	0													
		SEG No.			SEG0			SEG1				SEG127		
		Output			A	B	C	A	B	C		A	B	C
		Color			Red	Green	Blue	Red	Green	Blue		Red	Green	Blue
		Data bit			D11 to D8	D7 to D4	D3 to D0	D11 to D8	D7 to D4	D3 to D0		D11 to D8	D7 to D4	D3 to D0
Y-address			00h			01h			7Fh					
0	1													
		SEG No.			SEG0			SEG1				SEG127		
		Output			A	B	C	A	B	C		A	B	C
		Color			Blue	Green	Red	Blue	Green	Red		Blue	Green	Red
		Data bit			D3 to D0	D7 to D4	D11 to D8	D3 to D0	D7 to D4	D11 to D8		D3 to D0	D7 to D4	D11 to D8
Y-address			00h			01h			7Fh					
1	0													
		SEG No.			SEG0			SEG1				SEG127		
		Output			A	B	C	A	B	C		A	B	C
		Color			Blue	Green	Red	Blue	Green	Red		Blue	Green	Red
		Data bit			D3 to D0	D7 to D4	D11 to D8	D3 to D0	D7 to D4	D11 to D8		D3 to D0	D7 to D4	D11 to D8
Y-address			7Fh			7Eh			00h					
1	1													
		SEG No.			SEG0			SEG1				SEG127		
		Output			A	B	C	A	B	C		A	B	C
		Color			Red	Green	Blue	Red	Green	Blue		Red	Green	Blue
		Data bit			D11 to D8	D7 to D4	D3 to D0	D11 to D8	D7 to D4	D3 to D0		D11 to D8	D7 to D4	D3 to D0
Y-address			7Fh			7Eh			00h					

Display Modes

The following display modes are supported.

- Normal Mode
- Partial Display Mode
- Standby Mode

Each mode is described below.

Normal Mode

This is the mode which is used normally. It is selected when a reset occurs. To start up a display in practice, however, requires the execution of the Display ON command.

Normal Mode uses the following settings:

- Display size : Duty cycle setting
- Display bias : Bias (1)
- Contrast setting: Contrast (1)

Display ON/OFF

Display ON

Once a reset function is executed, the following settings must be made before Display ON is executed:

- Stand-By Mode OFF
- Oscillator ON
- OP Amp ON

Executing Display ON sets /DOFF High and takes the circuit out of the Display OFF state, thus enabling display.

Display OFF

Executing the Display OFF command causes the following:

- All SEG outputs : VLC2 or VLC3 (inverted by FR)
- All COM outputs : VLC1 or VLC4 (inverted by FR)

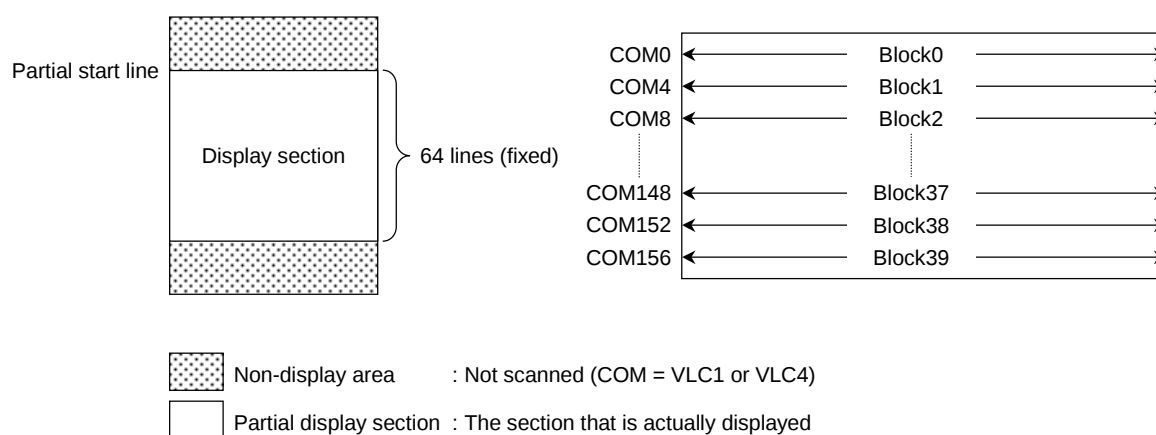
Partial Display Mode

In this mode it is possible to specify a partial screen area for display (64 lines or 32 lines plus start block). This mode consumes little power compared with Full-Screen Display Mode and is thus suitable for use for standby modes on a mobile phone.

This mode is valid when the display is ON.

To set up the partial display area, specify the partial area start block (scanning start position) with a block number for every four lines as shown below.

The partial area size can be selected as either 64 lines and 32 lines.



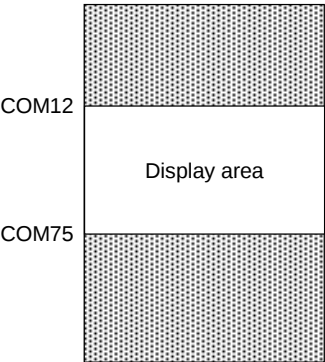
Switching from Normal Mode to the Partial Display Mode will occur at the start of the first frame after the setting has been completed.

Operation in Partial Display Mode

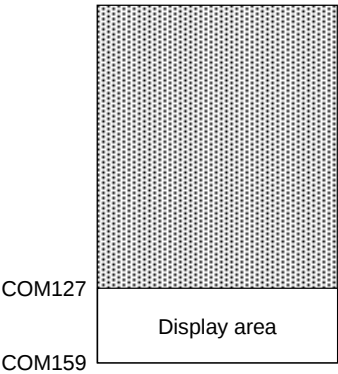
Display duty cycle	1/64 duty or 1/32 duty
Display bias	Bias (2)
Contrast value	Contrast (2)
Oscillation circuit	Automatic frequency switching
SEG output level	Display data (V _{LC0} , V _{LC2} , V _{LC3} , V _{LC5})
COM output (partial display section)	Scanning (V _{LC0} , V _{LC1} , V _{LC4} , V _{LC5})
Common output (non-display area)	V _{LC1} or V _{LC4} (inverted by FR)

Example of Use

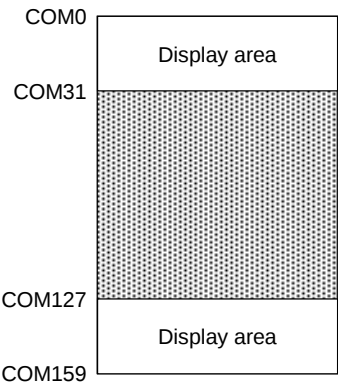
- (1) 1/160 Duty、CDR = 0、Mode = 1 (64 Line)、PDS = 0Ch



- (2) 1/160 Duty、CDR = 0、Mode = 0 (32 lines)、PDS = 1Fh



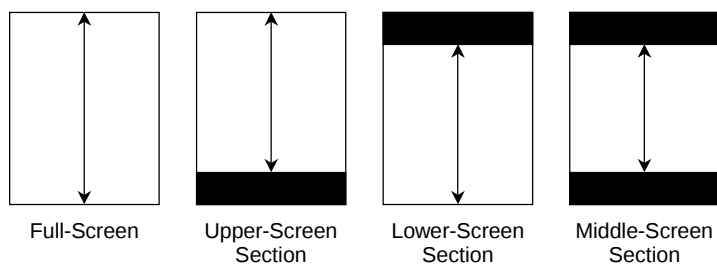
- (3) 1/160 Duty、CDR = 0、Mode = 1 (64 lines)、PDS = 1Fh



Area Scroll Function

It is possible to scroll the screen display partially by specifying the scroll area (start block, end block and the number of specific blocks). 1 block consists of 4 lines. This mode is valid after Display ON is executed.

Area scrolling supports four area modes.



It is possible to scroll the screen display partially by specifying the scroll area (start block, end block and the number of specific blocks). The size of a RAM block must be specified in multiples of 4 lines. The size of the display duty cycle block must also be specified in multiples of 4 lines.

Standby Mode

Standby Mode ON/OFF

Standby Mode

The Standby command causes the device to enter Standby Mode.

In Standby Mode:

- All SEG outputs : V_{SS}
- OSC : OFF
- Display clock (FR, PM, LP and CL) : Stopped
- Op-amp for display power : OFF (VLC0 to VLC5 = fixed at V_{SS})
- DC-DC conversion operation for display: OFF
- /DOFF : Low output
- /STB : Low output

In Standby Mode, it is possible to access commands and display data.

Exiting Standby Mode

When Standby Mode is exited:

- All SEG outputs : DOFF (VLC2 or VLC3)
- All COM outputs: DOFF (VLC1 or VLC4)
- OSC : ON (state before Standby Mode was entered)
- Booster : ON (state before Standby Mode was entered)
- Op-amp : ON (state before Standby Mode was entered)

The states other than Display OFF are the same as before the device entered Standby Mode. Therefore, after the device has exited Standby Mode, the Display ON command must be executed before data can be displayed on-screen.

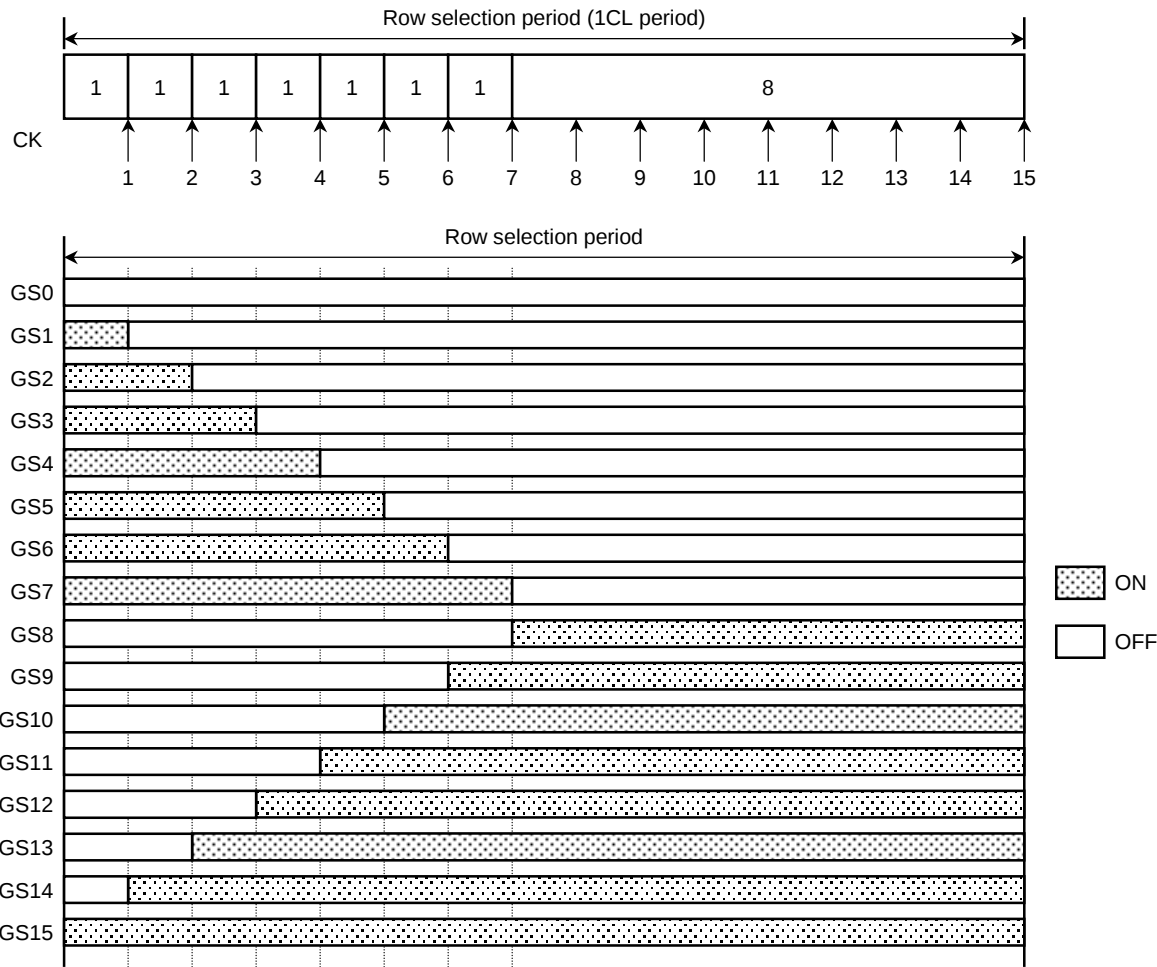
Grayscale Control Circuit

PWM grayscale

Two grayscale modes are available for selection on the T6K53.
GS = 0: Fixed-Palette Mode (16 predetermined grayscale levels)
GS = 1: Palette Selection Mode (any 16 grayscale levels selected from 32 available levels.)

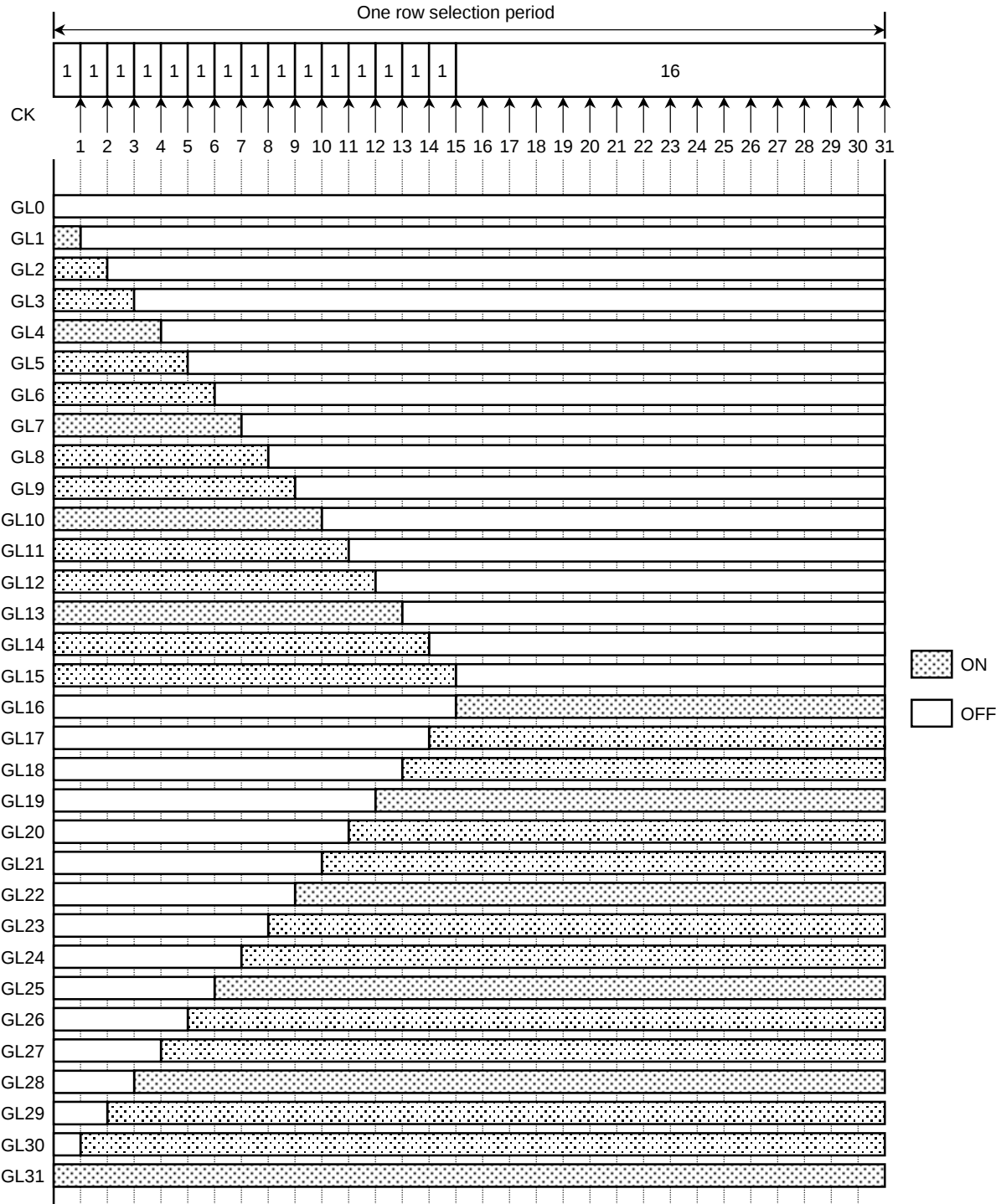
Fixed-Palette Mode

If GS = 0, Fixed-Palette Mode is selected. In this mode, grayscale level output is performed using a predetermined 16-grayscale palette.



Palette Selection Mode

If GS = 1, Palette Selection Mode is selected. In this mode, one row selection period is divided into 31 parts so as to enable selection of 16 grayscale levels from 32 available levels (GL0 to GL31) for display grayscale output.



Individual palettes can be selected for R, G and B separately. Three separate sets of 16 grayscale levels can be selected from the 32 grayscale levels shown above (for R, G and B) (GL0 to GL31) and set up in GS0 to GS15.

Gray Scale Level	DB4/12	DB3/11	DB2/10	DB1/9	DB0/8
GL0	0	0	0	0	0
GL1	0	0	0	0	1
GL2	0	0	0	1	0
...	...	...	...	...	...
GL30	1	1	1	1	0
GL31	1	1	1	1	1

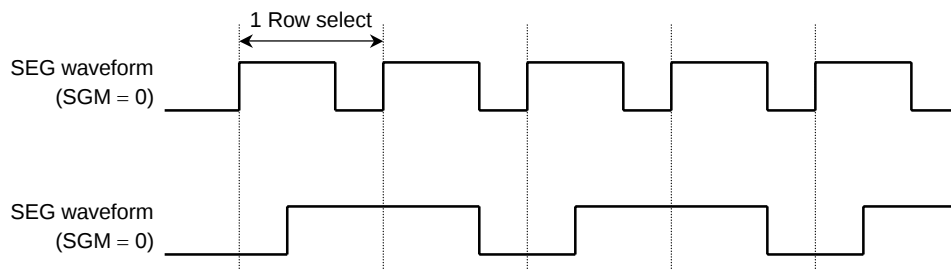
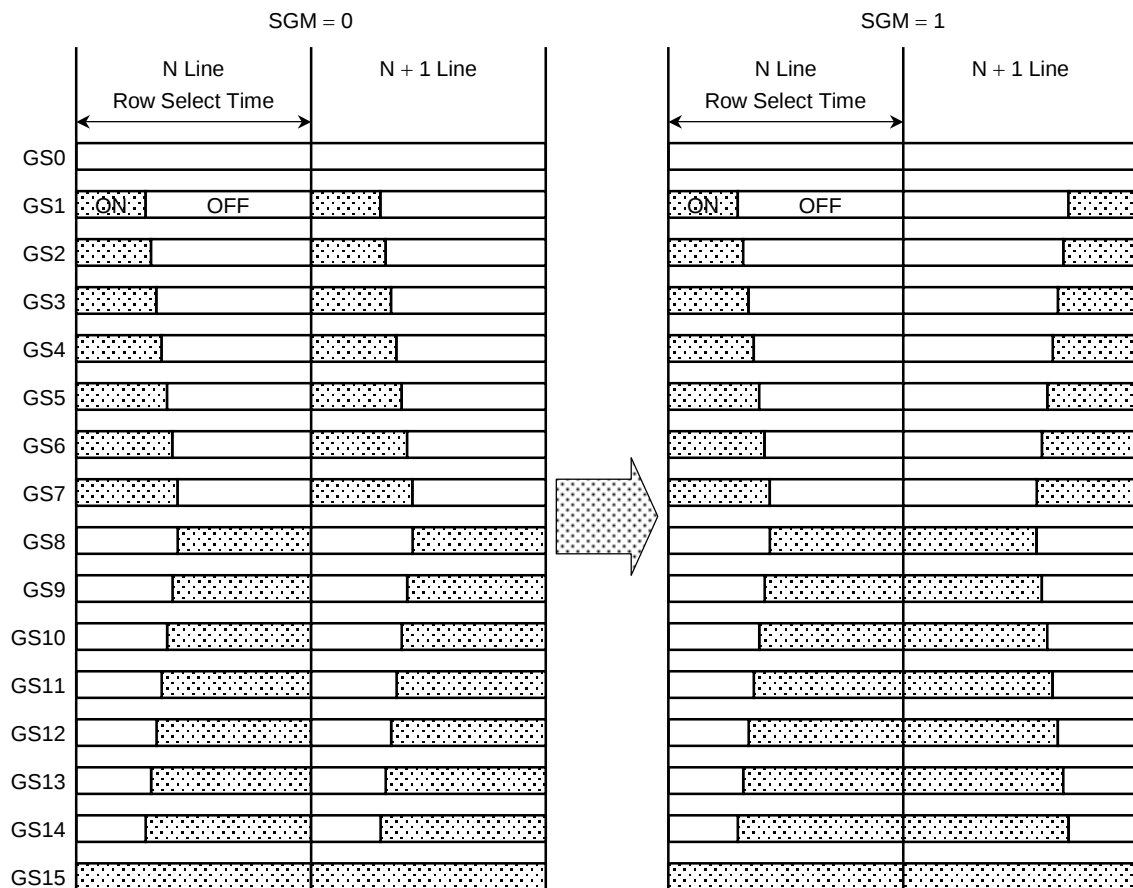
Normal/reverse display

In this mode data output for display on the LCD is reversed without alteration to the display image data.

REV = 0: Turned ON for data values of 1, i.e. VLC0 or VLC5 is selected as SEG output when data value = 1.

REV = 1: Turned ON for data values of 0, i.e. VLC0 or VLC5 is selected as SEG output when data value = 0.

Switching of the PWM waveform output timing



Oscillation Circuit

The oscillation circuit incorporates both a capacitor and a resistor. When the built-in oscillator is used (EXT = 0), the oscillation resistor incorporated in the oscillation circuit is switched automatically as the device is switched between Normal/Partial Display Mode (1) and Duty Cycle Setting Mode.

Oscillation frequencies when the built-in oscillation circuit is used

Display mode	Duty cycle setting	Oscillation frequency (typical)
Normal	1/160 duty	168.0 kHz
	1/144 duty	151.2 kHz
	1/128 duty	134.4 kHz
Partial	1/64 duty	67.2 kHz
	1/32 duty	67.2 kHz (divided by 2 to give internal clock)

- Frame period = 70 Hz (typical)
- Calculation method:

$$F_{osc} = \text{frame period} \times (\text{display line count}) \times \text{clock division number (15)}$$
- For a partial display in 1/32 Duty Mode, the internal clock pulses are generated at a frequency obtained by dividing the frequency for a partial display in 1/64 Duty Mode by 2.

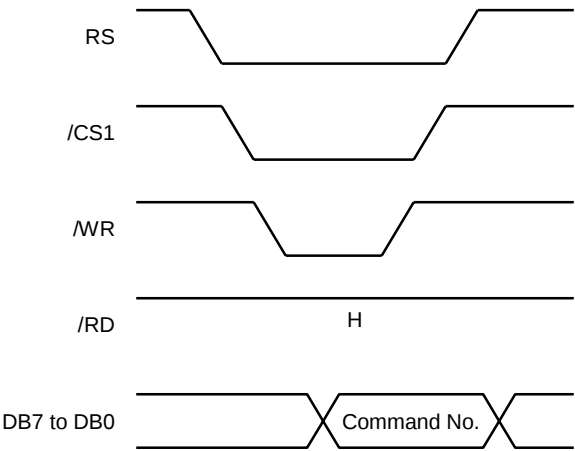
If EXT = 1, External Clock Mode is selected and an external clock signal can be input on the OSC pin.

In External Clock Mode, switching between the Normal and Partial Display Modes requires that the clock frequency be changed according to the display mode which is to be selected.

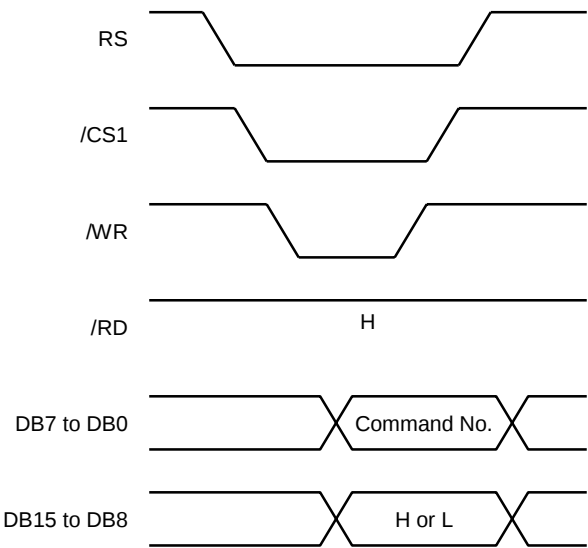
Data Bus Behavior When Data is Accessed (example: MPU = L, i.e. device is in 80 Mode)

Register set

8-Bit Mode

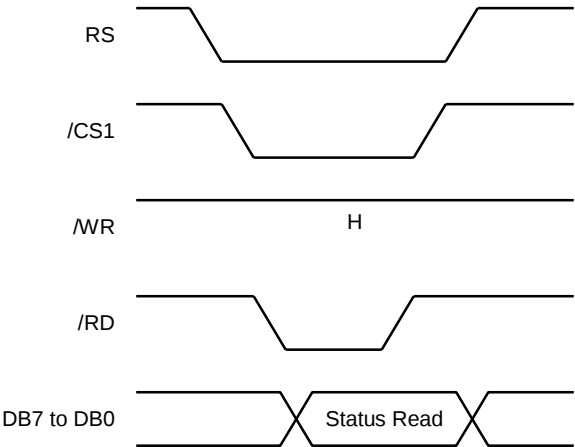


16-Bit Mode

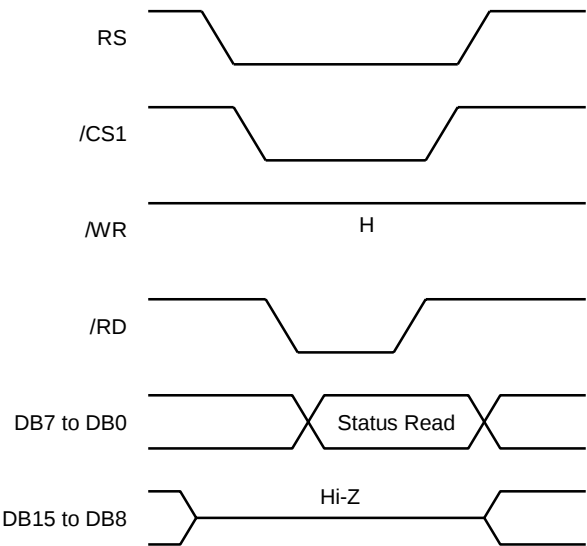


Command read (Status Read)

8-Bit Mode

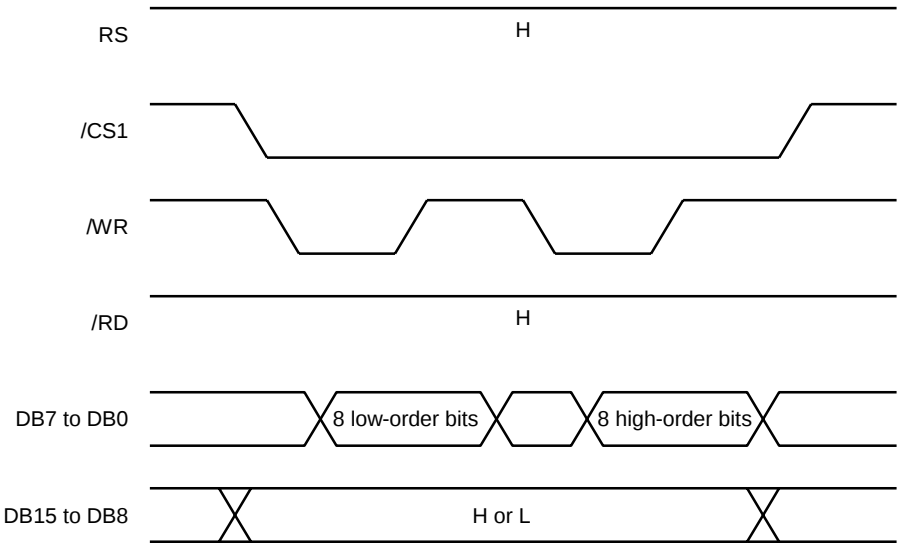


16-Bit Mode

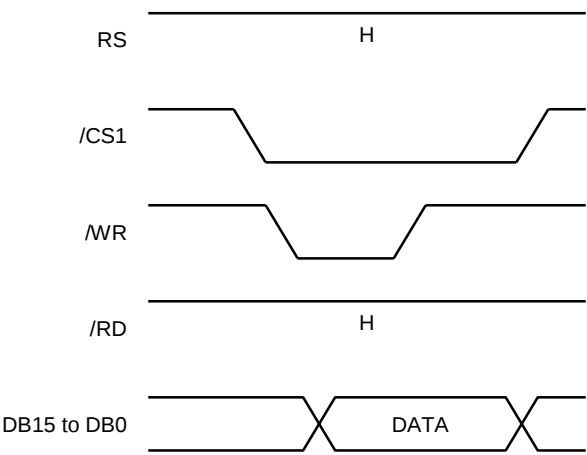


Command Data Write

8-Bit Mode

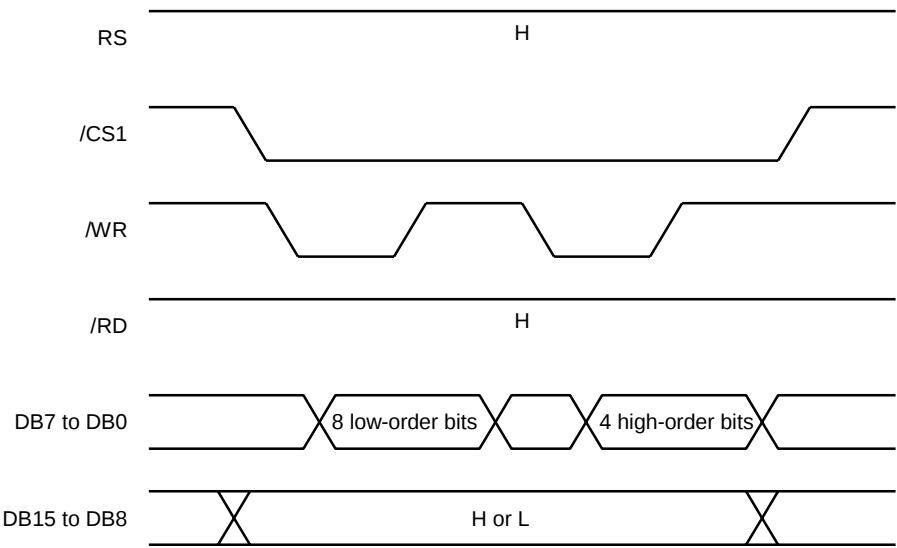


16-Bit Mode

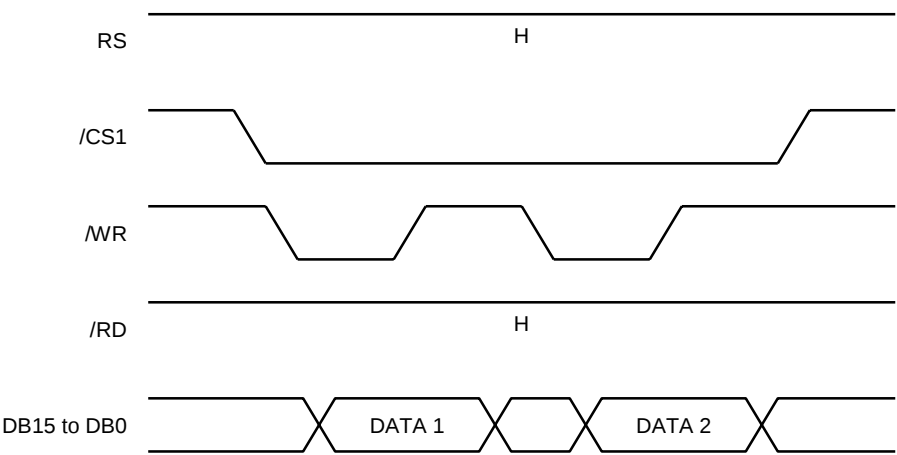


Display Data Write

8-Bit Mode

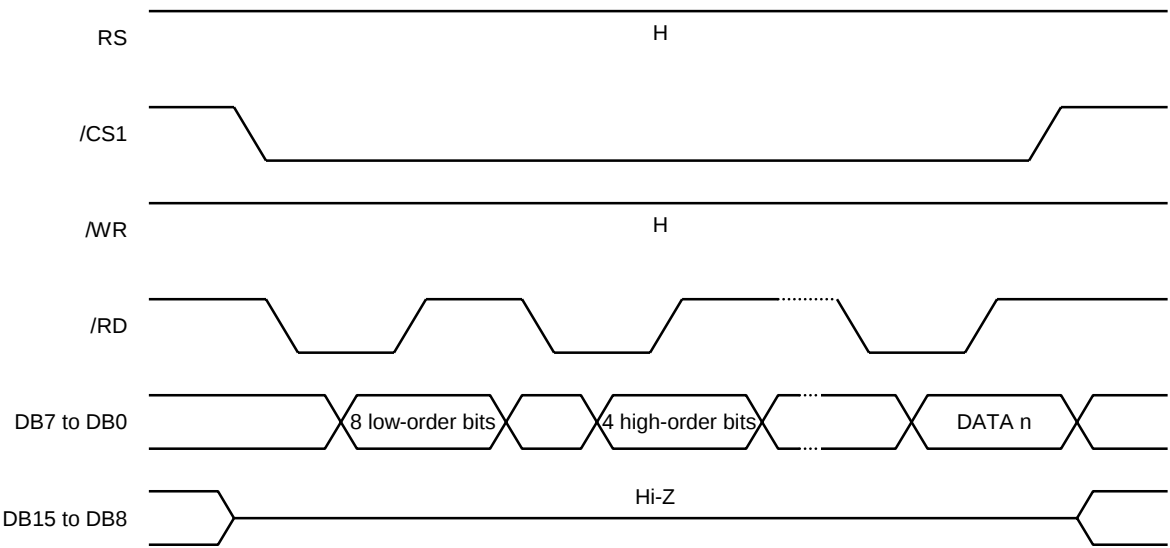


16-Bit Mode

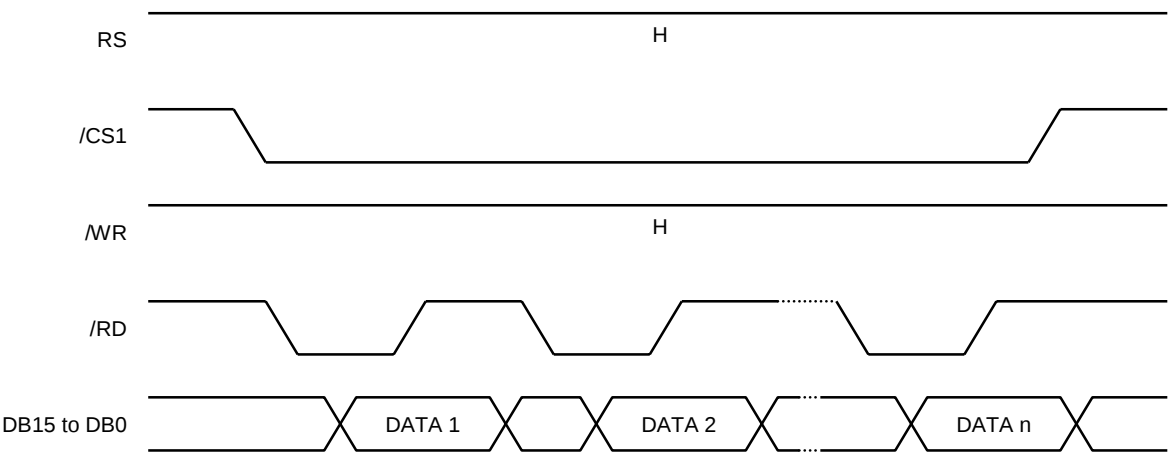


Display Data Read

8-Bit Mode



16-Bit Mode



Clock-Synchronous Serial Interface

Setting the P/S pin to the VSS level enables data to be transferred via a clock-synchronous serial interface. When data is transferred in this way, a synchronous clock input is received on the SCK pin, and transfer data is input on the SI pin and output on the SO pin. Just as with the parallel interface, the /CS1 and CS2 pins can be used for a chip select signal. If the /CS1 pin is used, for example, data transfer begins when /CS1 changes from High to Low and ends when it changes from Low to High. The CS2 pin is fixed at the VDD level.

The basic transfer data format uses 24 bits in total. The first eight bits are a start byte and the other 16 bits are the parameter data.

The start byte consists of six start bits (000110) followed by RS and R/W bits.

RS	R/W	Function
0	0	Register No. Set
0	1	Status Read
1	0	Command and Display Data Write
1	1	Display Data Read

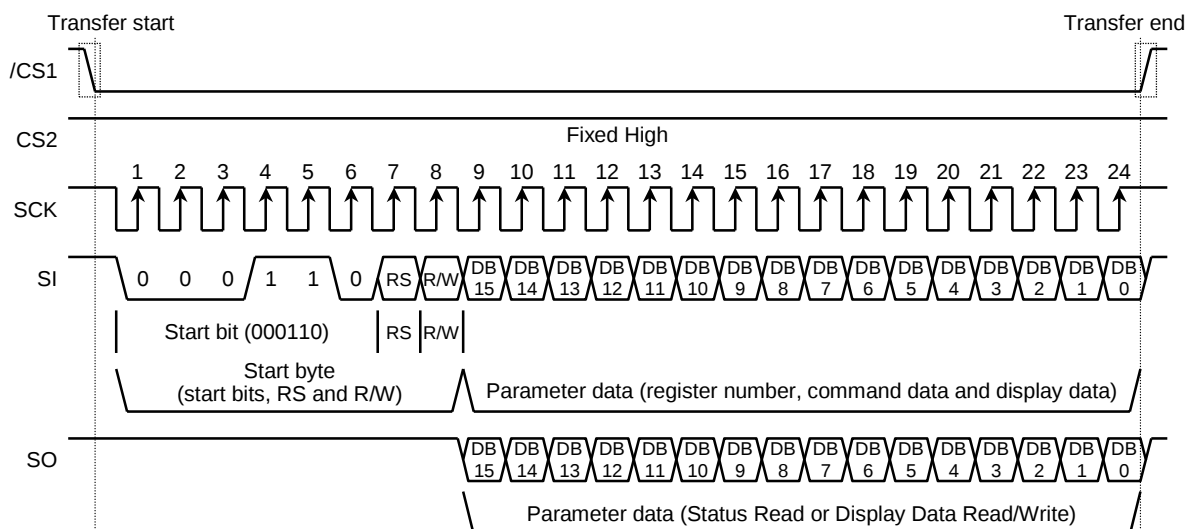
The 16-bit parameter data consists of DB15 to DB0. The bit configuration is the same as for the 16-bit parallel bus. During display data transfer, therefore, the 4 high-order bits (DB15 to DB12) are not valid data. With Register Set and Status Read, the 8 high-order bits are not valid data.

This serial interface supports continuous transfer of parallel data when display data is read or written. The data format used for continuous transfers is made up of an 8-bit start byte, the first 16-bit parameter data item and the second 16-bit parameter data item, which are transferred in order. Within the IC, parameter data is handled in units of 16 bits. The number of consecutive parameter data items is not specified. A data transfer ends when /CS1 goes High.

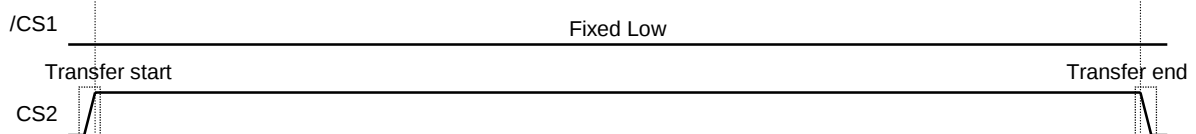
The first parameter data item (16 bits) received during a data read (Status Read or Display Data Read) is assumed to be dummy data. Normal data output begins with the second parameter data item.

If a transfer is terminated in the middle of the start byte or in the middle of one of the 16-bit parameter data items, the previously transferred data is nullified. In this case, the transfer should be restarted.

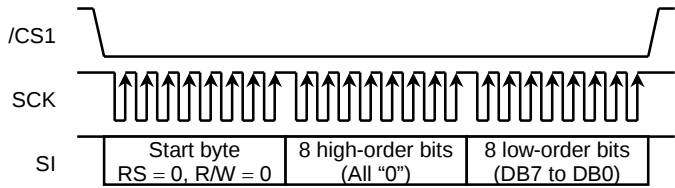
When /CS1 is the Chip Select signal:



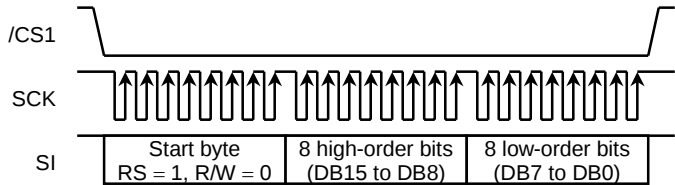
When CS2 is the Chip Select



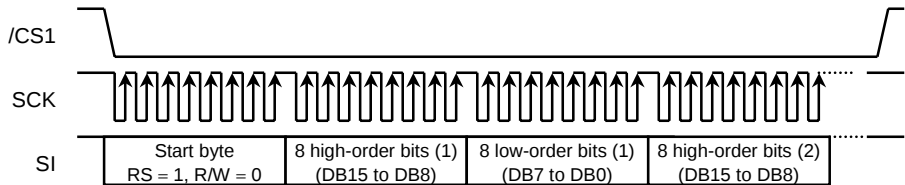
Register Set



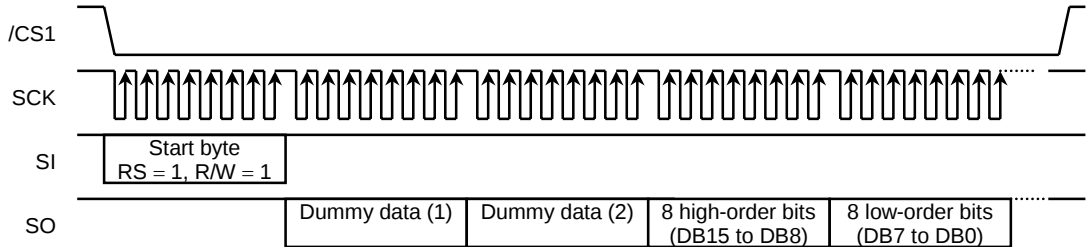
Command Setting



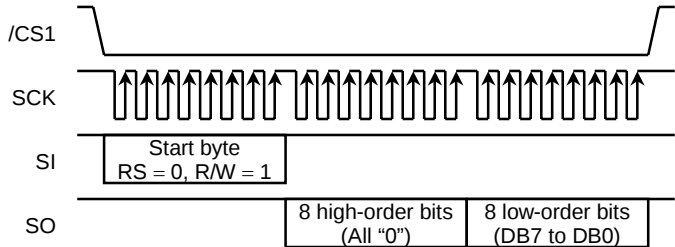
Display Data Write



Display Data Read

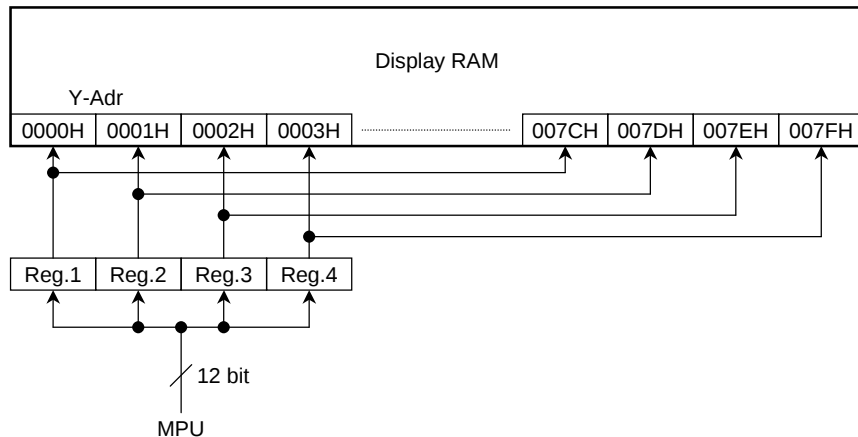


Status Read



High-Speed RAM Write function

The T6K53 incorporates a High-Speed RAM Write function. This function enables the T6K53 to support applications, such as animation software, which require high-speed rewriting of display data.

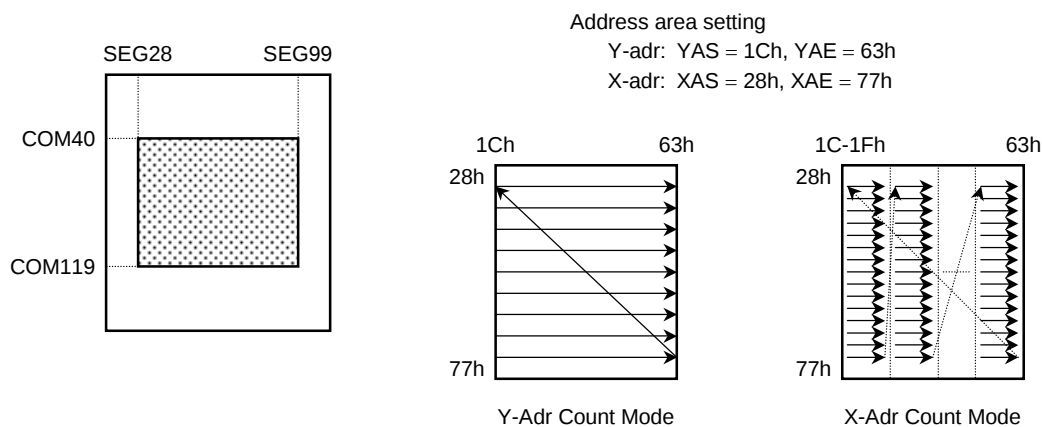


If High-Speed RAM Write is selected for writing display data (i.e. if HRW is set to 1), data received from the MPU is stored in Registers 1 to 4 (each of which consists of one word or 12 bits) and then transferred to the display RAM in 4-word units.

Thus, in High-Speed RAM Write Mode data access must be performed in 4-word units.

The Y-address area must be set up to be 000H to 0003H, 0004H to 0007H, 0008H to 000BH... or 007CH to 007FH. The Y-address area cannot be set up as individual 4-address units (e.g. YAS = 003H and YAE = 00FD). High-Speed RAM Write Mode does not support any read functions.

Example: Selecting a rectangular display area SEG28 to SEG99 and COM40 to COM119



When using High-Speed RAM Write Mode, observe the following precautions:

Precautions:

- Conduct the access count in 4-word units. Otherwise, no data transfer to RAM can occur, resulting in invalid data.
- Set the Y-address area in multiples of 4 address locations.
- In X-Address Count Mode, the count is incremented by one every four accesses.
- After this mode has been turned ON or OFF, be sure to execute a Y-Adr Area Set (31H) before beginning to access display data.
- In High-Speed RAM Write Mode, Display Data Read cannot be performed. To perform a read, first execute the High-Speed RAM Write Mode OFF command (HRW = 0), then start the access.

Command Setting

On the T6K53 both Register Set and Status Read are one-byte commands, while all other instructions consist of two bytes. In 16-Bit Mode both one-byte and two-byte commands are completed with a single access.

In 8-Bit Mode, Register Set and Status Read are completed with a single access. Other instructions are set up with two accesses – first the 8 low-order bits are accessed, then the 8 high-order bits.

In 8-Bit Mode, if a Register Set or Status Read is performed after the first-byte access, the access count will be cleared so that the next access starts with the first byte. Thus, when performing an access in 8-Bit Mode, perform a Status Read at regular intervals so as to avoid crashes due to noise.

Instruction Name	RS	/WR	/RD	Reg. No.	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Register set	L	L	H	—	*	*	*	*	*	*	*	*	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0
Status read	L	H	L	—	*	*	*	*	*	*	*	*	*	*	X/Y	REV	PT	RMW	DP	STB
Standby mode	H	L	H	01h	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	STB
Display ON/OFF	H	L	H	02h	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DP
Function mode (1)	H	L	H	04h	*	*	DC21	DC20	*	*	DC11	DC10	*	*	*	*	AMP	DCDC	EXT	OSC
Function mode (2)	H	L	H	05h	*	*	*	*	*	HRW	RMW	X/Y	*	*	GS	REV	SGM	SWP	CDR	SDR
Contrast control	H	L	H	10h	*	C26	C25	C24	C23	C21	C21	C20	*	C16	C15	C14	C13	C12	C11	C10
Display mode set	H	L	H	11h	*	BS22	BS21	BS20	*	BS12	BS11	BS10	*	*	*	*	*	*	DTY1	DTY0
N-line inversion	H	L	H	12h	*	*	*	*	*	*	*	*	NLI7	NLI6	NLI5	NLI4	NLI3	NLI2	NLI1	NLI0
Color palette (Red)	H	L	H	18h to 1Fh	*	*	*	GS1/GS3/GS5/GS7/GS9/GS11/GS13/GS15					*	*	*	GS0/GS2/GS4/GS6/GS8/GS10/GS12/GS14				
Color palette (Green)	H	L	H	20h to 27h	*	*	*	GS1/GS3/GS5/GS7/GS9/GS11/GS13/GS15					*	*	*	GS0/GS2/GS4/GS6/GS8/GS10/GS12/GS14				
Color palette (Blue)	H	L	H	28h to 2Fh	*	*	*	GS1/GS3/GS5/GS7/GS9/GS11/GS13/GS15					*	*	*	GS0/GS2/GS4/GS6/GS8/GS10/GS12/GS14				
X-adr area set	H	L	H	30h	XAE7	XAE6	XAE5	XAE4	XAE3	XAE2	XAE1	XAE0	XAS7	XAS6	XAS5	XAS4	XAS3	XAS2	XAS1	XAS0
Y-adr area set	H	L	H	31h	*	YAE6	YAE5	YAE4	YAE3	YAE2	YAE1	YAE0	*	YAS6	YAS5	YAS4	YAS3	YAS2	YAS1	YAS0
Partial display mode	H	L	H	40h	*	*	PDS5	PDS4	PDS3	PDS2	PDS1	PDS0	*	*	*	*	*	*	MODE	PT
Scroll mode & area start	H	L	H	50h	*	*	SAS5	SAS4	SAS3	SAS2	SAS1	SAS0	*	*	*	*	*	*	SM1	SM0
Scroll area set.	H	L	H	51h	*	*	SBN5	SBN4	SBN3	SBN2	SBN1	SBN0	*	*	SAE5	SAE4	SAE3	SAE2	SAE1	SAE0
Scroll start block	H	L	H	52h	*	*	*	*	*	*	*	*	*	*	SSB5	SSB4	SSB3	SSB2	SSB1	SSB0
Display data write	H	L	H	70h	*	*	*	*	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Display data read	H	H	L	70h	*	*	*	*	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Toshiba test mode	*	*	*	80h to FFh	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

Command Descriptions

Register set:

This command sets the register address for the command which is to be set up.
80H to FFH are test commands for use by Toshiba. Users should not attempt to access them.

Status read:

This command allows the state of each setting to be checked from the 8 low-order bits.

STB	Function
0	Standby Mode OFF
1	Standby Mode ON

DP	Function
0	Display OFF
1	Display ON

RMW	Function
0	Read-Modify-Write OFF
1	Read-Modify-Write ON

PT	Function
0	Partial OFF (Normal mode)
1	Partial ON (Partial display mode)

X/Y	Function
0	Y-Adr Count Mode
1	X-Adr Count Mode

REV	Function
0	Normal Mode (0: OFF; 1: ON.)
1	Reverse Mode (0: ON; 1: OFF.)

Standby Mode: 01h

This command turns Standby Mode ON/OFF.

STB	Function
0	Standby Mode OFF
1	Standby Mode ON

Display ON/OFF: 02h

This command turns the display ON/OFF.

DP	Function
0	Display OFF
1	Display ON

Function mode (1): 04h

This command sets up the operation of each function.

OSC: Turns the built-in oscillator ON/OFF.

OSC	Function
0	Oscillator OFF
1	Oscillator ON

EXT: Selects either the built-in oscillator or an external oscillator.

EXT	Function
0	Built-in Oscillator Mode
1	External Oscillator Mode

DCDC: Turns the DC-DC conversion circuit ON/OFF.

DCDC	Function
0	DCDC OFF
1	DCDC ON

AMP: Turns the operational amplifier ON/OFF.

AMP	Function
0	AMP OFF
1	AMP ON

DC1x: Specifies the number of DC-DC conversion steps for Normal Mode.

DC11	DC10	Function
0	0	×6 booster
0	1	×7 booster
1	0	×8 booster
1	1	Cannot be set

DC2x: Specifies the number of DC-DC conversion steps for Partial Display Mode.

DC21	DC20	Function
0	0	×3 booster
0	1	×4 booster
1	0	×5 booster
1	1	×6 booster

Function Mode (2): 05h

This command sets up the display operation mode.

SDR: Specifies the direction of segment output.

SDR	Function
0	Y-Adr = 00h → SEG0
1	Y-Adr = 00h → SEG127

CDR: Specifies the direction of COM output.

CDR	Function
0	COM0 → COM159
1	COM159 → COM0

SWP: Changes R, G and B assignments for SEG (A, B and C).

SWP	Function
0	SEG (A, B, C) = R, G, B
1	SEG (A, B, C) = B, G, R

SGM: Specifies the switching of PWM waveform output timing.

SGM	Function
0	OFF
1	ON

REV: Specifies whether the display output data will be reversed.

REV	Function
0	Normal Mode ("0": OFF, "1": ON)
1	Reverse Mode ("0": ON, "1": OFF)

GS: Switches the grayscale palette mode.

GS	Function
0	Fixed-Palette Mode
1	Palette Selection Mode

X/Y: Selects the RAM address count mode.

X/Y	Function
0	Y-Adr Count Mode
1	X-Adr Count Mode

RMW: Read-Modify-Write Mode ON/OFF

RMW	Function
0	Read-Modify-Write OFF
1	Read-Modify-Write ON

Read-Modify-Write Mode function

When a Display Data Read is executed, no address count is executed. The address count is executed only when display data is written. Hence, for example, after the read data has been changed, new data can be written to the previous address without the need to specify the address.

HRW: Turns High-Speed RAM Write Mode ON/OFF.

RMW	Function
0	High-Speed RAM Write Mode OFF
1	High-Speed RAM Write Mode ON

Contrast Control: 10h**Set Normal Mode Contrast**

C16	C15	C14	C13	C12	C11	C10
00h to 3Fh						

VLCD0 voltage (typical) for each Contrast (1) setting

CONT (dec)	CONT (Hex)	V _{LC0} (V)	CONT (dec)	CONT (Hex)	V _{LC0} (V)	CONT (dec)	CONT (Hex)	V _{LC0} (V)	CONT (dec)	CONT (Hex)	V _{LC0} (V)
0	00	10.00	32	20	12.52	64	40	15.04	96	60	17.56
1	01	10.08	33	21	12.60	65	41	15.12	97	61	17.64
2	02	10.16	34	22	12.68	66	42	15.20	98	62	17.72
3	03	10.24	35	23	12.76	67	43	15.28	99	63	17.80
4	04	10.31	36	24	12.83	68	44	15.35	100	64	17.87
5	05	10.39	37	25	12.91	69	45	15.43	101	65	17.95
6	06	10.47	38	26	12.99	70	46	15.51	102	66	18.03
7	07	10.55	39	27	13.07	71	47	15.59	103	67	18.11
8	08	10.63	40	28	13.15	72	48	15.67	104	68	18.19
9	09	10.71	41	29	13.23	73	49	15.75	105	69	18.27
10	0A	10.79	42	2A	13.31	74	4A	15.83	106	6A	18.35
11	0B	10.87	43	2B	13.39	75	4B	15.91	107	6B	18.43
12	0C	10.94	44	2C	13.46	76	4C	15.98	108	6C	18.50
13	0D	11.02	45	2D	13.54	77	4D	16.06	109	6D	18.58
14	0E	11.10	46	2E	13.62	78	4E	16.14	110	6E	18.66
15	0F	11.18	47	2F	13.70	79	4F	16.22	111	6F	18.74
16	10	11.26	48	30	13.78	80	50	16.30	112	70	18.82
17	11	11.34	49	31	13.86	81	51	16.38	113	71	18.90
18	12	11.42	50	32	13.94	82	52	16.46	114	72	18.98
19	13	11.50	51	33	14.02	83	53	16.54	115	73	19.06
20	14	11.57	52	34	14.09	84	54	16.61	116	74	19.13
21	15	11.65	53	35	14.17	85	55	16.69	117	75	19.21
22	16	11.73	54	36	14.25	86	56	16.77	118	76	19.29
23	17	11.81	55	37	14.33	87	57	16.85	119	77	19.37
24	18	11.89	56	38	14.41	88	58	16.93	120	78	19.45
25	19	11.97	57	39	14.49	89	59	17.01	121	79	19.53
26	1A	12.05	58	3A	14.57	90	5A	17.09	122	7A	19.61
27	1B	12.13	59	3B	14.65	91	5B	17.17	123	7B	19.69
28	1C	12.20	60	3C	14.72	92	5C	17.24	124	7C	19.76
29	1D	12.28	61	3D	14.80	93	5D	17.32	125	7D	19.84
30	1E	12.36	62	3E	14.88	94	5E	17.40	126	7E	19.92
31	1F	12.44	63	3F	14.96	95	5F	17.48	127	7F	20.00

Set Partial Display Mode Contrast

C26	C25	C24	C23	C22	C21	C20
00h to 3Fh						

VLC0 voltage (typical) for each Contrast (2) setting

CONT (dec)	CONT (Hex)	V _{LC0} (V)	CONT (dec)	CONT (Hex)	V _{LC0} (V)	CONT (dec)	CONT (Hex)	V _{LC0} (V)	CONT (dec)	CONT (Hex)	V _{LC0} (V)
0	00	5.00	32	20	7.52	64	40	10.04	96	60	12.56
1	01	5.08	33	21	7.60	65	41	10.12	97	61	12.64
2	02	5.16	34	22	7.68	66	42	10.20	98	62	12.72
3	03	5.24	35	23	7.76	67	43	10.28	99	63	12.80
4	04	5.31	36	24	7.83	68	44	10.35	100	64	12.87
5	05	5.39	37	25	7.91	69	45	10.43	101	65	12.95
6	06	5.47	38	26	7.99	70	46	10.51	102	66	13.03
7	07	5.55	39	27	8.07	71	47	10.59	103	67	13.11
8	08	5.63	40	28	8.15	72	48	10.67	104	68	13.19
9	09	5.71	41	29	8.23	73	49	10.75	105	69	13.27
10	0A	5.79	42	2A	8.31	74	4A	10.83	106	6A	13.35
11	0B	5.87	43	2B	8.39	75	4B	10.91	107	6B	13.43
12	0C	5.94	44	2C	8.46	76	4C	10.98	108	6C	13.50
13	0D	6.02	45	2D	8.54	77	4D	11.06	109	6D	13.58
14	0E	6.10	46	2E	8.62	78	4E	11.14	110	6E	13.66
15	0F	6.18	47	2F	8.70	79	4F	11.22	111	6F	13.74
16	10	6.26	48	30	8.78	80	50	11.30	112	70	13.82
17	11	6.34	49	31	8.86	81	51	11.38	113	71	13.90
18	12	6.42	50	32	8.94	82	52	11.46	114	72	13.98
19	13	6.50	51	33	9.02	83	53	11.54	115	73	14.06
20	14	6.57	52	34	9.09	84	54	11.61	116	74	14.13
21	15	6.65	53	35	9.17	85	55	11.69	117	75	14.21
22	16	6.73	54	36	9.25	86	56	11.77	118	76	14.29
23	17	6.81	55	37	9.33	87	57	11.85	119	77	14.37
24	18	6.89	56	38	9.41	88	58	11.93	120	78	14.45
25	19	6.97	57	39	9.49	89	59	12.01	121	79	14.53
26	1A	7.05	58	3A	9.57	90	5A	12.09	122	7A	14.61
27	1B	7.13	59	3B	9.65	91	5B	12.17	123	7B	14.69
28	1C	7.20	60	3C	9.72	92	5C	12.24	124	7C	14.76
29	1D	7.28	61	3D	9.80	93	5D	12.32	125	7D	14.84
30	1E	7.36	62	3E	9.88	94	5E	12.40	126	7E	14.92
31	1F	7.44	63	3F	9.96	95	5F	12.48	127	7F	15.00

Display Mode set: 11h**Set Duty**

This function sets up the display duty cycle for Normal Mode.

DTY1	DTY0	Function
0	0	1/160 Duty...COM0 to COM159
0	1	1/144 Duty...COM8 to COM151
1	0	1/128 Duty...COM16 to COM143
1	1	Cannot be set.

Set Bias

This function specifies the display bias ratio for Normal Display Mode and Partial Display Mode.

If the display mode is switched using the Partial Display command, the display bias ratio setting made using Set Bias will be selected automatically.

Normal Mode

BS12	BS11	BS10	Function
0	0	0	1/11 Bias
0	0	1	1/12 Bias
0	1	0	1/13 Bias
0	1	1	1/14 Bias
1	0	0	1/15 Bias

Partail Mode

BS22	BS21	BS20	Function
0	0	0	1/6 Bias
0	0	1	1/7 Bias
0	1	0	1/8 Bias
0	1	1	1/9 Bias
1	0	0	1/10 Bias

N-line Inversion: 12h

Sets the inversion period for the alternating signal (FR) to an arbitrary number of display lines.

NLI7	NLI6	NLI5	NLI4	NLI3	NLI2	NLI1	NLI0
00h to 9Fh							

00H: Frame inverted

01H: Inverted every line

02H: Inverted every two lines

.....

9EH: Inverted every 158 lines

9FH: Inverted every 159 lines

Color Palette (Red/Green/Blue): 18h to 2Fh

These are the registers which are used for setting the grayscale levels for Palette Selection Mode. Separate palettes can be selected individually for R, G and B, and 16 grayscale levels can be selected from the 32 levels available (GL0 to GL31) and specified individually for R, G and B as 5-bit values in GS0 to GS15.

On a reset, the GS0 to GS15 values for R, G and B become 00H. When using this mode, be sure to set up these registers before executing Display ON.

Reg No.	Color	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18h	Red	*	*	*	GS1					*	*	*	GS0				
19h		*	*	*	GS3					*	*	*	GS2				
1Ah		*	*	*	GS5					*	*	*	GS4				
1Bh		*	*	*	GS7					*	*	*	GS6				
1Ch		*	*	*	GS9					*	*	*	GS8				
1Dh		*	*	*	GS11					*	*	*	GS10				
1Eh		*	*	*	GS13					*	*	*	GS12				
1Fh		*	*	*	GS15					*	*	*	GS14				
20h	Green	*	*	*	GS1					*	*	*	GS0				
21h		*	*	*	GS3					*	*	*	GS2				
22h		*	*	*	GS5					*	*	*	GS4				
23h		*	*	*	GS7					*	*	*	GS6				
24h		*	*	*	GS9					*	*	*	GS8				
25h		*	*	*	GS11					*	*	*	GS10				
26h		*	*	*	GS13					*	*	*	GS12				
27h		*	*	*	GS15					*	*	*	GS14				
28h	Blue	*	*	*	GS1					*	*	*	GS0				
29h		*	*	*	GS3					*	*	*	GS2				
2Ah		*	*	*	GS5					*	*	*	GS4				
2Bh		*	*	*	GS7					*	*	*	GS6				
2Ch		*	*	*	GS9					*	*	*	GS8				
2Dh		*	*	*	GS11					*	*	*	GS10				
2Eh		*	*	*	GS13					*	*	*	GS12				
2Fh		*	*	*	GS15					*	*	*	GS14				

X-adr Area Set: 30h**XASx: Sets up the start address for the display RAM X-adr area.**

XAS7	XAS6	XAS5	XAS4	XAS3	XAS2	XAS1	XAS0
00h to 9Fh							

*: Do not specify an address higher than 9FH.

XAEEx: Sets up the end address for the display RAM X-adr area.

XAE7	XAE6	XAE5	XAE4	XAE3	XAE2	XAE1	XAE0
00h to 9Fh							

*: Do not specify an address higher than 9FH.

Y-adr Area Set: 31h**YASx: Sets up the start address for the display RAM Y-adr area.**

YAS6	YAS5	YAS4	YAS3	YAS2	YAS1	YAS0
00h to 3Fh						

YAEEx: Sets up the end address for the display RAM Y-adr area.

YAE6	YAE5	YAE4	YAE3	YAE2	YAE1	YAE0
00h to 3Fh						

Partial Display Mode: 40h

This command turns Partial Display Mode ON/OFF and sets up the display duty cycle for Partial Display Mode.

PT: Turns Partial Mode ON/OFF.

PT	Function
0	Partial OFF (Normal mode)
1	Partial ON (Partial display mode)

Mode: Selects the display duty cycle for Partial Display Mode.

Mode	Function
0	1/32 Duty
1	1/64 Duty

PDSx: Specifies the start block for Partial Display Mode.

PDS5	PDS4	PDS3	PDS2	PDS1	PDS0
00h to 27h					

Scroll Mode & Area Start: 50H

SM: Sets up Area Scroll Mode.

SM1	SM0	Function
0	0	Full-screen scroll
0	1	Upper screen section scroll
1	0	Lower screen section scroll
1	1	Middle screen section scroll

SASx: Specifies the start RAM block number for the scroll area.
A 4-line RAM block is specified.

SAS5	SAS4	SAS3	SAS2	SAS1	SAS0
00h to 27h					

Set Scroll Area: 51H

SAEx: Specifies the end block number for the scroll area. A 4-line RAM block is specified.
Setting = total number of RAM blocks – number of lower fixed blocks – 1

SAE5	SAE4	SAE3	SAE2	SAE1	SAE0
00h to 27h					

SBNx: Specifies the number of specific blocks. 4-line display duty blocks are specified.
Setting = number of display duty blocks – number of lower fixed blocks – 1

SBN5	SBN4	SBN3	SBN2	SBN1	SBN0
00h to 27h					

RAM block No.

Block start line	Block No.	Block start line	Block No.	Block start line	Block No.
X – ADR = 0	0	X – ADR = 64	16	X – ADR = 128	32
X – ADR = 4	1	X – ADR = 68	17	X – ADR = 132	33
X – ADR = 8	2	X – ADR = 72	18	X – ADR = 136	34
X – ADR = 12	3	X – ADR = 76	19	X – ADR = 140	35
X – ADR = 16	4	X – ADR = 80	24	X – ADR = 144	36
X – ADR = 20	5	X – ADR = 84	25	X – ADR = 148	37
X – ADR = 24	6	X – ADR = 88	26	X – ADR = 152	38
X – ADR = 28	7	X – ADR = 92	27	X – ADR = 156	39
X – ADR = 32	8	X – ADR = 96	28		
X – ADR = 36	9	X – ADR = 100	29		
X – ADR = 40	10	X – ADR = 104	30		
X – ADR = 44	11	X – ADR = 108	31		
X – ADR = 48	12	X – ADR = 112	32		
X – ADR = 52	13	X – ADR = 116	33		
X – ADR = 56	14	X – ADR = 120	34		
X – ADR = 60	15	X – ADR = 124	35		

Scroll Start Block: 52H

This command specifies the scroll start block as a parameter.

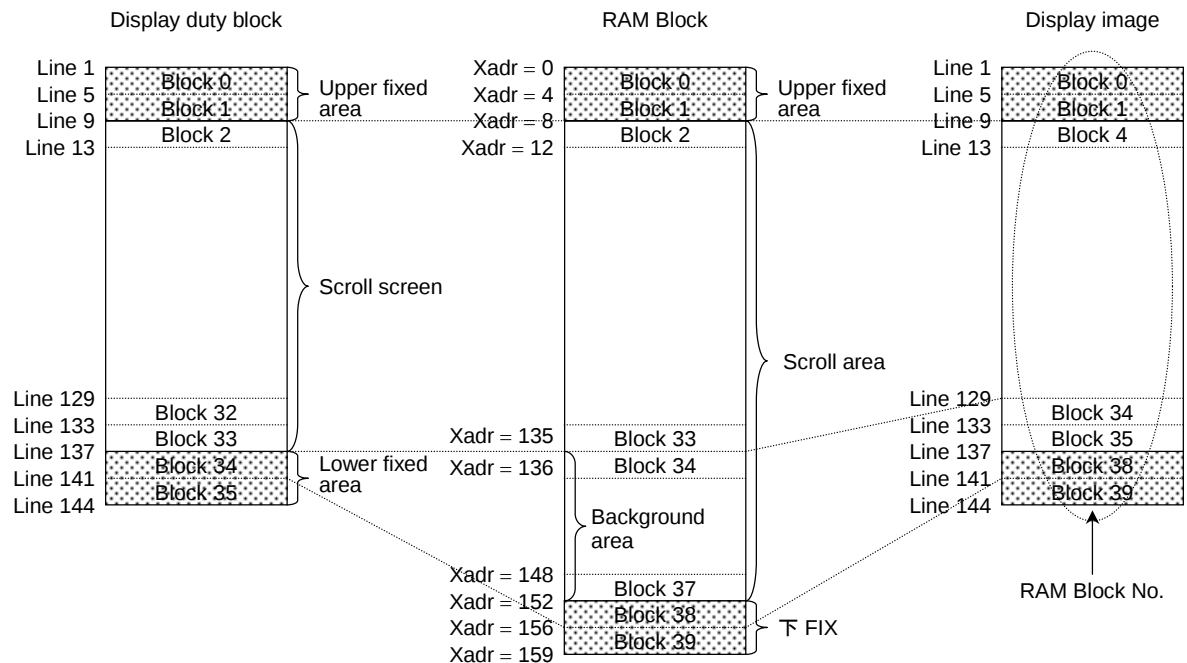
Executing this command causes the specified scroll start block to be displayed as the first data item in the scroll display area. A 4-line RAM block is specified.

SSB5	SSB4	SSB3	SSB2	SSB1	SSB0
00h to 27h					

Setting example

If displays are scrolled up by 8 lines in Middle Screen Section Mode when the duty cycle is 1/144 and lines 1 to 7 and 137 to 144 are fixed:

- Mode : Middle Screen Section Mode
- Scroll area start block : 2
- Scroll area end block : $40 - 2 - 1 = 37$
- Number of specific blocks : $36 - 2 - 1 = 33$
- Scroll start block : 4



Display Data: 70h

DDxx: Accesses the display RAM.

DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
0000h to 0FFFh											

16-Bit Mode

DB11 to DB0 → DD11 to DD0

8-Bit Mode

First access (DB7 to DB0) → DD11 to DD4

Second access (DB3 to DB0) → DD3 to DD0

Toshiba Test Mode: (80h to FFh)

The user cannot access commands in this area during normal use.

Post-Reset (Post-Initialization) States

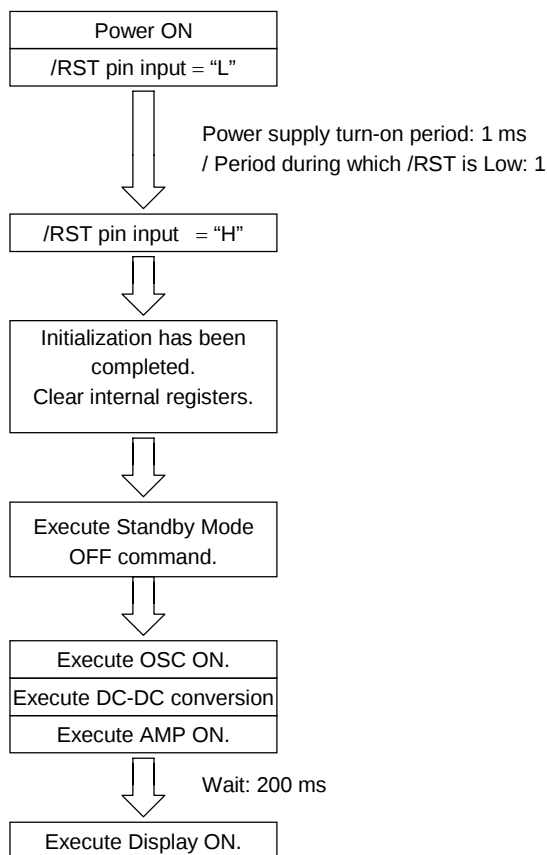
Instruction Name	Reg. No.	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Register set	—	*	*	*	*	*	*	*	*	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0
										0	0	0	0	0	0	0	0
Status read	—	*	*	*	*	*	*	*	*	*	*	X/Y	REV	PT	RMW	DP	STB
												0	0	0	0	0	1
Standby mode	01h	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	STB
																	1
Display ON/OFF	02h	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DP
																	0
Function mode (1)	04h	*	*	DC21	DC20	*	*	DC11	DC10	*	*	*	*	AMP	DCDC	EXT	OSC
				0	0			0	0					0	0	0	0
Function mode (2)	05h	*	*	*	*	*	HRW	RMW	X/Y	*	*	GS	REV	SGM	SWP	CDR	SDR
							0	0	0			0	0	0	0	0	0
Contrast control	10h	*	C26	C25	C24	C23	C21	C21	C20	*	C16	C15	C14	C13	C12	C11	C10
			0	0	0	0	0	0	0		0	0	0	0	0	0	0
Display mode set	11h	*	BS22	BS21	BS20	*	BS12	BS11	BS10	*	*	*	*	*	*	DTY1	DTY0
			0	0	0		0	0	0							0	0
N-line inversion	12h	*	*	*	*	*	*	*	*	NLI7	NLI6	NLI5	NLI4	NLI3	NLI2	NLI1	NLI0
										0	0	0	0	0	0	0	0
Color palette (Red)	18h to 1Fh	*	*	*	GS1/GS3/GS5/GS7/GS9/ GS11/GS13/GS15					*	*	*	GS0/GS2/GS4/GS6/GS8/ GS10/GS12/GS14				
					00h								00h				
Color palette (Green)	20h to 27h	*	*	*	GS1/GS3/GS5/GS7/GS9/ GS11/GS13/GS15					*	*	*	GS0/GS2/GS4/GS6/GS8/ GS10/GS12/GS14				
					00h								00h				
Color palette (Blue)	28h to 2Fh	*	*	*	GS1/GS3/GS5/GS7/GS9/ GS11/GS13/GS15					*	*	*	GS0/GS2/GS4/GS6/GS8/ GS10/GS12/GS14				
					00h								00h				
X-adr area set	30h	XAE7	XAE6	XAE5	XAE4	XAE3	XAE2	XAE1	XAE0	XAS7	XAS6	XAS5	XAS4	XAS3	XAS2	XAS1	XAS0
		0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1
Y-adr area set	31h	*	YAE6	YAE5	YAE4	YAE3	YAE2	YAE1	YAE0	*	YAS6	YAS5	YAS4	YAS3	YAS2	YAS1	YAS0
			0	0	0	0	0	0	0		1	1	1	1	1	1	1
Partial display mode	40h	*	*	PDS5	PDS4	PDS3	PDS2	PDS1	PDS0	*	*	*	*	*	*	MODE	PT
				0	0	0	0	0	0							0	0
Scroll mode & area start	50h	*	*	SAS5	SAS4	SAS3	SAS2	SAS1	SAS0	*	*	*	*	*	*	SM1	SM0
				0	0	0	0	0	0							0	0
Scroll area set	51h	*	*	SBN5	SBN4	SBN3	SBN2	SBN1	SBN0	*	*	SAE5	SAE4	SAE3	SAE2	SAE1	SAE0
				0	0	0	0	0	0			1	0	0	1	1	1
Scroll start block	52h	*	*	*	*	*	*	*	*	*	*	SSB5	SSB4	SSB3	SSB2	SSB1	SSB0
												0	0	0	0	0	0

Summary of Display Outputs and Display Power Supply States for Individual Operation Modes

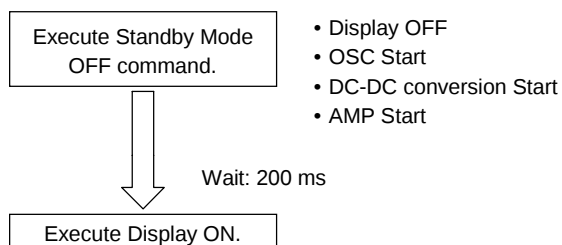
After reset (Standby Mode is ON after a reset.)	• OSC : OFF • DC-DC conversion: OFF • AMP : OFF • SEG output : V_{SS} • COM output : V_{SS} • V_{LC0} to V_{LC5} : V_{SS}
Standby Mode OFF (Normally the display is OFF.)	• OSC : ON (ON command is required after initialization.) • DC-DC conversion: ON (ON command is required after initialization.) • AMP : ON (ON command is required after initialization.) • SEG output : V_{LC2} or V_{LC3} (Display OFF) • COM output : V_{LC1} or V_{LC4} (Display OFF)
Display ON (display output)	• SEG output : Display data is output. • COM output : Scanning is performed.
Display OFF (Display output is stopped.)	• SEG output : V_{LC2} or V_{LC3} (Display OFF) • COM output : V_{LC1} or V_{LC4} (Display OFF)
Standby Mode ON (Sleep state)	• OSC : OFF • DC-DC conversion: OFF • AMP : OFF • SEG output : V_{SS} • COM output : V_{SS} • V_{LC0} to V_{LC5} : V_{SS}

Command Execution and State Transition

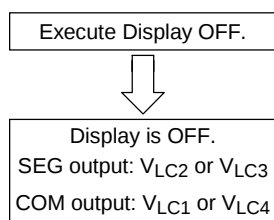
- (1) Reset (Initialize) → Standby Mode OFF → Display ON



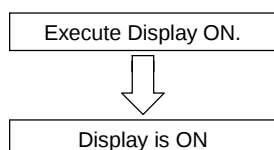
- (2) Return from Standby Mode to display mode



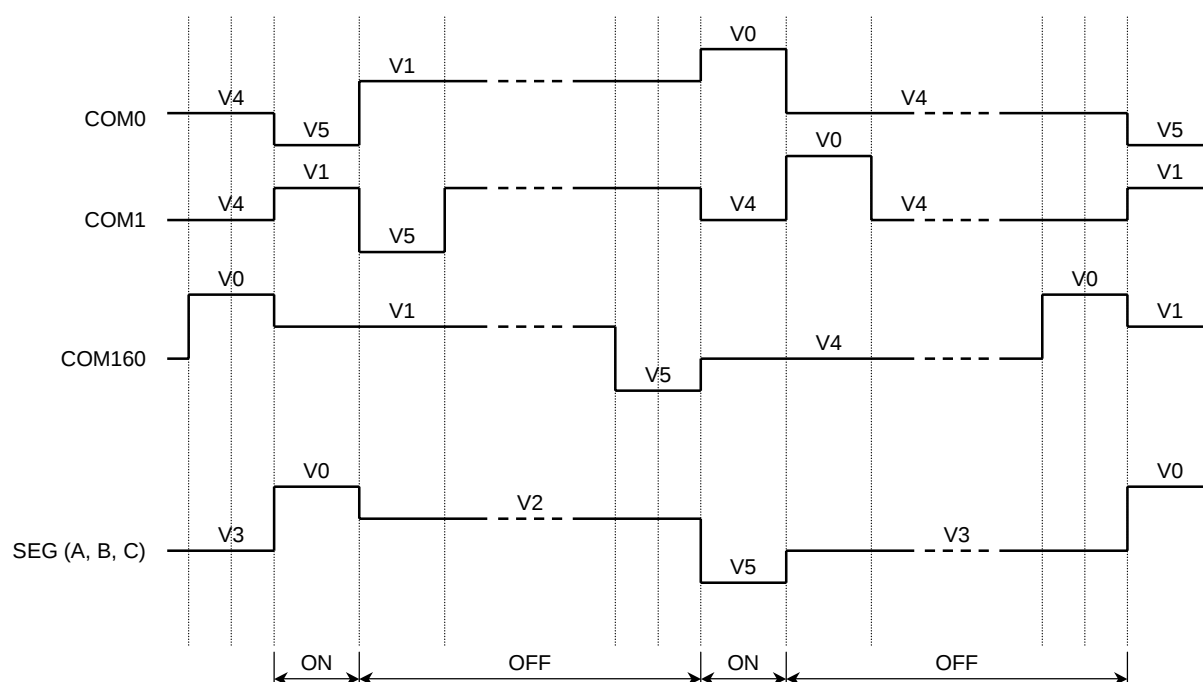
- (3) Display in progress → Display OFF



- (4) Display OFF → Display ON



Lcd Drive Waveform (Normal Display Mode)



LCD drive timing chart (1/160 duty)

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}, V_{IN} (Note 1)	-0.3 to 6.0	V
Supply Voltage (2)	$V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}, V_{CC1}, V_{CC2}$	$V_{SS} + 22.0$ to $V_{SS} - 0.3$	V
Input Voltage	V_{in} (Note 1), (Note 2)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	T_{opr}	-30 to 85	°C
Storage Temperature	T_{stg}	-55 to 125	°C

Note 1: Value with reference to $V_{SS} = 0$ V

Note 2: Does not include $V_{CC1}, V_{CC2}, V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}$ and V_{LC5} .

This setting is suitable for inputs or a data bus.

Electrical Characteristics 1

(Conditions: Unless otherwise specified, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }3.3\text{ V}$, $V_{CC} = 20.0\text{ V}$, $T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Test Circuit	Test Conditions	Min	Typ.	Max	Unit	Applicable
Operating voltage (1)		V_{DD}	—	—	1.7	—	3.3	V	V_{DD}
Operating voltage (2)		V_{IN}	—	—	2.7	—	3.3	V	V_{IN}
Operating voltage (3)	Normal display	V_{CC}	—	—	5.0 – V_{SS}	—	20.0 – V_{SS}	V	V_{CC}
	Partial display	V_{CC}		—	4.0 – V_{SS}	—	20.0 – V_{SS}	V	
Input voltage	High level	V_{IH}	—	—	0.8 $\times V_{DD}$	—	V_{DD}	V	DB0 to DB15, D/I, /WR, /RD, /CS1, CS2, D/I, P/S, 68/80, SI, SCK, /RST, /STB
	Low level	V_{IL}		—	0	—	0.2 $\times V_{DD}$	V	
Output voltage	High level	V_{OH}	—	$I_{OH} = -400\text{ }\mu\text{A}$	$V_{DD} - 0.2$	—	V_{DD}	V	DB0 to DB15, SO
	Low level	V_{OL}		$I_{OL} = 400\text{ }\mu\text{A}$	0	—	0.2	V	
Segment driver on-resistance	Normal display mode	R_{col}	—	(Note 3)	—	2.0	3.0	$k\Omega$	SEG
Common driver ON-resistance	Normal display mode	R_{row}	—	(Note 3)	—	1.2	2.0	$k\Omega$	COM
Input leakage current		I_{IL}	—	$V_{inp} = V_{DD}\text{ to GND}$	-1	—	1	μA	DB0 to DB15, D/I, /WR, /RD, /CS1, CS2, RSI, P/S, WLS, SI, SO, SCK, /RST, /STB
Operating frequency		f_{osc}	—	(Note 7)	—	168	—	kHz	OSC
External clock input frequency		f_{ex}	—	(Note 7)	—	168	—	kHz	OSC
External clock duty		f_{duty}	—	—	45	50	55	%	OSC
External clock rise/fall time		t_r/t_f	—	—	—	—	50	ns	OSC
Current consumption (1)		I_{SS1}	—	(Note 4)	—	300	TBD	μA	V_{SS}
Current consumption (2)		I_{SS2}	—	(Note 5)	—	100	TBD	μA	V_{SS}
Current consumption (5)		I_{SSSTB}	—	(Note 6)	-1	—	1	μA	V_{SS}

Note 3: $V_{CC} = 10.0\text{ V}$, Load current $\pm 100\text{ }\mu\text{A}$, 1/11 bias

Note 4: $V_{DD} = 3.0\text{ V}$, $V_{CC} = 18.0\text{ V}$ ($\times 7$ booster), no data access, internal clock (OSC = 168 kHz), no load, 1/14 bias, 1/160 duty, op-amp ON, regulator ON, Normal Display Mode, display pattern: all-white

Note 5: $V_{DD} = 3.0\text{ V}$, $V_{CC} = 10\text{ V}$ ($\times 4$ booster), no data access, internal clock (OSC = 67.2 kHz), no load, 1/9 bias, 1/64 duty, op-amp ON, regulator ON, Partial Display Mode, display pattern: all-white

Note 6: $V_{DD} = 3.3\text{ V}$, $V_{CC} - V_{SS} = 22.0\text{ V}$, /STB = "L"

Note 7: 1/160 duty, $f_{FR} = 70\text{ Hz}$

Electrical Characteristics 2

(Conditions: Unless otherwise specified, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }3.3\text{ V}$, $V_{CC} = 15.5\text{ V}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit	Applicable
Output voltage (×3 booster)	V_{O1}	(1)	(Note 8)	TBD	8.7	—	V	V_{OUT}
Output voltage (×4 booster)	V_{O2}	(2)	(Note 9)	TBD	11.6	—	V	V_{OUT}
Output voltage (×5 booster)	V_{O3}	(3)	(Note 10)	TBD	14.5	—	V	V_{OUT}
Output voltage (×6 booster)	V_{O4}	(4)	(Note 11)	TBD	17.4	—	V	V_{OUT}
Output voltage (×7 booster)	V_{O5}	(5)	(Note 12)	TBD	18.3	—	V	V_{OUT}
Output voltage (×8 booster)	V_{O6}	(6)	(Note 13)	TBD	20.0	—	V	V_{OUT}

Note 8: $V_{IN} = 3.0\text{ V}$, $V_{CC} = 8.7\text{ V}$ (external power supply input), $C_n+/C_n- = 1.0\text{ }\mu\text{F}$, $V_{OUT} - V_{SS} = 1.0\text{ V}$, $OSC = 67.2\text{ kHz}$, contrast = max, $T_a = 25^\circ\text{C}$, $I_{load} = 200\text{ }\mu\text{A}$

Note 9: $V_{IN} = 3.0\text{ V}$, $V_{CC} = 11.6\text{ V}$ (external power supply input), $C_n+/C_n- = 1.0\text{ }\mu\text{F}$, $V_{OUT} - V_{SS} = 1.0\text{ V}$, $OSC = 67.2\text{ kHz}$, contrast = max, $T_a = 25^\circ\text{C}$, $I_{load} = 200\text{ }\mu\text{A}$

Note 10: $V_{IN} = 3.0\text{ V}$, $V_{CC} = 14.5\text{ V}$ (external power supply input), $C_n+/C_n- = 1.0\text{ }\mu\text{F}$, $V_{OUT} - V_{SS} = 1.0\text{ V}$, $OSC = 67.2\text{ kHz}$, contrast = max, $T_a = 25^\circ\text{C}$, $I_{load} = 200\text{ }\mu\text{A}$

Note 11: $V_{IN} = 3.0\text{ V}$, $V_{CC} = 17.4\text{ V}$ (external power supply input), $C_n+/C_n- = 1.0\text{ }\mu\text{F}$, $V_{OUT} - V_{SS} = 1.0\text{ V}$, $OSC = 168\text{ kHz}$, contrast = max, $T_a = 25^\circ\text{C}$, $I_{load} = 500\text{ }\mu\text{A}$

Note 12: $V_{IN} = 2.7\text{ V}$, $V_{CC} = 18.3\text{ V}$ (external power supply input), $C_n+/C_n- = 1.0\text{ }\mu\text{F}$, $V_{OUT} - V_{SS} = 1.0\text{ V}$, $OSC = 168\text{ kHz}$, contrast = max, $T_a = 25^\circ\text{C}$, $I_{load} = 500\text{ }\mu\text{A}$

Note 13: $V_{IN} = 2.7\text{ V}$, $V_{CC} = 20.0\text{ V}$ (external power supply input), $C_n+/C_n- = 1.0\text{ }\mu\text{F}$, $V_{OUT} - V_{SS} = 1.0\text{ V}$, $OSC = 168\text{ kHz}$, contrast = max, $T_a = 25^\circ\text{C}$, $I_{load} = 500\text{ }\mu\text{A}$

Electrical Characteristics 3

(Conditions: Unless otherwise specified, $V_{SS} = 0\text{ V}$, $V_{DD} = V_{IN} = 2.7\text{ to }3.3\text{ V}$, $V_{CC} = 15.5\text{ V}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit	Applicable
Regulator reference high voltage (1)	V_{HR1}	—	(Note 14)	19.95	20.00	20.05	V	V_{CC}
Regulator reference high voltage (2)	V_{HR2}	—	(Note 15)	14.95	15.00	15.05	V	V_{CC}
Regulator reference high voltage Temperature gradient	V_{HRINC}	—	(Note 14) $T_a = -20\text{ to }60^\circ\text{C}$	—	-0.00	—	%/ $^\circ\text{C}$	V_{CC}
Regulator reference high voltage Temperature gradient variation	ΔV_{HRINC}	—	(Note 14) $T_a = -20\text{ to }60^\circ\text{C}$	-0.02	—	0.02	%/ $^\circ\text{C}$	V_{CC}

Note 14: $V_{DD} = V_{IN} = 3.0\text{ V}$, $V_{CC} = 20\text{ V}$ (external supply), contrast = max, no display load, Normal Display Mode

Note 15: $V_{DD} = V_{IN} = 3.0\text{ V}$, $V_{CC} = 15\text{ V}$ (external supply), contrast = max, no display load, Normal Display Mode

Electrical Characteristics 4

(Conditions: Unless otherwise specified, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }3.3\text{ V}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit	Applicable
Op-amp output voltage offset (1)	V_{opoff}	—	(Note 16)	TBD	—	TBD	mV	V_{LC0} , V_{LC1} , V_{LC2} , V_{LC3} , V_{LC4}
Op-amp output voltage offset (2)	V_{opoffs1}	—	(Note 17)	TBD	—	TBD	mV	V_{LC0} , V_{LC1} , V_{LC2} , V_{LC3} , V_{LC4}
Op-amp output voltage offset (3)	V_{opoffs2}	—	$I_{\text{load}} = \pm 300\text{ }\mu\text{A}$ (Note 17)	TBD	—	TBD	mV	V_{LC0} , V_{LC1} , V_{LC2} , V_{LC3} , V_{LC4}

Note 16: $V_{DD} = 2.7\text{ to }3.3\text{ V}$, $V_{SS} = 0\text{ V}$, 1/15 bias, 1/160 duty, $V_{CC} = 20.0\text{ V}$, op-amp ON, no load

V_{LC0} : $V_{\text{LC0}} = V_{\text{opoff}}$

V_{LC1} : $(V_{\text{LC0}} \div 14/15) - V_{\text{LC1}} = V_{\text{opoff}}$

V_{LC2} : $(V_{\text{LC0}} \div 13/15) - V_{\text{LC2}} = V_{\text{opoff}}$

V_{LC3} : $(V_{\text{LC0}} \div 2/15) - V_{\text{LC3}} = V_{\text{opoff}}$

V_{LC4} : $(V_{\text{LC0}} \div 1/15) - V_{\text{LC4}} = V_{\text{opoff}}$

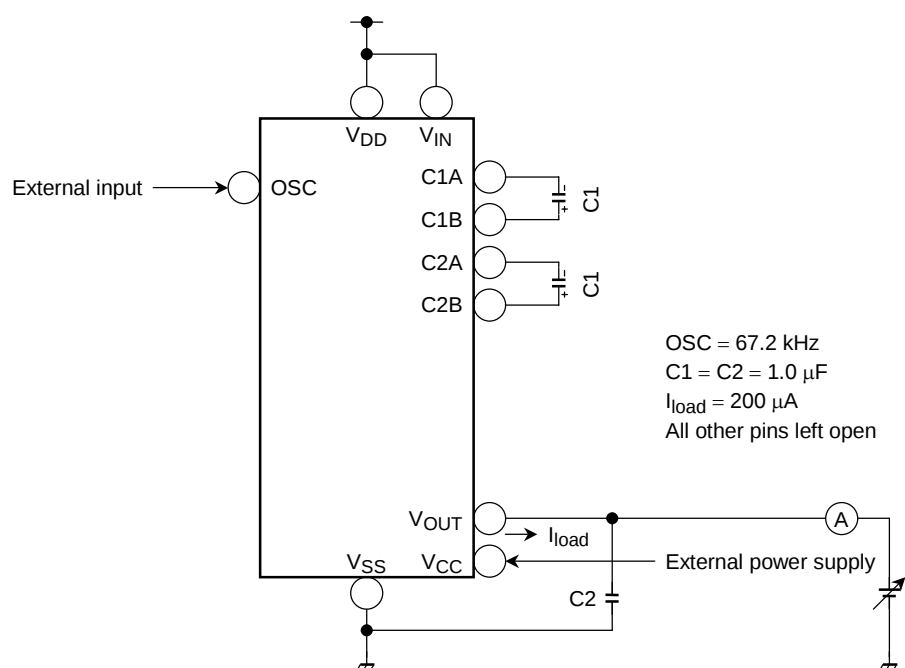
Note 17: $V_{DD} = 2.7\text{ to }3.3\text{ V}$, $V_{SS} = 0\text{ V}$, 1/15 bias, 1/160 duty, $V_{CC} = 20.0\text{ V}$, op-amp ON, no load

$V_{\text{opoff1}} = \{ (V_{\text{LC1}} - V_{\text{LC2}}) - (V_{\text{LC0}} - V_{\text{LC1}}) \} + \{ (V_{\text{LC3}} - V_{\text{LC4}}) - (V_{\text{LC4}} - V_{\text{LC5}}) \}$

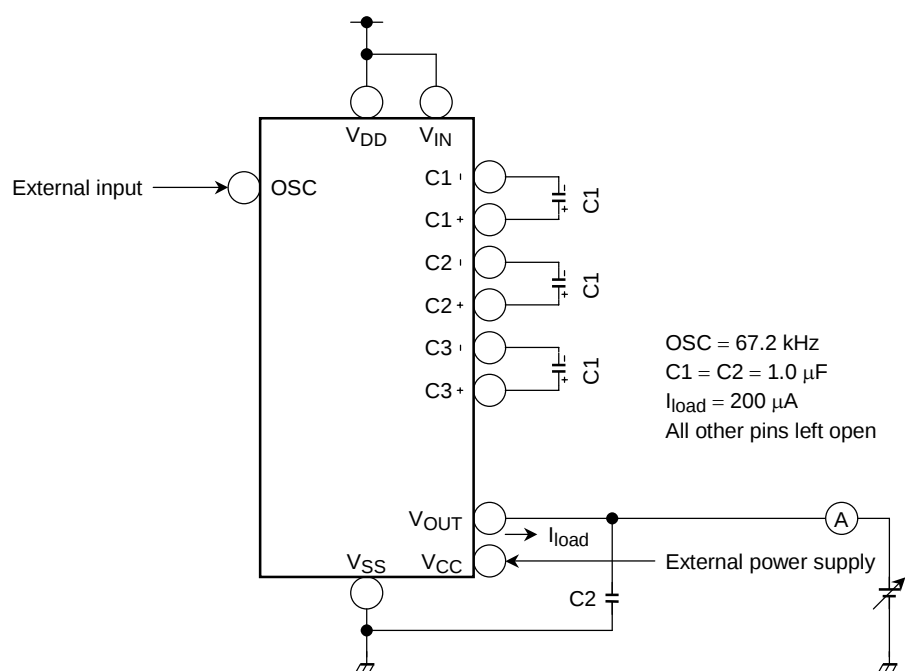
$V_{\text{opoff2}} = \{ (V_{\text{LC1}} - V_{\text{LC2}}) - (V_{\text{LC0}} - V_{\text{LC1}}) \} + \{ (V_{\text{LC3}} - V_{\text{LC4}}) - (V_{\text{LC4}} - V_{\text{LC5}}) \}$

Test Circuit

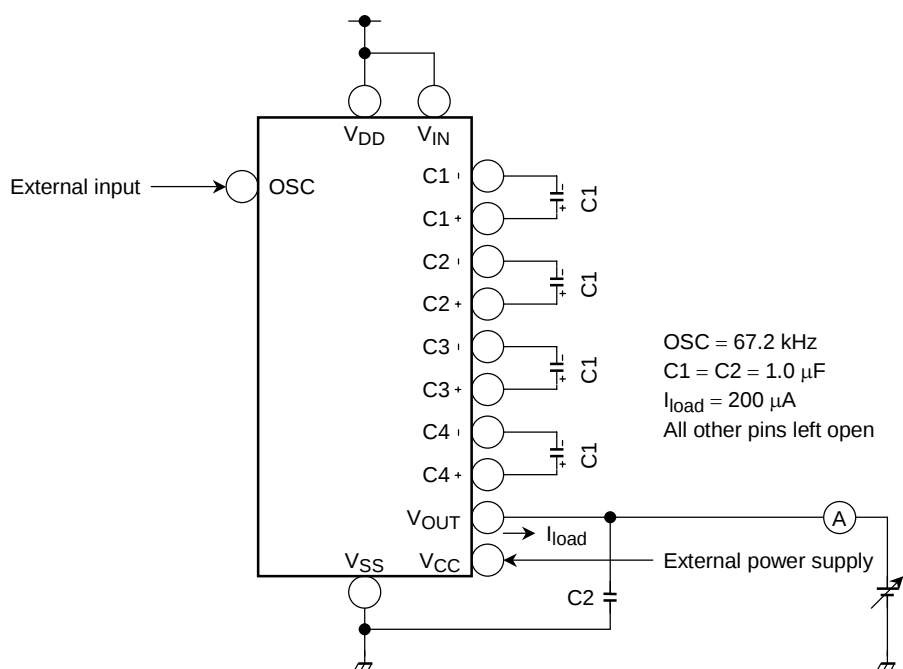
(1) With $\times 3$ booster



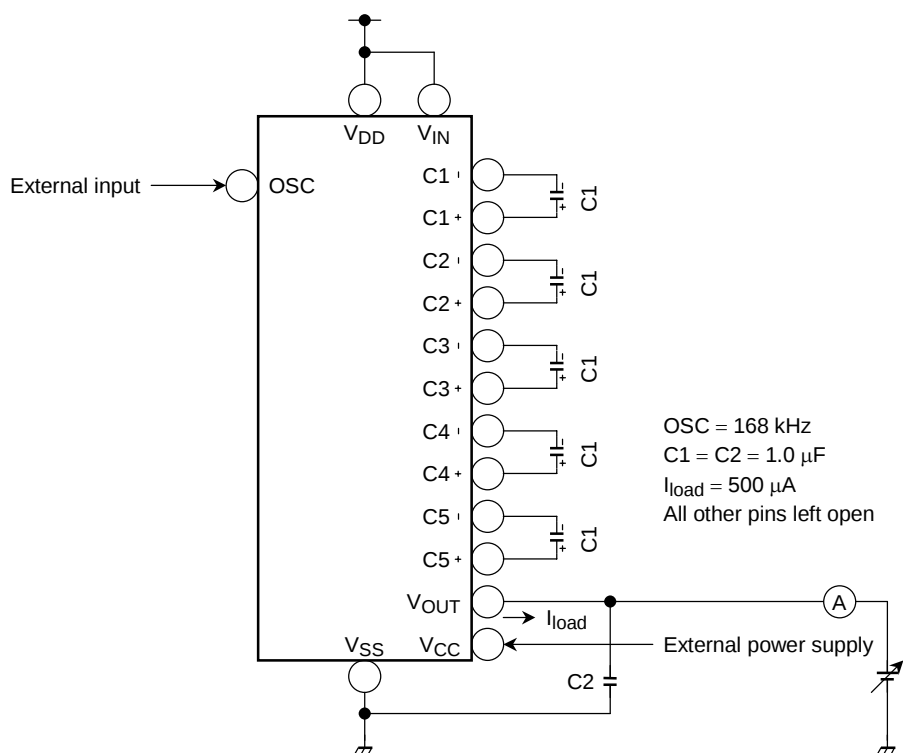
(2) With $\times 4$ booster



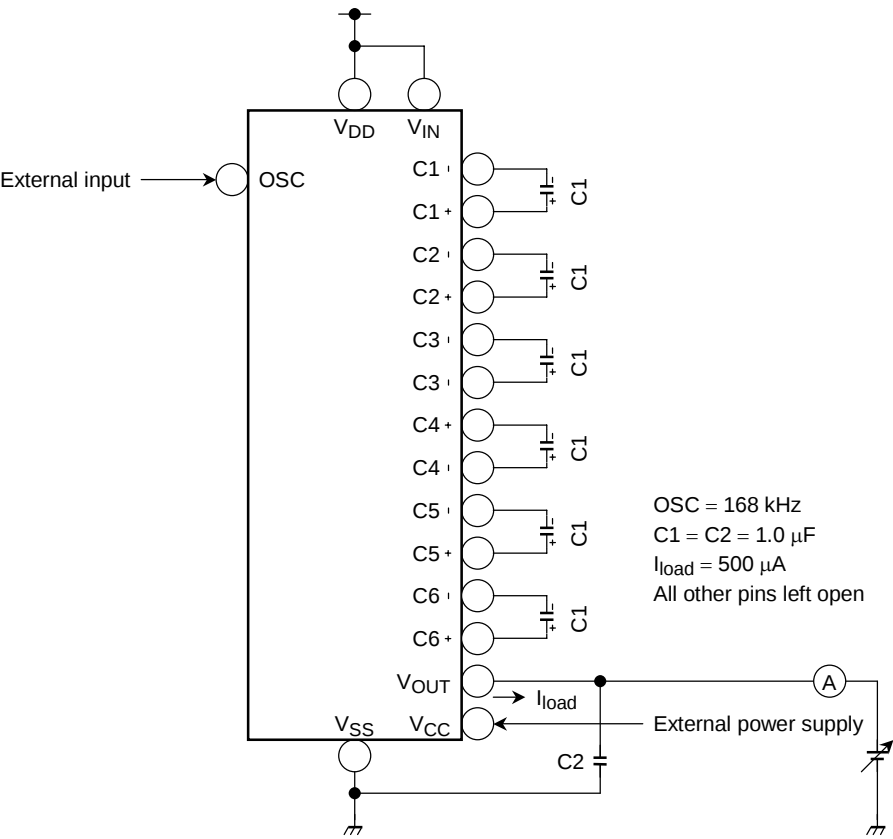
(3) With × 5 booster



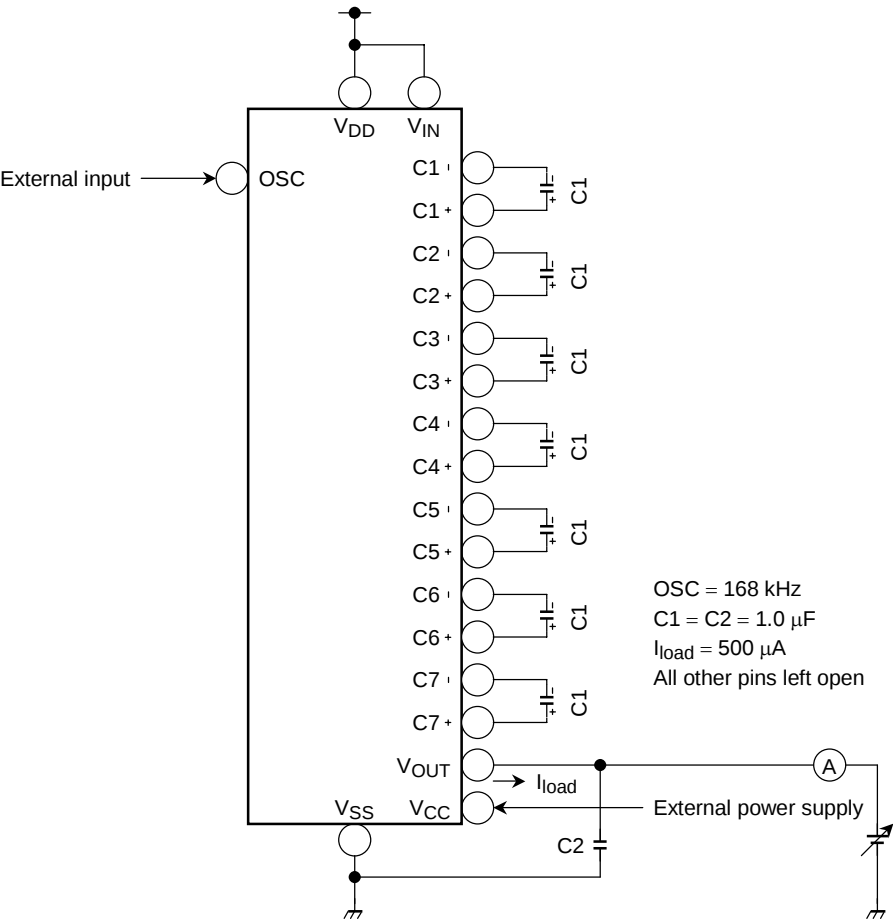
(4) With × 6 booster



(5) With × 7 booster



(6) With × 8 booster



The diagram illustrates the timing relationships for the AD9080. The signals and their timing parameters are as follows:

- D/I:** Data/Address input. High-level voltage is V_{IH} , low-level voltage is V_{IL} . The address hold time is t_{AH} .
- /CS1 (CS2 = H):** Chip select 1. Low-level voltage is V_{IL} . The address setup time is t_{AS} , and the chip select pulse width is $PWEL$.
- /WR:** Write strobe. High-level voltage is V_{IH} , low-level voltage is V_{IL} . The setup time before the data write is t_{Ef} , and the hold time after the data write is t_{Ef} .
- Data Write:** Data bus during a write operation. High-level voltage is V_{IH} , low-level voltage is V_{IL} . The data setup time is t_{DS} , and the data hold time is t_{DHW} .
- /RD:** Read strobe. High-level voltage is V_{IH} , low-level voltage is V_{IL} . The setup time before the data read is t_{Ef} , and the hold time after the data read is t_{Er} .
- Data Read:** Data bus during a read operation. High-level voltage is V_{OH} , low-level voltage is V_{OL} . The data setup time is t_{DD} , and the data hold time is t_{DHR} .
- t_{cycE} :** The total cycle time for the data read operation.

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	100		ns
Enable pulse width	P_{WEL}	TBD		ns
Enable rise/fall time	t_{Er}, t_{Ef}		TBD	ns
Address set-up time	t_{AS}	TBD		ns
Address hold time	t_{AH}	TBD		ns
Data set-up time	t_{DS}	TBD		ns
Write data hold time	t_{DHW}	TBD		ns
Data delay time	t_{DD} (Note 18)		TBD	ns
Read data hold time	t_{DHR} (Note 18)	TDB		ns

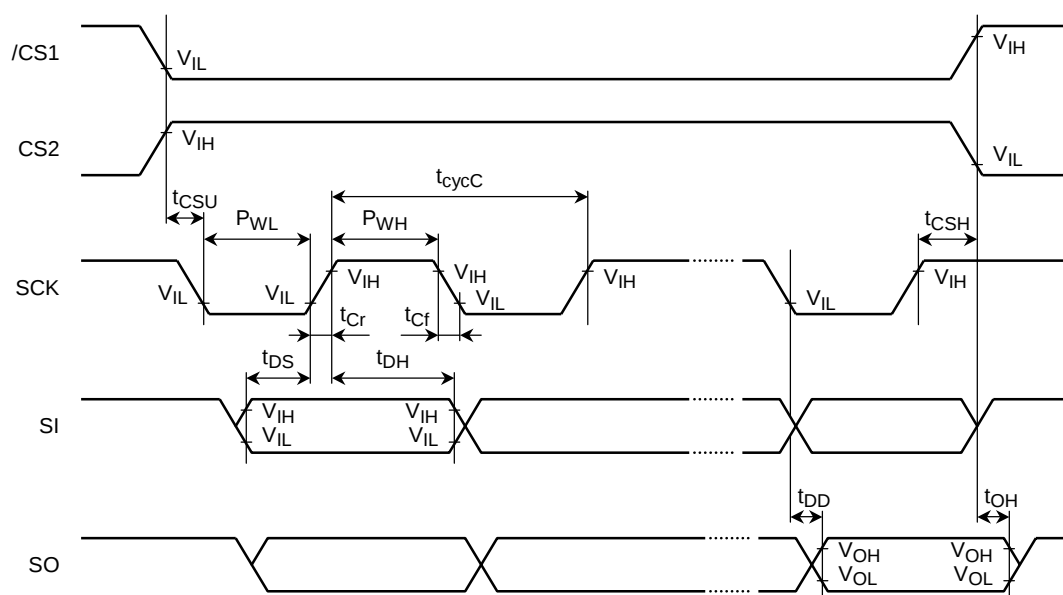
Note 18: When a load circuit as shown in the figure is connected

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	100		ns
Enable pulse width	P_{WEH}	TBD		ns
Enable rise/fall time	t_{Er}, t_{Ef}		TBD	ns
Address set-up time	t_{AS}	TBD		ns
Address hold time	t_{AH}	TBD		ns
Data set-up time	t_{DS}	TBD		ns
Write data hold time	t_{DHW}	TBD		ns
Data delay time	t_{DD} (Note 19)		TBD	ns
Read data hold time	t_{DHR} (Note 19)	TDB		ns

DB0 to 

Note 19: When a load circuit as shown in the figure is connected

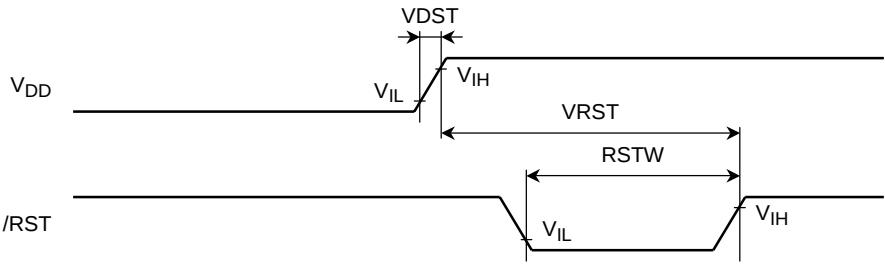
Switching Characteristics 3 (Serial Interface)



(Conditions: Unless Otherwise Specified, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.4\text{ to }3.3\text{ V}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Min	Max	Unit
Clock cycle time	t_{cycC}	100		ns
Clock pulse width	P_{WCL}, P_{WCH}	40		ns
Clock rise/fall time	t_{Cr}, t_{Cf}		10	ns
Chip select set-up time	t_{CSU}	20		ns
Chip select hold time	t_{CSH}	50		ns
Data set-up time	t_{DS}	30		ns
Write data hold time	t_{DH}	20		ns
Data output delay time	t_{DD}		30	ns
Data output hold time	t_{OH}	10		ns

Switching Characteristics 4



(Conditions: Unless Otherwise Specified, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }3.3\text{ V}$, $V_{CC} = 15.5\text{ V}$, $T_a = 25^{\circ}\text{C}$)

Characteristics	Symbol	Min	Max	Unit
V_{DD} rise time	VDST	—	1	ms
Reset hold time	VRST	1	—	μs
Reset pulse width	RSTW	1	—	μs

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