To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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M62501P/FP

PWM IC for the Synchronized Deflection System Control

REJ03D0857-0200
Rev.2.00
Jun 14, 2006

General Description

The M62501P/FP is a controller for a deflection system of CRT display monitors. It performs a stable PWM control over a wide fluctuation of external signals, thanks to the built-in trigger mode oscillator. The IC is suitable for an application to a high voltage drive of monitors because of its following circuits and functions;

- low voltage malfunction protection circuit,
- over or under voltage protection circuit for a control line,
- soft-start function.

It is also applicable to a horizontal output correction.

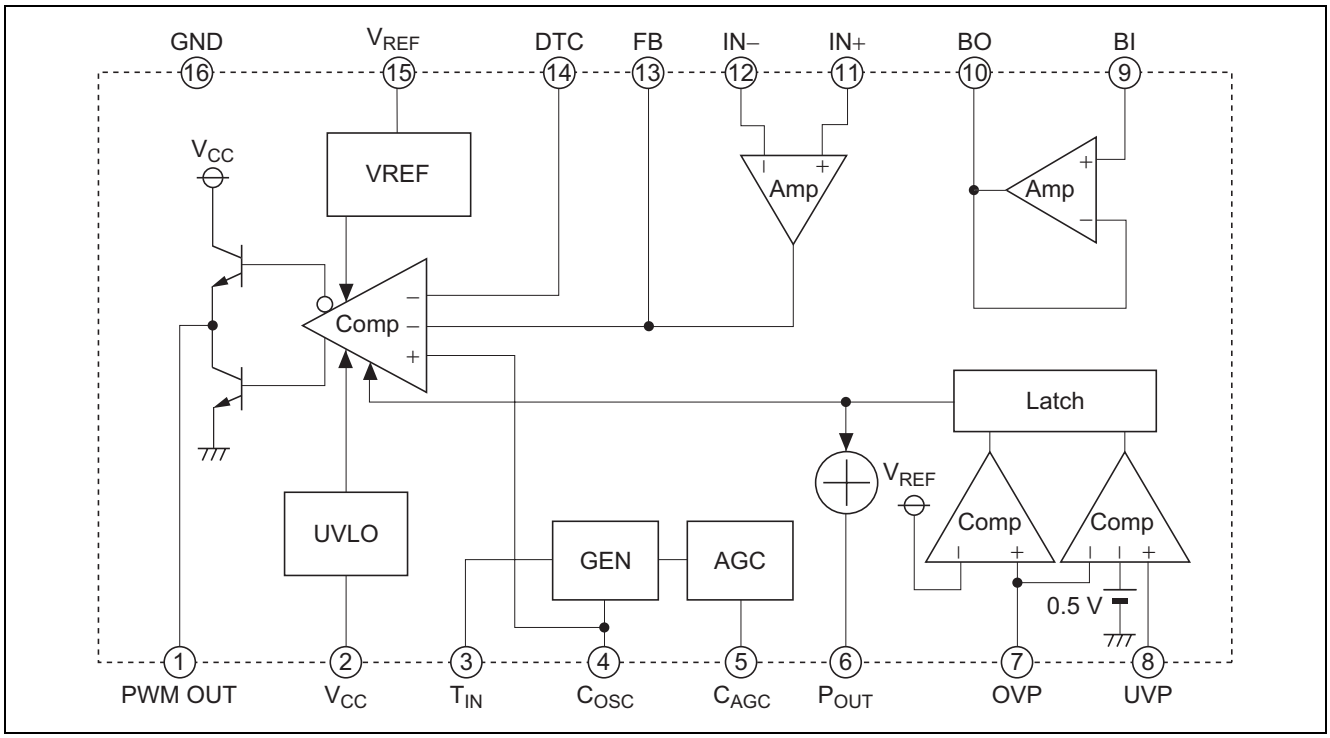
Features

- PWM output synchronized with external signals
- Wide pulse width modulation control frequency
  15 kHz to 150 kHz
- Soft start function
- The under voltage output malfunction protection circuit
  start V_{CC} > 9 V
  stop V_{CC} < 6 V
- Built-in over voltage protection (OVP) and under voltage protection (UVP) control

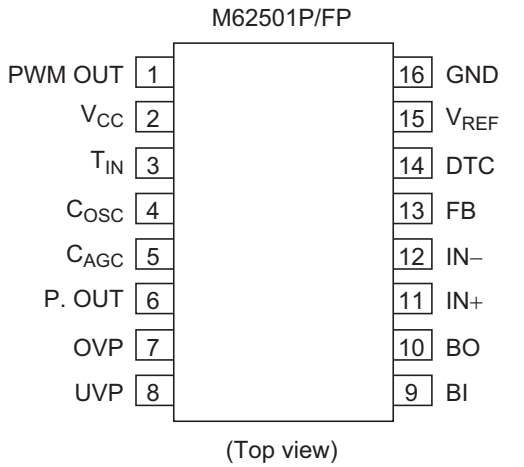
Application

CRT display monitor

Block Diagram



Pin Arrangement



Outline: PRDP0016AA-A (16P4) [P]
PRSP0016DA-A (16P2S-A) [FP]

Terminal Number and The Facility

PIN No.	Symbol	Functional Description
1	PWM OUT	PWM output
2	V_{CC}	Power supply
3	T_{IN}	Trigger input
4	C_{OSC}	Setting oscillating frequency
5	C_{AGC}	AGC setting
6	P.OUT	Error signal output
7	OVP	Input of over voltage protection
8	UVP	Input of under voltage protection
9	BI	Positive input of buffer Amp.
10	BO	Output of buffer Amp.
11	IN+	Positive input of Op-Amp.
12	IN–	Negative input of Op-Amp.
13	FB	Output of Op-Amp.
14	DTC	Dead time control (Soft start function)
15	V_{REF}	Output of reference voltage (5 V)
16	GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

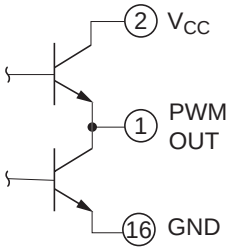
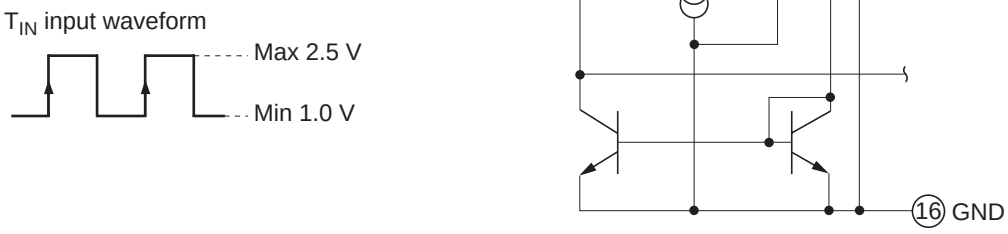
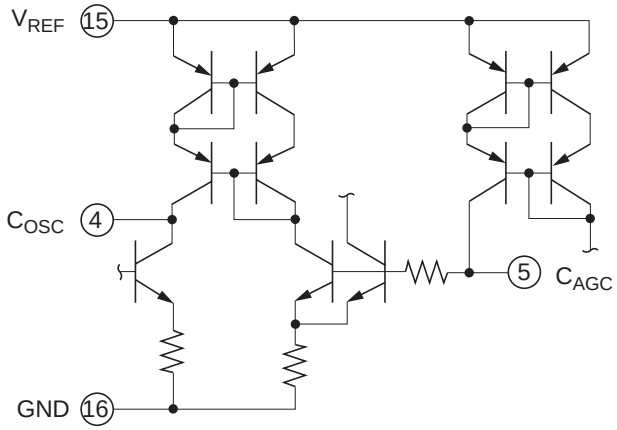
Item	Symbol	Ratings		Unit	Conditions
Supply voltage	V_{CC}	15		V	
Output voltage	V_{OUT}	15		V	
Output current	I_{OUT}	±100		mA	
Error amplifier input common mode voltage	V_{ICM}	–0.3 to V_{CC}		V	
Error amplifier differential input voltage	V_{ID}	V_{CC}		V	
Power dissipation	Pd	P	FP	mW	
		1200	650		
Thermal derating	Kθ	P	FP	mW/°C	Ta ≥ 25°C
		9.6	5.2		
Operating temperature	Topr	–20 to +75		°C	
Storage temperature	Tstg	–40 to +150		°C	

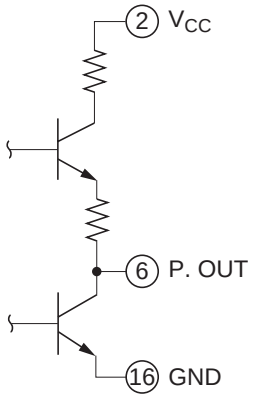
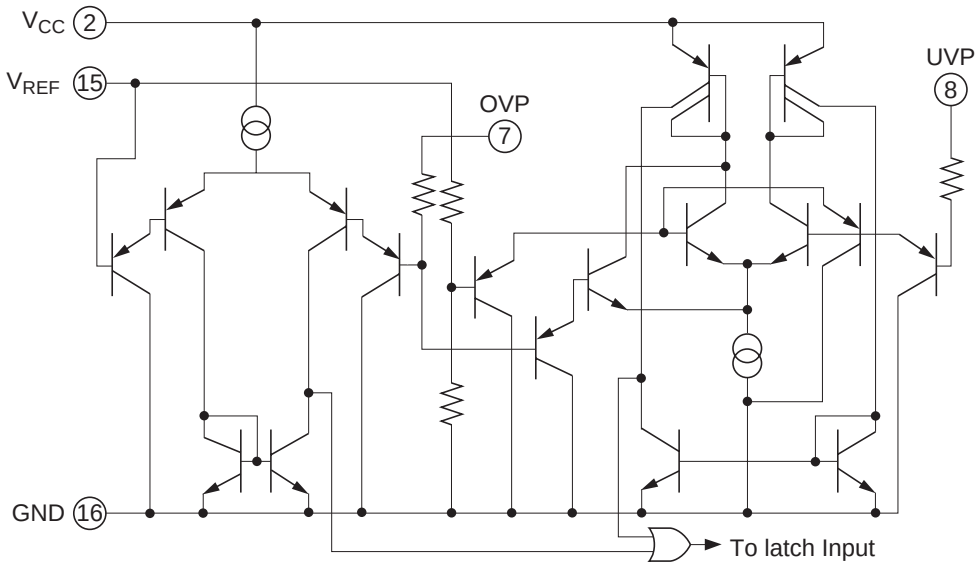
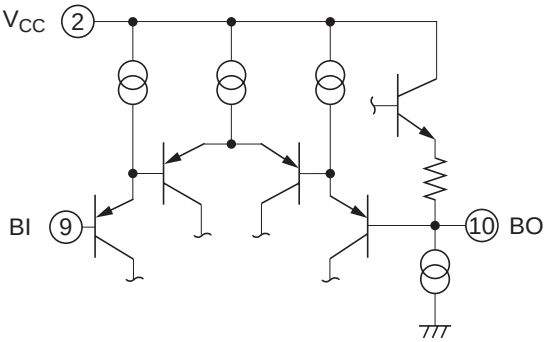
Electrical Characteristics

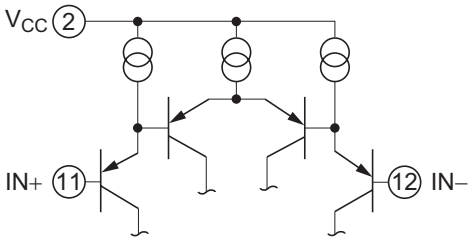
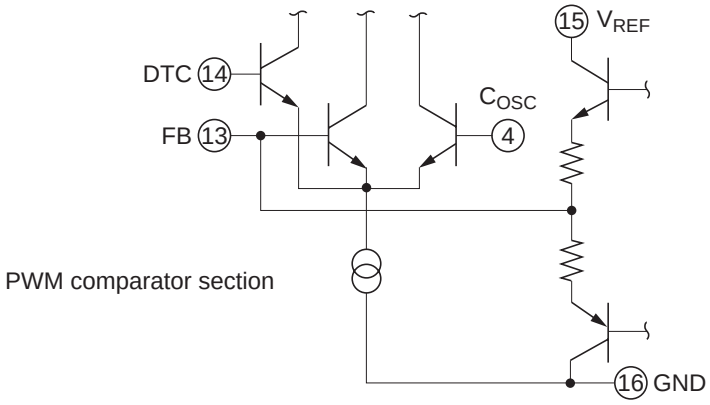
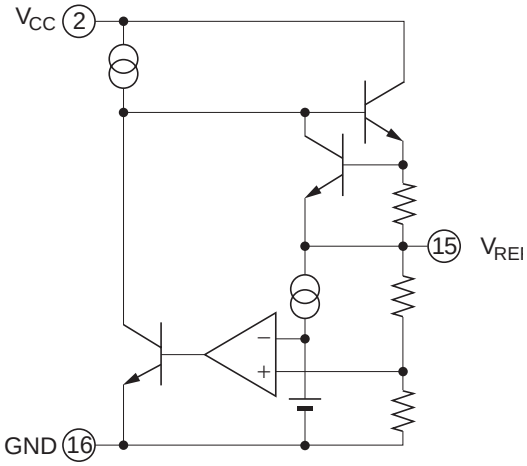
(V_{CC} = 12 V, TIN = 40 kHz, Ta = 25°C, unless otherwise noted)

Block	Item	Symbol	Limits			Unit	Test Conditions
			Min	Typ	Max		
All device	Range of power supply	V_{CC}	V_{CC} OFF		14	V	
	Circuit current	I_{CC}	—	20	—	mA	Output off mode
Reference voltage section	Reference voltage	V_{REF}	4.80	5.00	5.20	V	I_{REF} = –5 mA
	Input regulation	Reg-in	—	1.0	10	mV	V_{CC} = 7 to 14 V I_{REF} = –5 mA
	Load regulation	Reg-L	—	2.0	20	mV	I_{REF} = 0 to –5 mA
	Reference voltage thermal coefficient	TC_{VREF}	—	0.01	—	%/°C	
	Maximum reference current	$I_{REF\ MAX}$	—	–30	—	mA	
	Short-circuit current	Is	—	–30	—	mA	
Error Amp.	Input offset voltage	V_{IO}	—	—	7	mV	
	Input bias current	I_{Ib}	–100	—	—	nA	
	Input offset current	I_{IO}	–100	—	100	nA	
	Common mode input voltage range	V_{ICM}	–0.3	—	V_{CC} – 2	V	
	Open loop transmission gain	AV	70	110	—	dB	
	Slew rate	SR	—	4	—	V/µs	
	Output voltage range	V_{OR}	0.3	—	V_{REF} – 1.5	V	
	Output sink current	Isink	10	—	—	mA	
	Output source current	Isource	—	—	–10	mA	
Buffer Amp.	Input bias current	Ib	–20	—	—	nA	
	Slew rate	SR	—	4	—	V/µs	
	Output voltage	V_{OR}	0.3	—	V_{CC} – 2.5	V	
	Output sink current	Isink	2	—	—	mA	
	Output source current	Isource	—	—	–10	mA	
Oscillator	Oscillation frequency	f_{OSC}	15	—	150	kHz	
	The oscillator waveform bound voltage	$V_{OSC\ H}$	—	3.5	—	V	
	The oscillator waveform lower limit voltage	$V_{OSC\ L}$	—	1.5	—	V	
	High level of TIN	$V_{TIN\ H}$	2.5	—	V_{CC}	V	
	Low level of TIN	$V_{TIN\ L}$	—	—	1.0	V	
PWM output section	Output saturation voltage L	$V_{sat\ L}$	—	0.7	1.4	V	I_O = 100 mA
	Output saturation voltage H	$V_{sat\ H}$	9.5	10.5	—	V	I_O = –100 mA
UVLO section	ON threshold voltage	$V_{TH\ ON}$	8.0	9.0	10.0	V	
	OFF threshold voltage	$V_{TH\ OFF}$	5.4	6.0	6.6	V	
OVP section	OVP terminal threshold voltage	$V_{TH\ OVP}$	4.75	5.00	5.25	V	
	OVP terminal input current	$I_{IN\ OVP}$	—	—	1.0	µA	
UVP section	Input offset voltage	V_{UVPO}	—	—	7	mV	
	UVP terminal input current	$I_{IN\ UVP}$	—	—	1.0	µA	
P.OUT section	Output saturation voltage	Vsat	—	—	0.4	V	I_{PO} = 10 mA
	Output leakage current	I_L	—	—	1.0	µA	V_{PO} = 12 V

Terminal Functional Description and Equivalent Circuit

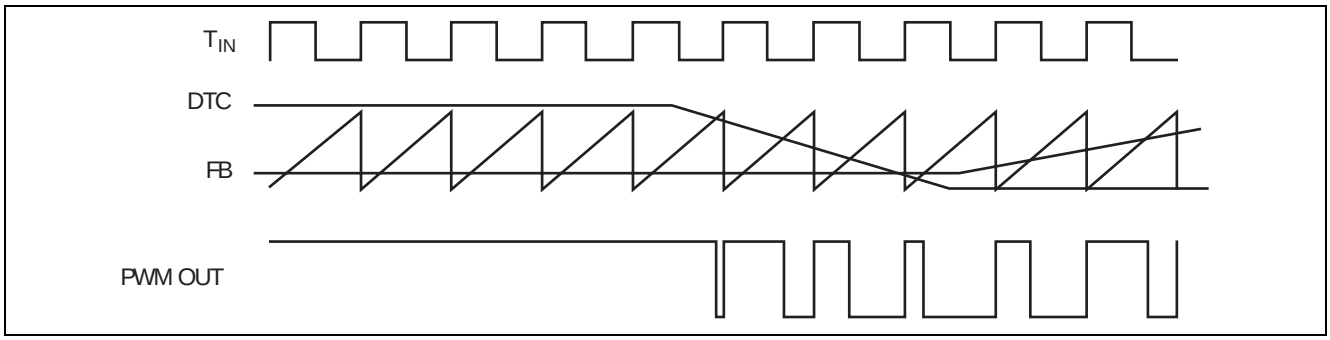
Terminal No.	Symbol	Function and Terminal Circumscription Circuitry
1	PWM OUT	PWM output terminal • The PWM output synchronized with the T_{IN} input. • Output "H" level = 10.5 V typ (The output load current: –100 mA, V_{CC} = 12 V) • Output "L" level = 0.7 V typ (The output load current: +100 mA, V_{CC} = 12 V) 
2	V_{CC}	Power supply terminal
3	T_{IN}	Trigger input terminal • Frequency range 15 kHz to 150 kHz • It takes in a start edge.  T_{IN} input waveform
4	C_{OSC}	Cosc terminal • It generates a saw wave by connecting capacitor between 4-pin and GND. • Recommended capacitor value is 1000 pF.
5	C_{AGC}	C_{AGC} terminal • It sets up sensitivity of AGC by connecting capacitor between 5-pin and GND. • Recommended capacitor value is 1 μF. 

Terminal No.	Symbol	Function and Terminal Circumscription Circuitry
6	P.OUT	The abnormal state detection output terminal • The output becomes "H" from "L" when an abnormality is detected in the OVP or UVP terminal. Then the PWM output terminal becomes "H" settlement, too. • Do OFF of power supply (V_{CC}) to remove latch of abnormal state. • In abnormal state detection; Output "H" level = 10.5 V typ (The output load current: no-load, V_{CC} = 12 V) Output "L" level = 1.5 V typ (The output load current: –1 mA, V_{CC} = 12 V) • In normal state ; Output "L" level = 0.4 V typ (The output load current: +10 mA, V_{CC} = 12 V) 
7 8	OVP UVP	Over voltage protection of the control line (OVP) • Setting terminal voltage; GND ≤ V_{OVP} < V_{REF} Under voltage protection of the control line (UVP) • Setting terminal voltage; GND ≤ V_{UVP} < V_{OVP}  Note: It is connected to GND when the abnormal detection terminal is not used.
9 10	BI BO	The input terminal of a buffer Amp. (BI) The output terminal of a buffer Amp. (BO) 

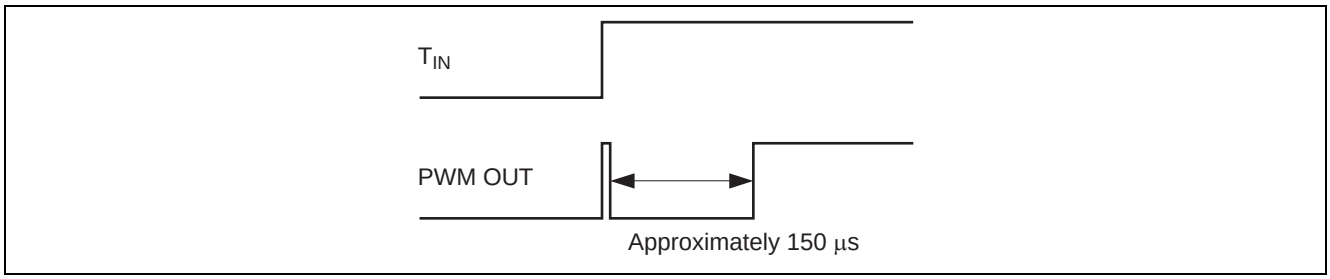
Terminal No.	Symbol	Function and Terminal Circumscription Circuitry
11 12	IN+ IN–	Positive input terminal of an Op-Amp. (IN+) Negative input terminal of an Op-Amp. (IN–) 
13 14	FB DTC	Output terminal of an Op-Amp. (FB) Dead time control terminal (DTC) • It can do soft start during power-on under keeping time constant. 
15	V_{REF}	Reference voltage terminal • 5 V output voltage (The terminal can begin to take outside connected load 5 mA.) 
16	GND	Ground terminal

Timing Chart

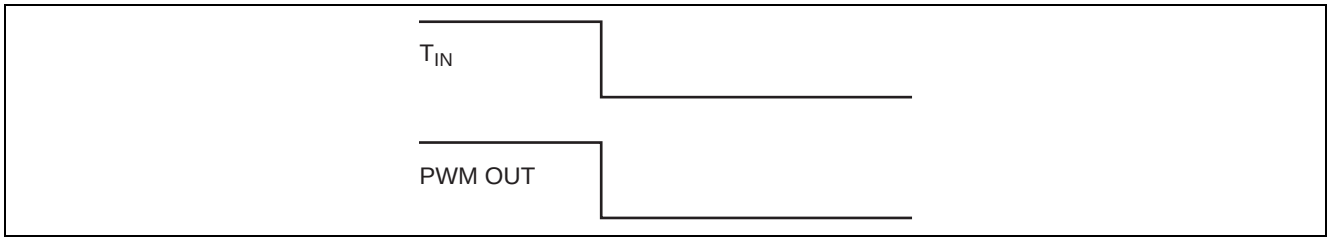
PWM OUT ON Duty is fixed in the voltage of higher one between DTC terminal and FB terminal voltage.



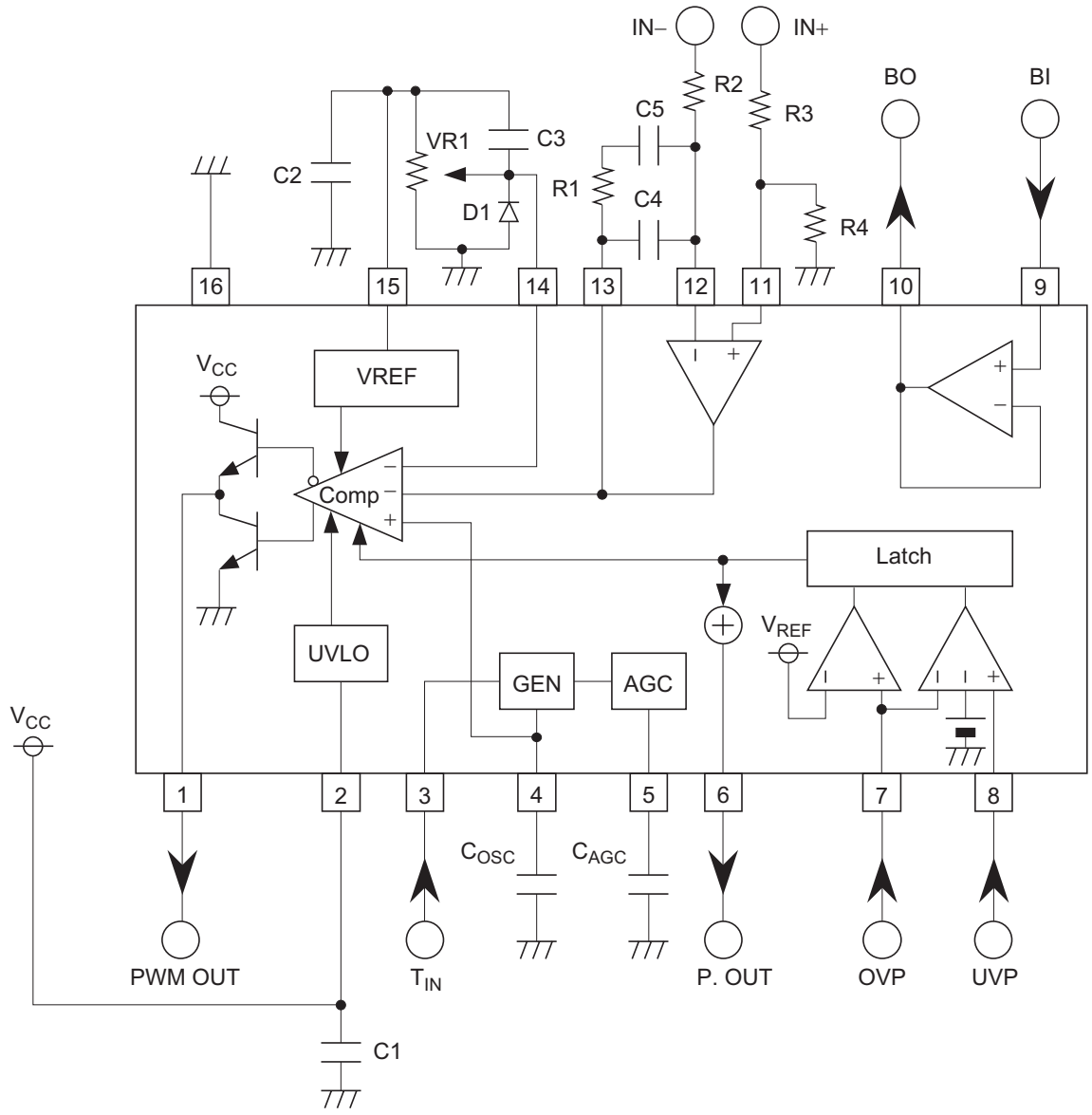
- Waveform at "H" was taken from "L", and having put T_{IN} up.
  (PWM output is fixed in "H", too when fix T_{IN} terminal in "H")



- Waveform at "L" was taken from "H", and having put T_{IN} up.
  (PWM output is fixed in "L", too when fix T_{IN} terminal in "L")



M62501 Application



C1, C2: Stabilization capacitors of V_{CC} and V_{REF}.

VR1: It is decided considering a load capacity of V_{REF}.
(A load capacity is approximately 5 mA.)
Recommended value is around 10 kΩ.

C3, DI: They are for the soft start function. A time constant is decided considering VR1.

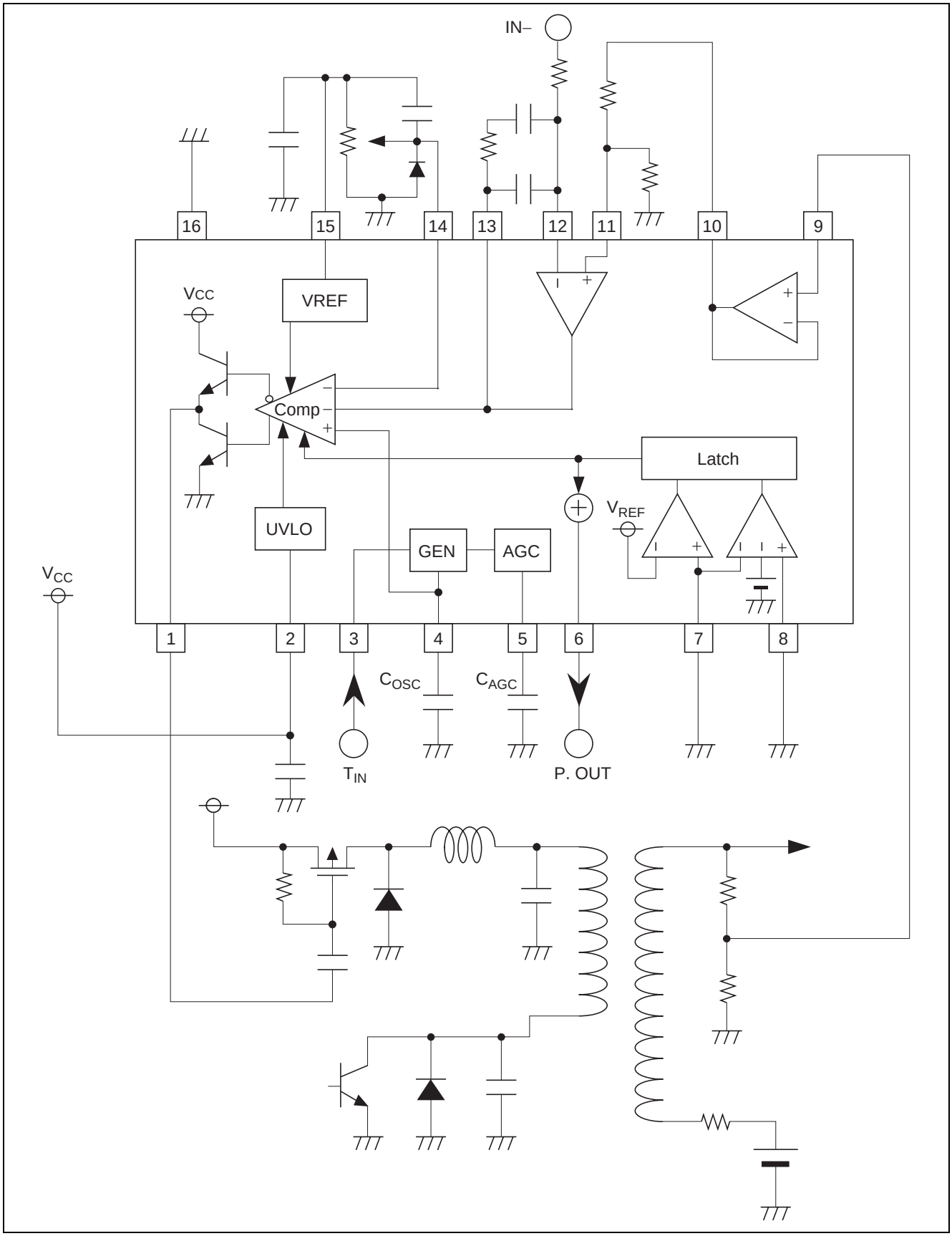
C_{AGC}: This capacitor is for stabilization of AGC. A larger capacitor improves a stability of the system, however a system response is degraded.
Recommended value is around 1 μF.

C_{OSC}: This capacitor is for a saw wave generation. Recommended value is around 1000 pF.

R1, R2, R3, R4, C4, C5:
They are for a gain setting of the error Amp. R2 should be several kΩ to dozens of kΩ to set a voltage gain 20 dB to 40 dB at f = 1 kHz, so that the feed back loop is stable.
When the voltage gain is too low, it causes jitter.
Recommended values of C4, C5 and R1 are ;
C4 = dozens of pF to several hundreds pF
C5 = several thousands pF to tens of thousands pF
R1 = dozens of kΩ to several hundreds kΩ.

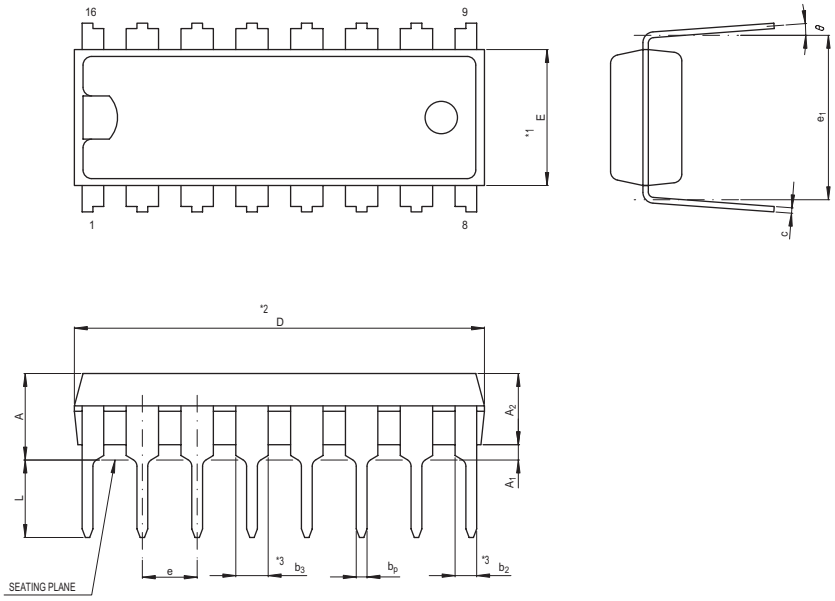
Note: Connect 7-pin and 8-pin terminal to GND when don't use under voltage protection. (UVP)

Example of Application Circuit



Package Dimensions

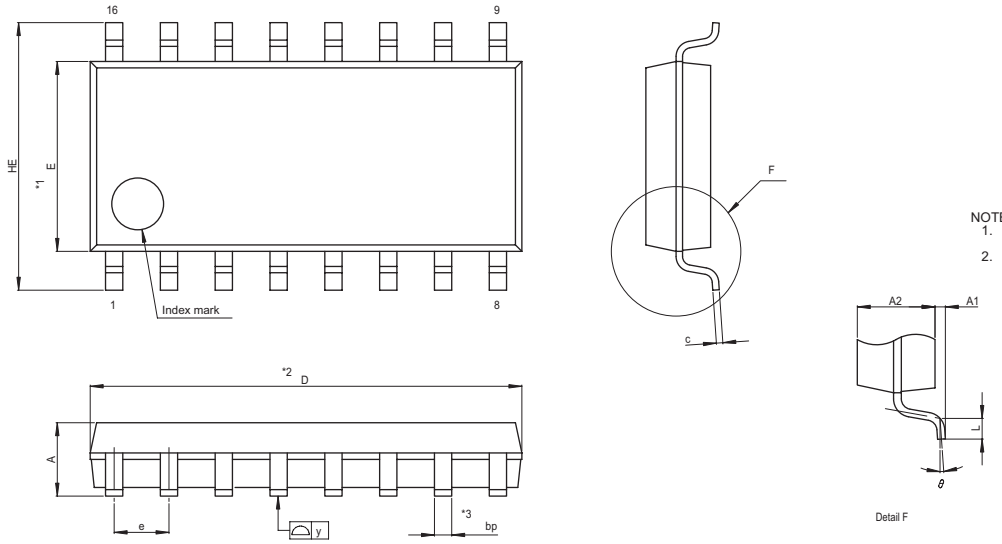
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19-2.54	PRDP0016AA-A	16P4	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-4.4x10-1.27	PRSP0016DA-A	16P2S-A	0.15g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.8	10.0	10.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A_1	0.05	—	—
A	—	—	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	1.07	1.27	1.47
y	—	—	0.1
L	0.2	0.4	0.6

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