19-2390; Rev 0; 4/02

MAXIM

Lowest Jitter Quad PECL-to-ECL Differential Translators

General Description

The MAX9424–MAX9427 high-speed, low-skew quad PECL-to-ECL translators are designed for high-speed data and clock driver applications. These devices feature an ultra-low 0.24ps(RMS) random jitter and channel-to-channel skew is less than 90ps in asynchronous mode.

The four channels can be operated synchronously with an external clock, or in asynchronous mode determined by the state of the SEL input. An enable input provides the ability to force all the outputs to a differential low state.

The parts differ from one another by their input and output termination options. The input options are an open input or an internal differential 100Ω termination. The output options are an open-emitter output or a series 50Ω termination. See *Ordering Information*.

The MAX9424–MAX9427 operate from a positive voltage supply of +2.375V to +5.5V, and a negative supply voltage of -2.375V to -5.5V and operate across the extended temperature range of -40°C to +85°C. They are offered in 32-pin 5mm x 5mm TQFP and space-saving 5mm x 5mm QFN packages.

Applications

Data and Clock Driver and Buffer

Central Office Backplane Clock Distribution

DSLAM Backplane

Base Station

ATE

Features

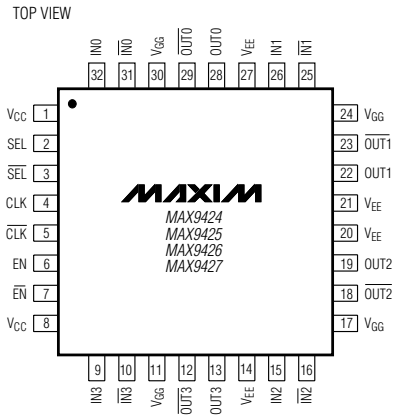
- **0.24ps RMS Added Random Jitter**
- **10ps Channel-to-Channel Skew in Synchronous Mode**
- **Guaranteed 500mV Differential Output at 3GHz Clock Frequency**
- **420ps Propagation Delay in Asynchronous Mode**
- **Functionally Compatible with**
  SK4426 (MAX9424)
  SK4430 (MAX9425)
  SK4436 (MAX9426)
  SK4440 (MAX9427)
- **Integrated 50Ω Outputs (MAX9425/MAX9427)**
- **Integrated 100Ω Inputs (MAX9426/MAX9427)**
- **Synchronous/Asynchronous Operation**

Ordering Information

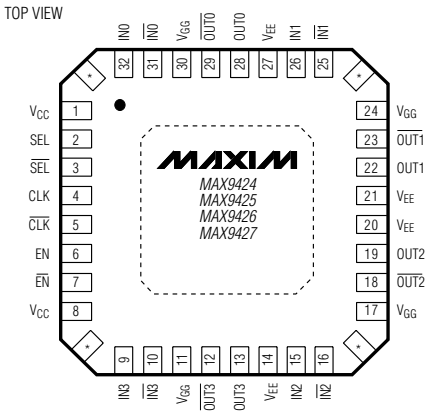
PART	TEMP RANGE	PIN-PACKAGE	INPUT (IN_, $\overline{IN\_}$)	OUTPUT (OUT_, $\overline{OUT\_}$)
MAX9424EHJ	-40°C to +85°C	32 TQFP	Open	Open
MAX9424EGJ*	-40°C to +85°C	32 QFN	Open	Open
MAX9425EHJ	-40°C to +85°C	32 TQFP	Open	50Ω
MAX9425EGJ*	-40°C to +85°C	32 QFN	Open	50Ω
MAX9426EHJ	-40°C to +85°C	32 TQFP	100Ω	Open
MAX9426EGJ*	-40°C to +85°C	32 QFN	100Ω	Open
MAX9427EHJ	-40°C to +85°C	32 TQFP	100Ω	50Ω
MAX9427EGJ*	-40°C to +85°C	32 QFN	100Ω	50Ω

**Future product—contact factory for availability.*

Pin Configurations



TQFP (5mm x 5mm)



QFN

NOTE: CORNER PINS ARE CONNECTED TO V_{GG}.

Lowest Jitter Quad PECL-to-ECL Differential Translators

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{GG} ..... -0.3V to +6.0V
V_{GG} to V_{EE} ..... -0.3V to +6.0V
Input Pins to V_{GG} ..... -0.3V to (V_{CC} + 0.3V)
Differential Input Voltage ..... $|V_{CC} - V_{GG}|$ or 3.0V, whichever is less
Continuous Output Current 50mA
Surge Output Current 100mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin 5mm x 5mm TQFP
(derate 9.5mW/°C above +70°C) 761mW
32-Pin 5mm x 5mm QFN
(derate 21.3mW/°C above +70°C) 1.7W
Junction-to-Ambient Thermal Resistance in Still Air
32-Pin 5mm x 5mm TQFP ..... +105°C/W
32-Pin 5mm x 5mm QFN ..... +47°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow
32-Pin 5mm x 5mm TQFP ..... +73°C/W
Junction-to-Case Thermal Resistance
32-Pin 5mm x 5mm TQFP ..... +25°C/W
32-Pin 5mm x 5mm QFN ..... +2°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
ESD Protection
Human Body Model (all input pins) ..... ±500V
Human Body Model (all output pins) ..... ±2kV
Soldering Temperature (10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{GG} = 2.375V to 5.5V, V_{GG} - V_{EE} = 2.375V to 5.5V, MAX9424/MAX9426 outputs terminated with 50Ω to V_{GG} - 2.0V, MAX9425/MAX9427 not externally terminated, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{GG} = 3.3V, V_{GG} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUTS (IN_, $\overline{IN\_}$, CLK, $\overline{CLK}$, EN, $\overline{EN}$, SEL, $\overline{SEL}$)							
Differential Input High Voltage	V_{IHD}	Figure 1		V_{GG} + 1.4		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 1		V_{GG}		V_{CC} - 0.2	V
Differential Input Voltage	V_{ID}	Figure 1	V_{CC} - V_{GG} < 3.0V	0.2		V_{CC} - V_{GG}	V
			V_{CC} - V_{GG} ≥ 3.0V	0.2		3.0	
Input Current	I_{IH}, I_{IL}	MAX9424/ MAX9425	EN, $\overline{EN}$, SEL, $\overline{SEL}$, IN_, $\overline{IN\_}$, CLK or $\overline{CLK}$ = V_{IHD} or V_{ILD}	-10		25	µA
		MAX9426/ MAX9427	EN, $\overline{EN}$, SEL, $\overline{SEL}$, CLK, or $\overline{CLK}$ = V_{IHD} or V_{ILD}	-10		25	
Differential Input Resistance (IN_, $\overline{IN\_}$)	R_{IN}	MAX9426/MAX9427		86	100	114	Ω
OUTPUTS (OUT_, $\overline{OUT\_}$)							
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1		600	635		mV
Output Common-Mode Voltage	V_{OCM}	Figure 1		V_{GG} - 1.50	V_{GG} - 1.25	V_{GG} - 1.05	V
Output Impedance	R_{OUT}	MAX9425/MAX9427		40	50	60	Ω
Internal Current Source	I_{SINK}	MAX9425/MAX9427		6	8	10	mA
POWER SUPPLY							
Positive Supply Current	I_{CC}	(Note 4)			16	27	mA
Negative Supply Current	I_{EE}	MAX9424/MAX9426 (Note 4)			100	130	mA
		MAX9425/MAX9427 (Note 4)			172	230	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{GG} = 2.375V to 5.5V, V_{GG} - V_{EE} = 2.375V to 5.5V, outputs terminated with 50Ω to V_{GG} - 2.0V, EN = V_{IHD}, $\overline{EN}$ = V_{ILD}, $f_{CLK} \le$ 3.0GHz, $f_{IN} \le$ 1.5GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{GG} + 1.4V to V_{CC}, V_{ILD} = V_{GG} to V_{CC} - 0.2V, V_{IHD} - V_{ILD} = 0.2V to smallest of $|V_{CC} - V_{GG}|$ or 3.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} - V_{GG} = 3.3V, V_{GG} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, T_A = +25°C, unless otherwise noted.) (Notes 1 and 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN_ to OUT_ Differential Propagation Delay	t_{PLH1} t_{PHL1}	Figure 3, SEL = high, asynchronous operation	300	420	570	ps
CLK to OUT_ Differential Propagation Delay	t_{PLH2} t_{PHL2}	Figure 4, SEL = low, synchronous operation	460	580	730	ps
OUT_ to OUT_ Skew	t_{SKD1}	SEL = high, asynchronous operation (Note 6)		38	90	ps
OUT_ to OUT_ Skew	t_{SKD2}	SEL = low, synchronous operation (Note 6)		10	70	ps
Maximum Clock Frequency	$f_{CLK(MAX)}$	MAX9424/MAX9426, V_{OH} - $V_{OL} \ge$ 500mV, SEL = low	3.0			GHz
		MAX9425/MAX9427, V_{OH} - $V_{OL} \ge$ 300mV, SEL = low				
Maximum Data Frequency	$f_{IN(MAX)}$	MAX9424/MAX9426, V_{OH} - $V_{OL} \ge$ 400mV, SEL = high	2.0			GHz
		MAX9425/MAX9427, V_{OH} - $V_{OL} \ge$ 250mV, SEL = high				
Added Random Jitter	t_{RJ}	SEL = low, f_{CLK} = 3.0GHz clock, f_{IN} = 1.5GHz (Note 7)		0.24	0.8	$ps_{(RMS)}$
		SEL = high, f_{IN} = 2.0GHz (Note 7)		0.3	0.8	
Added Deterministic Jitter	t_{DJ}	SEL = low, f_{CLK} = 3.0GHz, IN_ = 3.0Gbps 2^{23} - 1 PRBS pattern (Note 7)		27	80	$ps_{(P-P)}$
		SEL = high, IN_ = 2.0Gbps 2^{23} - 1 PRBS pattern (Note 7)		20	80	
IN_ to CLK Setup Time	t_S	Figure 4	80			ps
CLK to IN_ Hold Time	t_H	Figure 4	80			ps
Output Rise Time	t_R	Figure 3		89	120	ps
Output Fall Time	t_F	Figure 3		87	120	ps
Propagation Delay Temperature Coefficient	$\Delta t_{PD}/\Delta T$			0.2	1	ps/°C

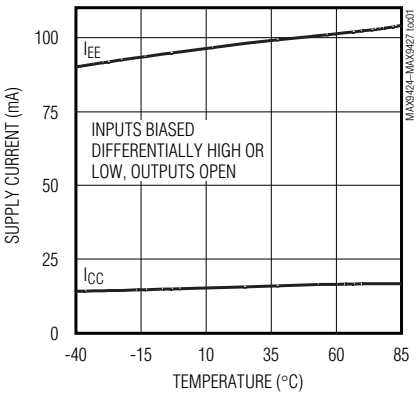
Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: All outputs open, all inputs biased differential high or low except V_{CC}, V_{GG}, and V_{EE}.
Note 5: Guaranteed by design and characterization, and are not production tested. Limits are set to ±6 sigma.
Note 6: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 7: Device jitter added to the input signal.

Lowest Jitter Quad PECL-to-ECL Differential Translators

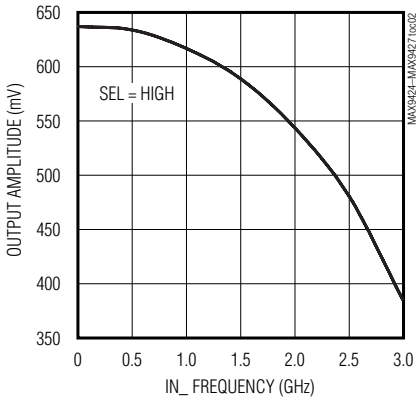
Typical Operating Characteristics

(MAX9424: V_{CC} - V_{GG} = 3.3V, V_{GG} - V_{EE} = 3.3V, outputs terminated with 50Ω to V_{GG} - 2.0V, enabled, f_{CLK} = 3.0GHz, f_{IN} = 1.5GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, T_A = +25°C, unless otherwise noted.)

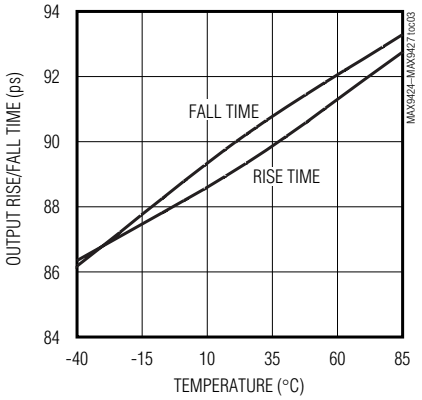
SUPPLY CURRENT vs. TEMPERATURE



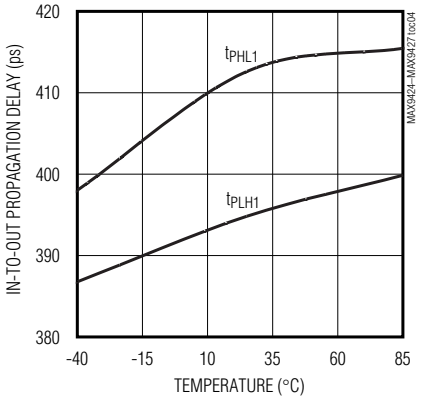
OUTPUT AMPLITUDE (V_{OH} - V_{OL}) vs. IN_ FREQUENCY



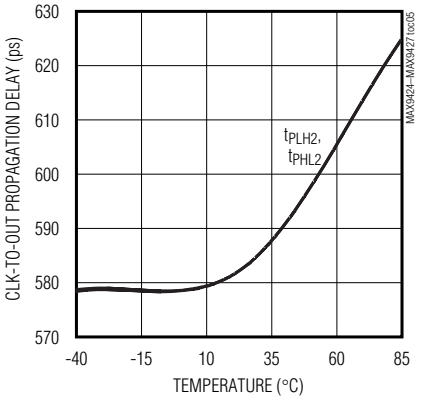
OUTPUT RISE/FALL TIME vs. TEMPERATURE



IN-TO-OUT PROPAGATION DELAY vs. TEMPERATURE



CLK-TO-OUT PROPAGATION DELAY vs. TEMPERATURE

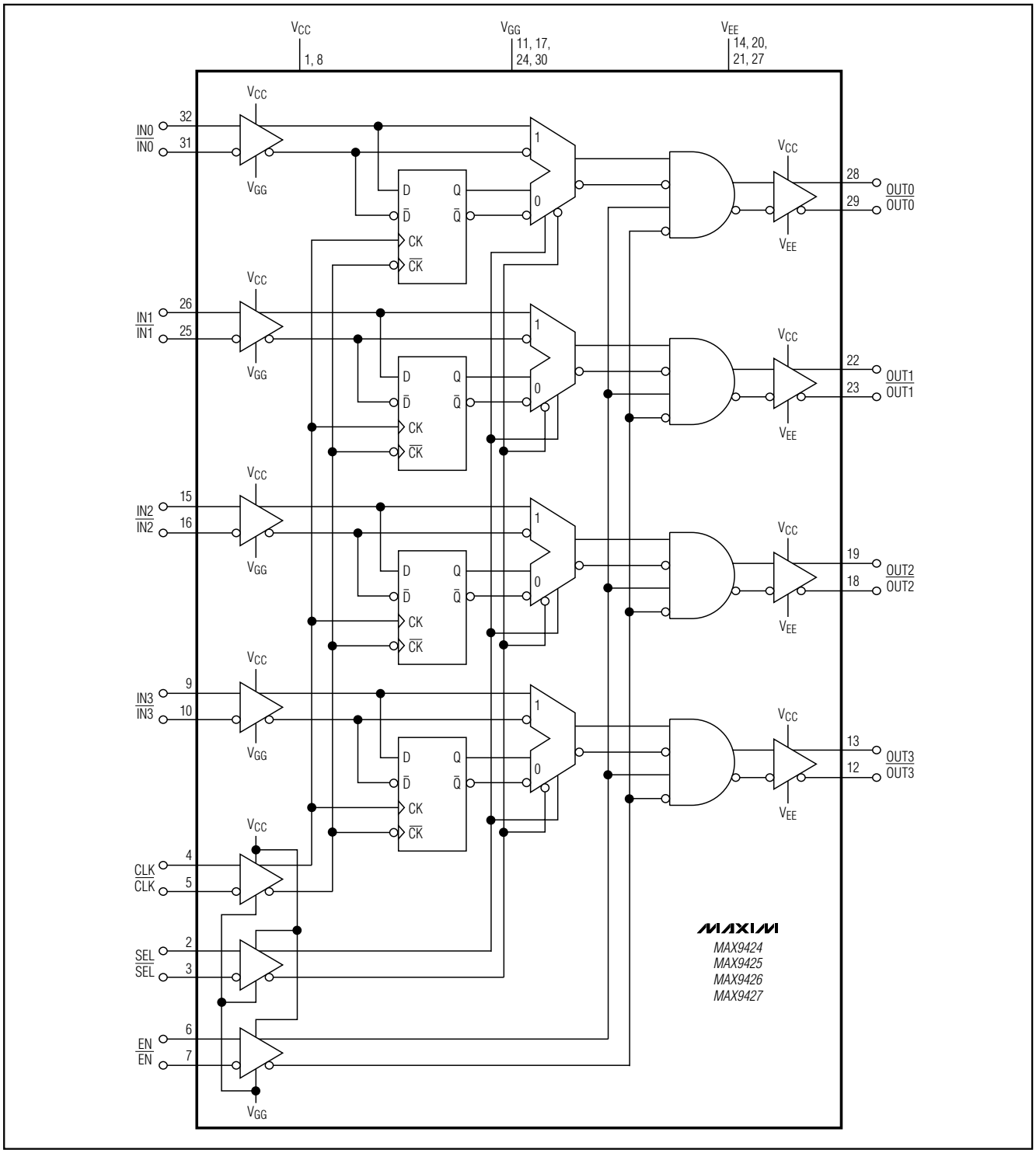


Pin Description

PIN	NAME	FUNCTION
1, 8	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to V_{GG} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	SEL	Noninverting Differential Select Input. Setting SEL = 1 and $\overline{SEL}$ = 0 enables all four channels to operate independently. Setting SEL = 0 and $\overline{SEL}$ = 1 enables all four channels to be synchronized to CLK.
3	$\overline{SEL}$	Inverting Differential Select Input
4	CLK	Noninverting Differential Clock Input
5	$\overline{CLK}$	Inverting Differential Clock Input
6	EN	Noninverting Differential Output Enable Input. Setting EN = 1 and $\overline{EN}$ = 0 enables all four outputs. Setting EN = 0 and $\overline{EN}$ = 1 disables all four outputs.
7	$\overline{EN}$	Inverting Differential Output Enable Input
9	IN3	Noninverting Differential Input 3
10	$\overline{IN3}$	Inverting Differential Input 3
11, 17, 24, 30	V_{GG}	Ground Reference
12	$\overline{OUT3}$	Inverting Differential Output 3
13	OUT3	Noninverting Differential Output 3
14, 20, 21, 27	V_{EE}	Negative Supply Voltage. Bypass from V_{EE} to V_{GG} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
15	IN2	Noninverting Differential Input 2
16	$\overline{IN2}$	Inverting Differential Input 2
18	$\overline{OUT2}$	Inverting Differential Output 2
19	OUT2	Noninverting Differential Output 2
22	OUT1	Noninverting Differential Output 1
23	$\overline{OUT1}$	Inverting Differential Output 1
25	$\overline{IN1}$	Inverting Differential Input 1
26	IN1	Noninverting Differential Input 1
28	OUT0	Noninverting Differential Output 0
29	$\overline{OUT0}$	Inverting Differential Output 0
31	$\overline{IN0}$	Inverting Differential Input 0
32	IN0	Noninverting Differential Input 0

Lowest Jitter Quad PECL-to-ECL Differential Translators

Functional Diagram



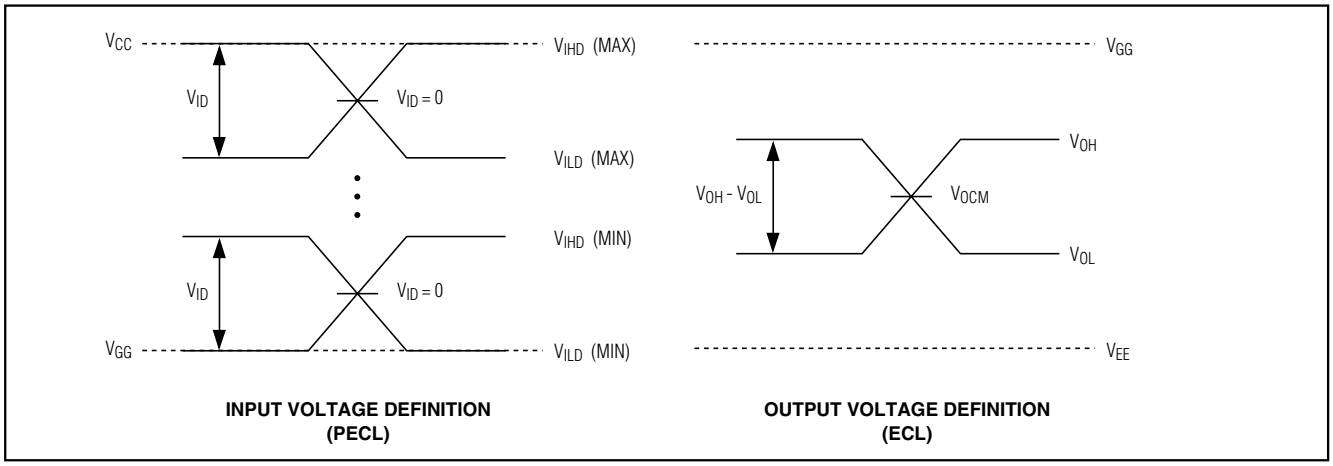


Figure 1. Input and Output Voltage Definitions

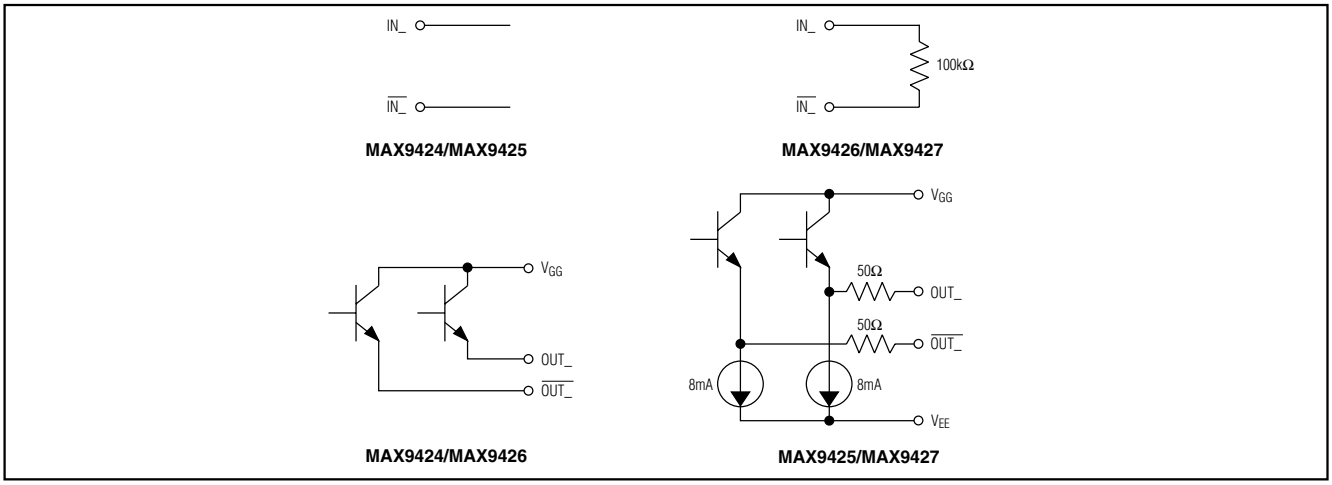


Figure 2. Input and Output Configurations

Detailed Description

The MAX9424–MAX9427 high-speed, low-skew PECL-to-ECL differential translators are designed for high-speed data and clock driver applications. These devices translate up to four PECL signals to ECL signals.

The four channels can be operated synchronously with an external clock, or in asynchronous mode, determined by the state of the SEL input. An enable input provides the ability to force all the outputs to a differential low state.

A variety of input and output terminations are offered for maximum design flexibility. The MAX9424 has open inputs and open-emitter outputs. The MAX9425 has open inputs and 50Ω series outputs. The MAX9426 has 100Ω differential input impedance and open-emitter outputs. The MAX9427 has 100Ω differential input impedance and 50Ω series outputs.

Supply Voltages

These devices require a positive voltage supply (connect to V_{CC}), a negative voltage supply (connect to V_{EE}), and a ground reference (connect to V_{GG}). V_{CC} is independent of V_{EE} and therefore the supply voltages do not need to be symmetrical. The PECL input voltages are referenced to V_{CC}, and the ECL output voltages are referenced to V_{GG}.

Data Inputs and Outputs

The input and output structures are shown in Figure 2. The open inputs of the MAX9424/MAX9425 require external termination, whereas the MAX9426/MAX9427 have integrated 100Ω differential input termination resistors between IN_ and $\overline{IN\_}$.

Lowest Jitter Quad PECL-to-ECL Differential Translators

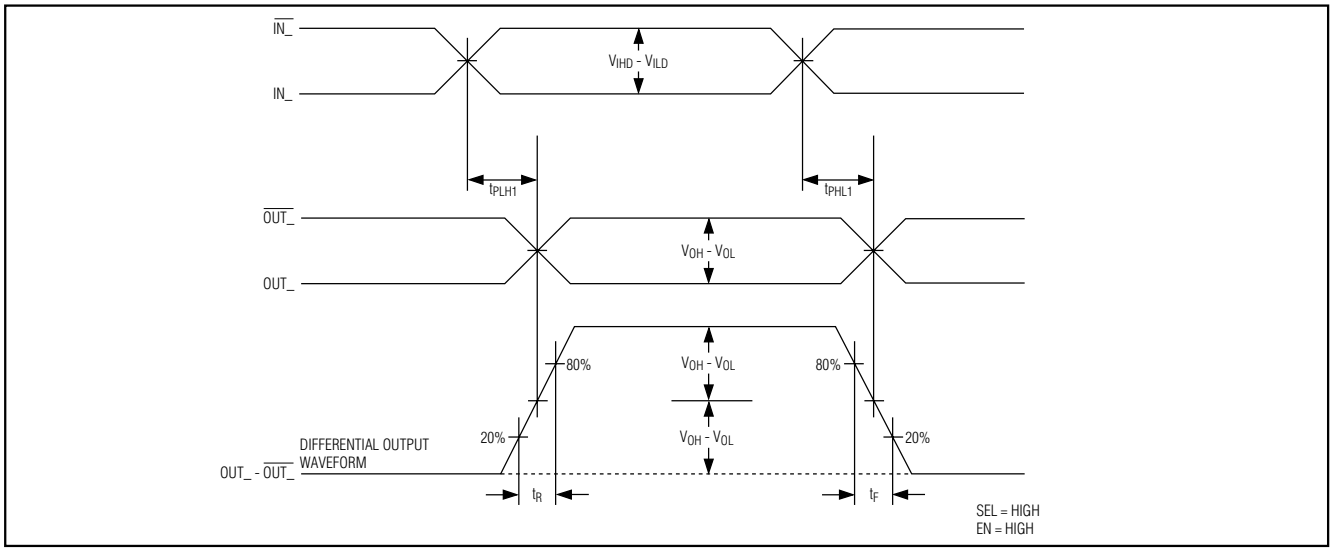


Figure 3. IN to OUT Propagation Delay and Transition Timing Diagram

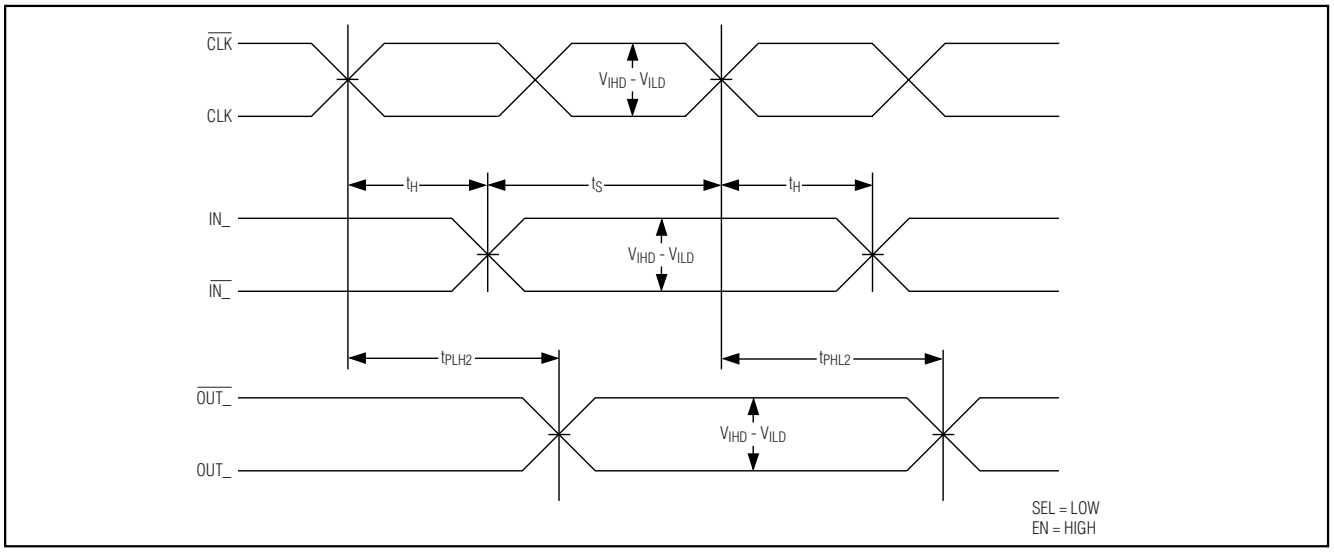


Figure 4. CLK to OUT Propagation Delay Timing Diagram

The MAX9425/MAX9427 have internal 50Ω series-output termination resistors and 8mA internal pulldown current sources, removing the need for external termination. The MAX9424/MAX9426 have open-emitter outputs, which require external termination (see the *Output Termination* section).

Enable

Setting EN = high and $\overline{EN}$ = low enables the device. Alternatively, setting EN = low and $\overline{EN}$ = high forces the outputs to a differential low; all changes on CLK, SEL, and IN_ are ignored.

Asynchronous Operation

Setting SEL = high and $\overline{SEL}$ = low enables the four channels to operate independently. The clock signal is ignored in this mode. When asynchronous mode is selected, drive or bias the CLK and $\overline{CLK}$ inputs. Biasing the clock inputs properly is shown in Figure 5. This prevents the unused clock inputs from toggling, which eliminates unnecessary switching noise.

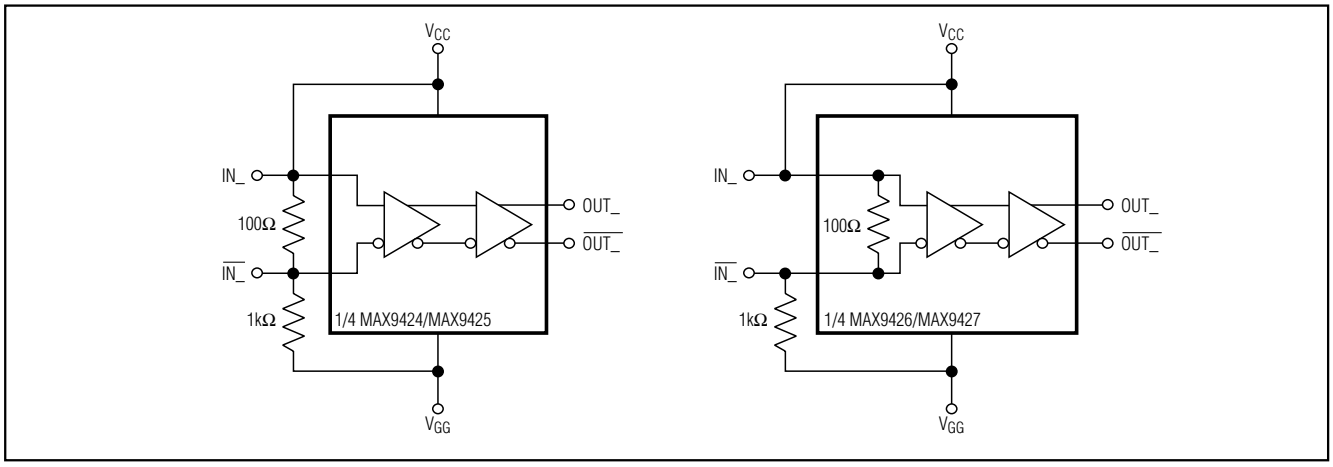


Figure 5. Input Bias Circuits for Unused Inputs

Synchronous Operation

Setting SEL = low and $\overline{SEL}$ = high enables all four channels to operate in synchronous mode where the buffered inputs are clocked out simultaneously on the rising edge of the differential clock input (CLK and $\overline{CLK}$). To have the input signals clocked out on the falling edge, swap the clock lines.

Differential Signal Input

The maximum input signal magnitude for each of the devices is V_{CC} - V_{GG} or 3.0V, whichever is less. This includes IN_, $\overline{IN\_}$, CLK, $\overline{CLK}$, SEL, $\overline{SEL}$, EN and $\overline{EN}$.

Applications Information

Input Bias

Bias any unused inputs as shown in Figure 5. This avoids noise coupling that can cause toggling of the unused outputs.

Output Termination

Terminate the open-emitter outputs (MAX9424/MAX9426) through 50Ω to V_{GG} - 2V or use equivalent Thevenin terminations. Terminate both outputs of a differential pair and use identical termination on each for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if OUT0 is used as a single-ended output, terminate both OUT0 and $\overline{OUT0}$.

Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

Power-Supply Bypassing

Typically, V_{GG} is directly connected to ground. Bypass each V_{CC} pin to V_{GG} with high-frequency surface-mount ceramic 0.01µF capacitors. Place these capacitors as close to the device as possible. Use the same bypass capacitor configuration between each V_{EE} pin and V_{GG}. In high-frequency, high-noise environments, add a 0.1µF capacitor in parallel with each 0.01µF capacitor.

Use multiple vias when connecting the bypass capacitors to V_{GG} (ground). This reduces trace inductance, lowering power-supply bounce when drawing high transient currents.

Circuit Board Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners, and using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Chip Information

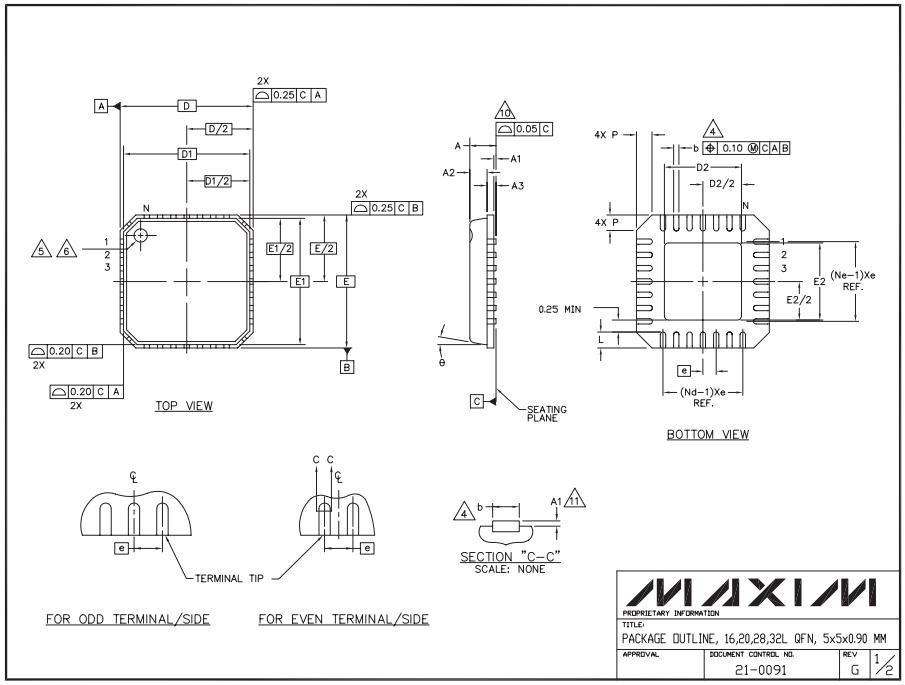
TRANSISTOR COUNT: 882

PROCESS: Bipolar

Lowest Jitter Quad PECL-to-ECL Differential Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE
e	0.80 BSC			
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

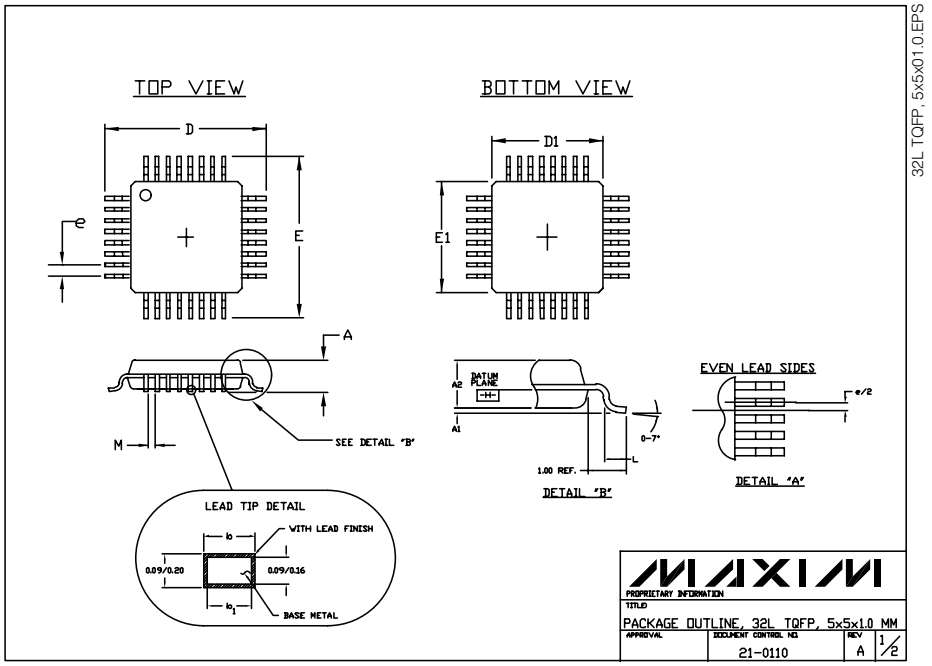
SYMBOL	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE
e	0.65 BSC			
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C MIN.	NOM.	MAX.	NOTE
e	0.50 BSC			
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D MIN.	NOM.	MAX.	NOTE
e	0.50 BSC			
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS	
	DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~~	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	~~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

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