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The S-29453A Series is high speed, low power 8K-bit serial E²PROM with a wide operating voltage range. It is organized as 512-word×16-bit. It is capable of sequential read, where addresses are automatically incremented in 16-bit blocks. The instruction code is compatible with the M6M800X1 Series.

■ Features

- Low power consumption
 - Standby : 1 μ A Max.
 - Operating : 1.2 mA Max. (V_{CC} =5.5 V)
 - 0.4 mA Max. (V_{CC} =2.5 V)
- Wide operating voltage range
 - Write : 2.5 to 5.5 V
 - Read : 1.8 to 5.5 V
- Sequential read capable
- Endurance : 10^5 cycles/word
- Data retention : 10 years

■ Pin Assignment

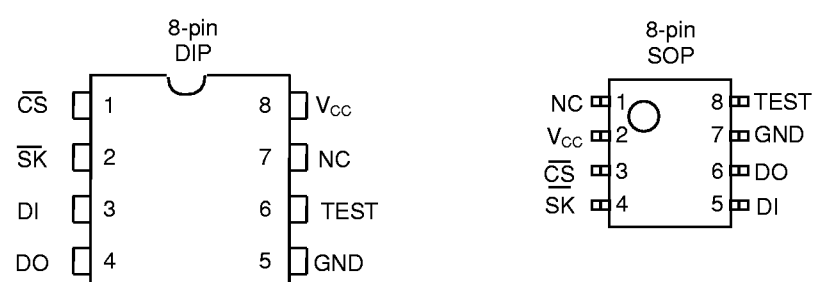


Figure 1

$\overline{CS}$	Chip select input
$\overline{SK}$	Serial clock input
DI	Serial data input
DO	Serial data output
GND	Ground (0 V)
V_{CC}	Power supply
TEST	Test pin (normally kept open) (can be connected to GND or V_{CC})

■ Block Diagram

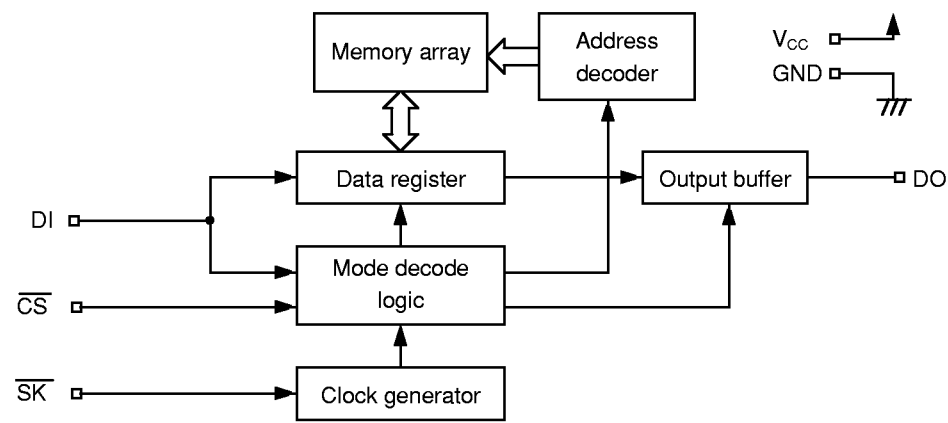


Figure 2

■ Instruction Set

Table 1

Instruction	Operation block	Address	Data
READ (Read data)	1010100A ₈	A ₇ to A ₀	D ₁₅ to D ₀ output*
PROGRAM (Write data)	1010010A ₈	A ₇ to A ₀	D ₁₅ to D ₀
EWEN (Program enable)	10100011	xxxxxxx	—
EWDS (Program disable)	10100000	xxxxxxx	—

x : Doesn't matter.

* : When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC}	V
Storage temperature under bias	T _{bias}	-50 to +95	°C
Storage temperature	T _{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V _{CC}	Read Operation	1.8	—	5.5	V
		Write Operation	2.5	—	5.5	V
High level input voltage	V _{IH}	V _{CC} =2.5 to 5.5V	0.8×V _{CC}	—	V _{CC}	V
		V _{CC} =1.8 to 2.5V	0.8×V _{CC}	—	V _{CC}	V
Low level input voltage	V _{IL}	V _{CC} =2.5 to 5.5V	0.0	—	0.2×V _{CC}	V
		V _{CC} =1.8 to 2.5V	0.0	—	0.15×V _{CC}	V
Operating temperature	T _{opr}		-40	—	+85	°C

■ DC Electrical Characteristics

Table 4

Parameter	Symbol	Conditions	V _{CC} =5.0 V±10 %			V _{CC} =2.5 to 3.3 V			V _{CC} =1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I _{CC1}	DO unloaded	—	—	1.2	—	—	0.5	—	—	0.4	mA
Current consumption (PROGRAM)	I _{CC2}	DO unloaded	—	—	5.0	—	—	2.0	—	—	—	mA

Parameter	Symbol	Conditions	V _{CC} =5.0 V±10 %			V _{CC} =2.5 to 4.5 V			V _{CC} =1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I _{SB}	Input: V _{CC} or GND	—	—	1.0	—	—	1.0	—	—	1.0	μA
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I _{LO}	V _{OUT} =GND to V _{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V _{OL}	CMOS I _{OL} =100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
		TTL I _{OL} =2.1 mA	—	—	0.45	—	—	—	—	—	—	V
High level output voltage	V _{OH}	CMOS V _{CC} =2.5 to 5.5 V : I _{OH} =-100 μA V _{CC} =1.8 to 2.5 V : I _{OH} =-10 μA	V _{CC} -0.7	—	—	V _{CC} -0.7	—	—	V _{CC} -0.3	—	—	V
		TTL, I _{OH} =-400 μA	2.4	—	—	—	—	—	—	—	—	V
Write enable latch data hold voltage	V _{DH}		1.5	—	—	1.5	—	—	1.5	—	—	V

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N _W	10 ⁵	—	—	cycles/word

■ Pin Capacitance

Table 7

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} =0 V	—	—	8	pF
Output Capacitance	C _{OUT}	V _{OUT} =0 V	—	—	10	pF

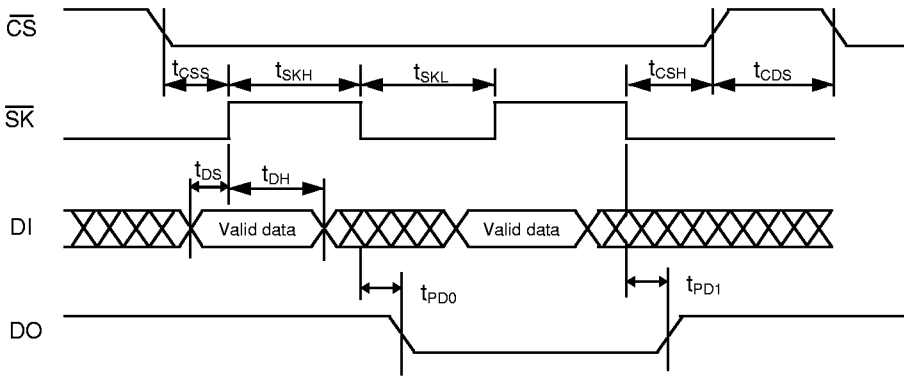
■ AC Electrical Characteristics

Table 8 Measuring conditions

Input pulse voltage	0.1×V _{CC} to 0.9×V _{CC}
Output reference voltage	0.5×V _{CC}
Output load	100pF

Table 9

Parameter	Symbol	Read/Write operations						Read operation			Unit
		V _{CC} =5.0 V±10 %			V _{CC} =2.5 to 4.5 V			V _{CC} =1.8 to 2.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{\text{CS}}$ setup time	t _{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{\text{CS}}$ hold time	t _{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{\text{CS}}$ setup time (CPU)	t _{CSS (CPU)}	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{\text{CS}}$ hold time (CPU)	t _{CSH (CPU)}	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{\text{CS}}$ deselect time	t _{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	μs
Data setup time	t _{DS}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Data hold time	t _{DH}	0.2	—	—	0.4	—	—	0.8	—	—	μs
1 data output delay time	t _{PD1}	—	—	0.4	—	—	0.8	--	—	2.0	μs
0 data output delay time	t _{PD0}	—	—	0.4	—	—	0.8	--	—	2.0	μs
Clock frequency	f _{SK}	0.0	—	2.0	0.0	—	0.5	0.0	—	0.2	MHz
Clock pulse width	t _{SKH} , t _{SKL}	0.25	—	—	1.0	—	—	2.5	—	—	μs
Output disable time	t _{HZ1} , t _{HZ2}	0	50	150	0	500	1000	—	—	—	ns
Output enable time	t _{SV}	0	50	150	0	500	1000	—	—	—	ns
Programming time	t _{PR}	—	4.0	10	—	4.0	10	—	—	—	ms



Input data is retrieved on the rising edge of $\overline{\text{SK}}$.
Output data is triggered on the falling edge of $\overline{\text{SK}}$.

Figure 3 Timing Chart

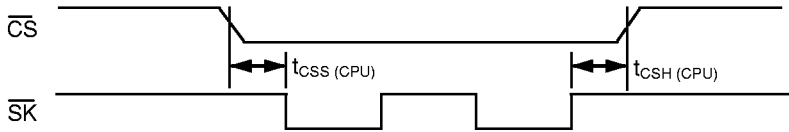


Figure 4 Timing Chart for t_{CS (CPU)} and t_{CSH (CPU)} when CPU is connected

■ Operation

Instructions (in the order of operation code, address, and data) are latched to DI in synchronization with the rising edge of $\overline{SK}$ after $\overline{CS}$ goes low. A start-bit can only be recognized when the high of DI is latched at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low, it is impossible for it to be recognized as long as DI is low, even if there are $\overline{SK}$ pulses after $\overline{CS}$ goes low. Instruction finishes when $\overline{CS}$ goes high, where it must be high between commands during t_{CDS} .

All input, including DI and $\overline{SK}$ signals, is ignored while $\overline{CS}$ is high. The operation code plus address is a multiple of 8-bits. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

1. READ

The READ instruction reads data from a specified address. The READ operation code and address are continuously latched in synchronization with the rising edge of $\overline{SK}$. The DO pin begins to output at the 16-th clock from a start-bit. Data is continuously output in synchronization with the falling edge of $\overline{SK}$.

When all of the data (D_{15} to D_0) in the specified address has been read, data in the next address can be read with the input of another $\overline{SK}$ clock. Thus, the data over whole area of the memory can be read by continuously inputting $\overline{SK}$ clocks as long as $\overline{CS}$ is low.

The last address ($A_n \dots A_1 A_0 = 1 \dots 11$) rolls over to the top address ($A_n \dots A_1 A_0 = 0 \dots 00$).

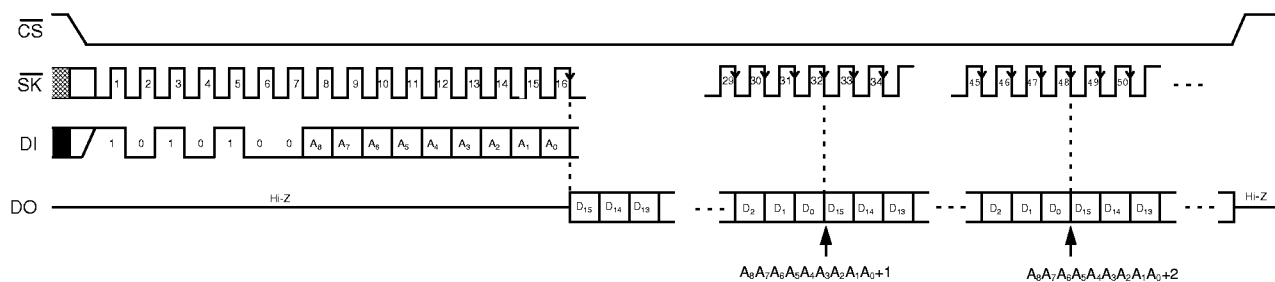


Figure 5 Read Timing

2. PROGRAM

The PROGRAM instruction writes 16-bit data to a specified address.

After changing $\overline{CS}$ to low, input PROGRAM operation code, address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing $\overline{CS}$ to high will start the PROGRAM operation. It is not necessary to make the data "1" before initiating the PROGRAM operation.

The write operation is completed in 10 ms (t_{PR} Max.), and the typical write period is less than 5 ms. In the S-29453A, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting $\overline{CS}$ to "L" and checking the DO pin after the write operation begins by setting $\overline{CS}$ to "H". VERIFY operations to detect changes in the DO output can be executed in succession. One is a change from "L" to "H" with $\overline{CS}$ ="L". The other is a change from "L" to "H" after setting $\overline{CS}$ to "L" and returning $\overline{CS}$ to "H" repeatedly.

Because all $\overline{SK}$ and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedance state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedance state upon the recognition of a high of DI attached to the rising edge of an $\overline{SK}$ pulse.

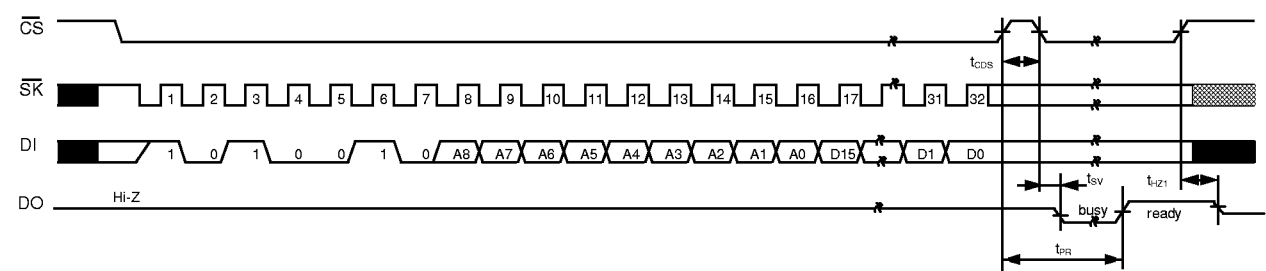


Figure 6 PROGRAM Timing

3. Write enable (EWEN) and Write disable (EWDS)

The EWEN instruction puts the S-29453A into write enable mode, which accepts PROGRAM instruction. The EWDS instruction puts the S-29453A into write disable mode, which refuses PROGRAM instruction.

The S-29453A powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

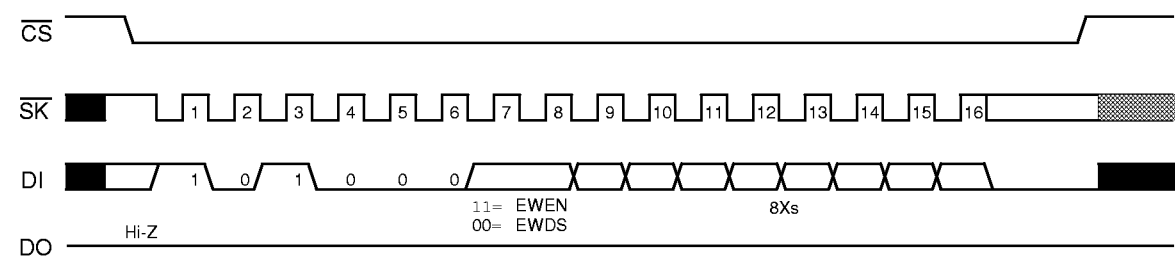


Figure 7 EWEN/EWDS Timing

■ Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low. The write operation begins by inputting the write instruction and setting $\overline{CS}$ to high. The DO pin then outputs low during the write operation and high at its completion by setting $\overline{CS}$ to low (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having $\overline{CS}$ go low, the DO pin is switched from a state of high-impedence to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedence (see Figure 8).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

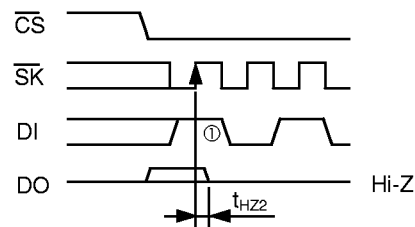


Figure 8 Start-Bit latching timing

■ Three-Wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to $\overline{CS}$, $\overline{SK}$, DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI (See Figure 9).

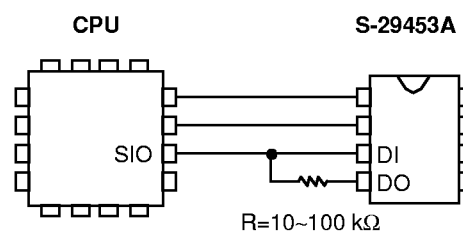


Figure 9 3-wire interface

■ Dimensions (Unit : mm)

1. 8-pin DIP

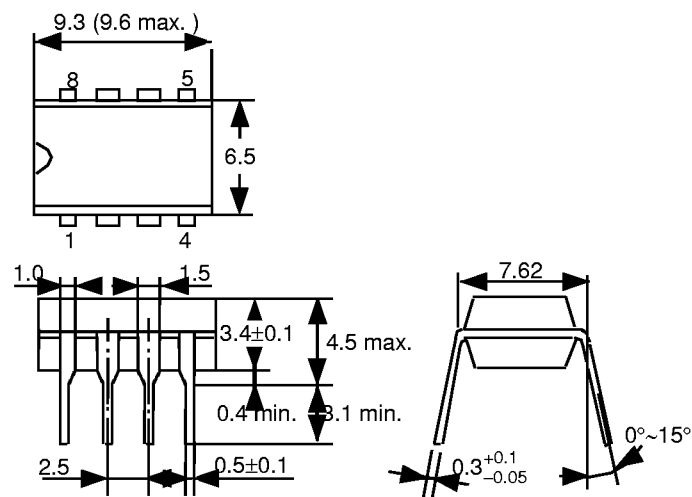


Figure 10

2. 8-pin SOP

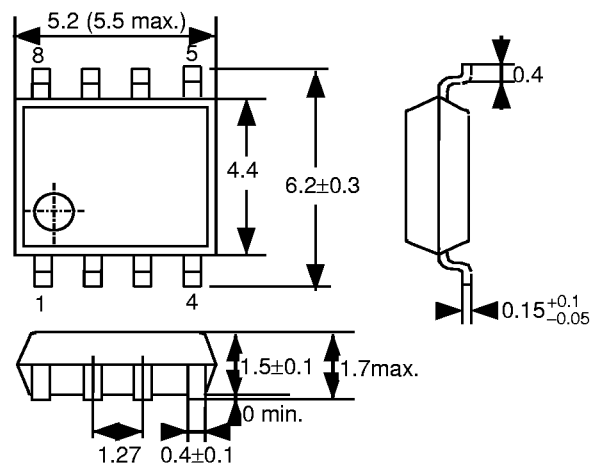


Figure 11

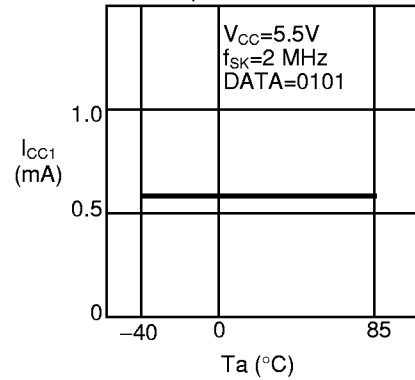
■ Ordering Information

S-29453A XX
 Package DP : DIP
 FE : SOP

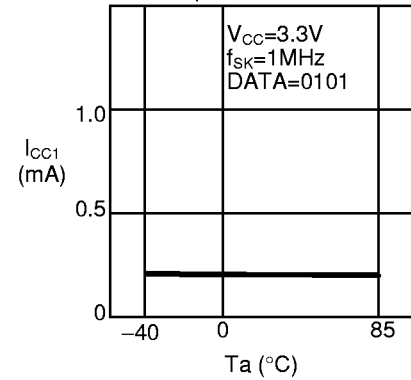
■ Characteristics

1. DC Characteristics

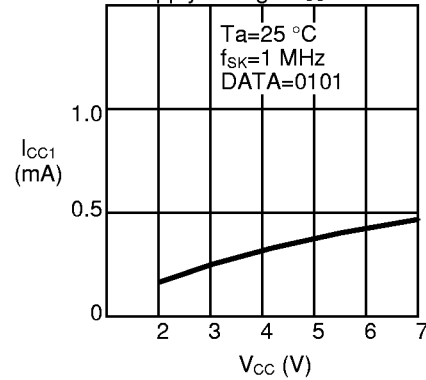
1.1 Current consumption (READ) I_{CC1} - Ambient temperature T_a



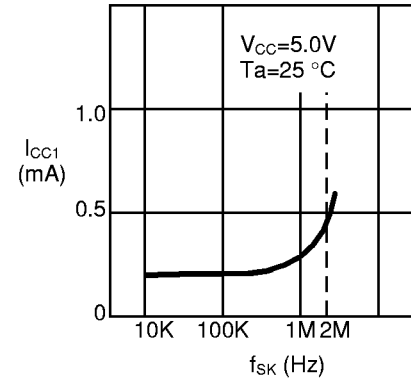
1.2 Current consumption (READ) I_{CC1} - Ambient temperature T_a



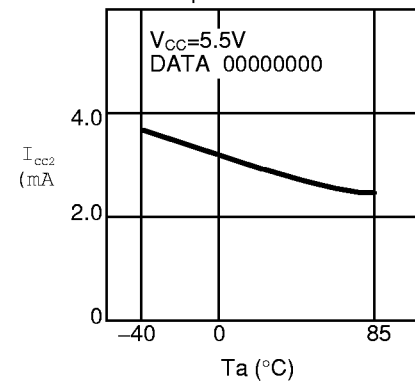
1.3 Current consumption (READ) I_{CC1} - Power supply voltage V_{CC}



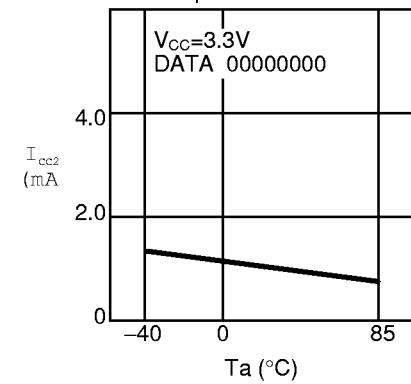
1.4 Current consumption (READ) I_{CC1} - Clock frequency f_{SK}



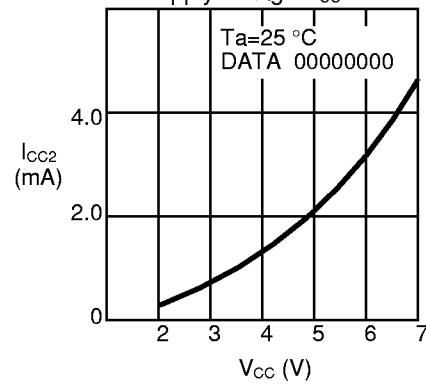
1.5 Current consumption (PROGRAM) I_{CC2} - Ambient temperature T_a



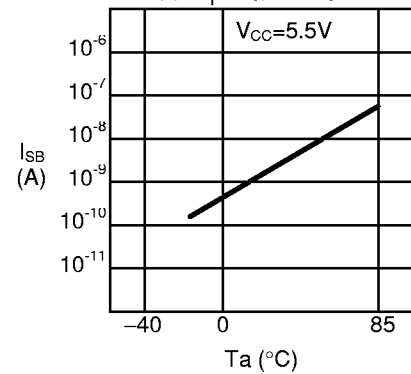
1.6 Current consumption (PROGRAM) I_{CC2} - Ambient temperature T_a

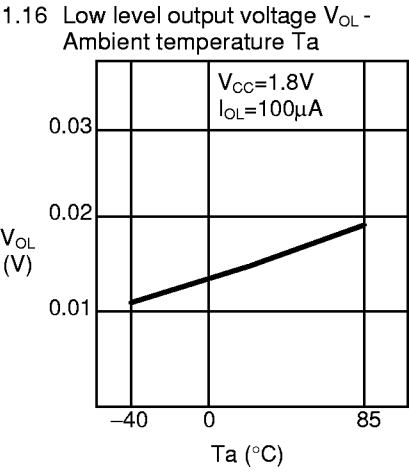
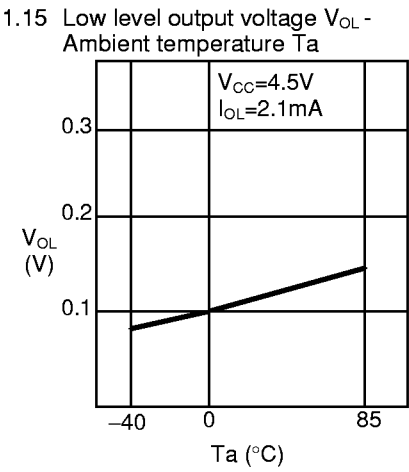
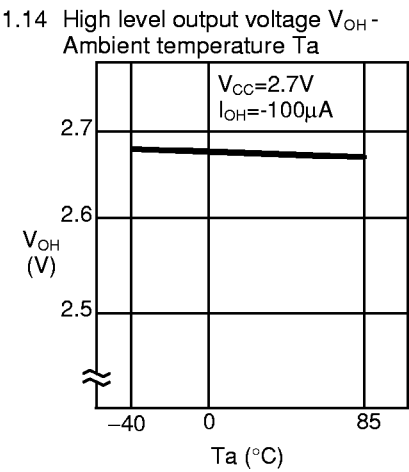
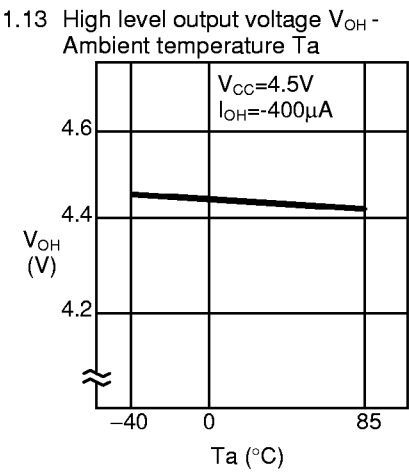
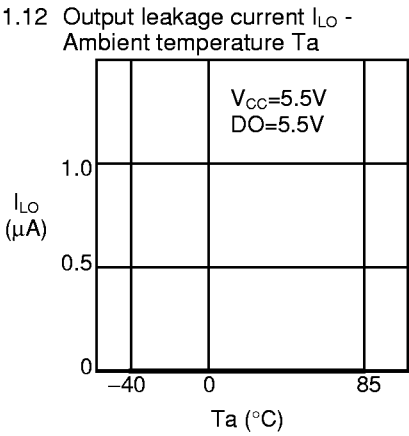
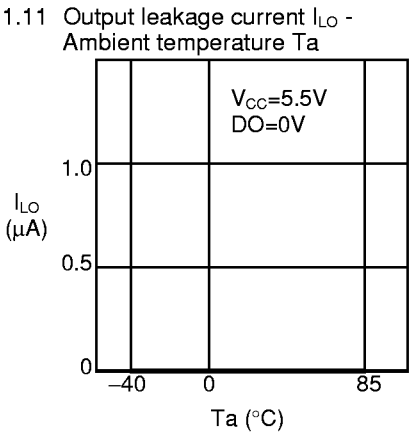
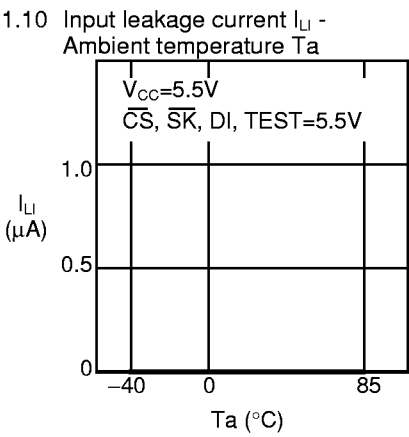
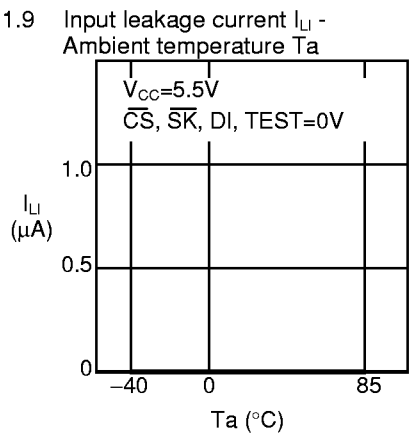


1.7 Current consumption (PROGRAM) I_{CC2} - Power supply voltage V_{CC}

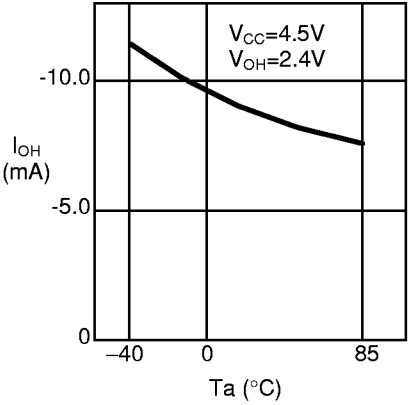


1.8 Standby current consumption I_{SB} - Ambient temperature T_a

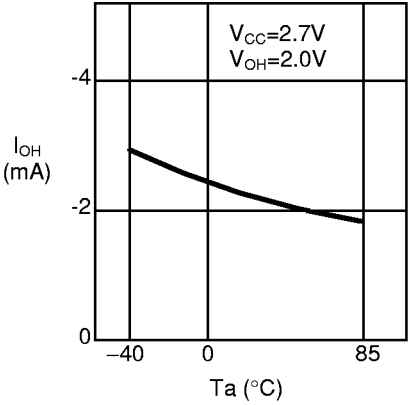




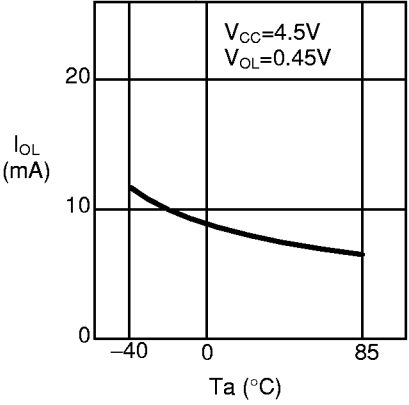
1.17 High level output current I_{OH} - Ambient temperature T_a



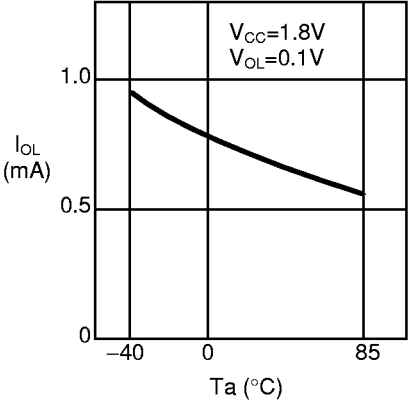
1.18 High level output current I_{OH} - Ambient temperature T_a



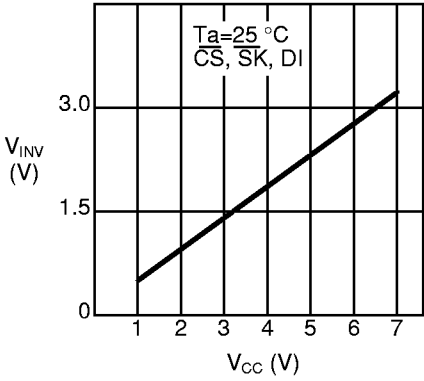
1.19 Low level output current I_{OL} - Ambient temperature T_a



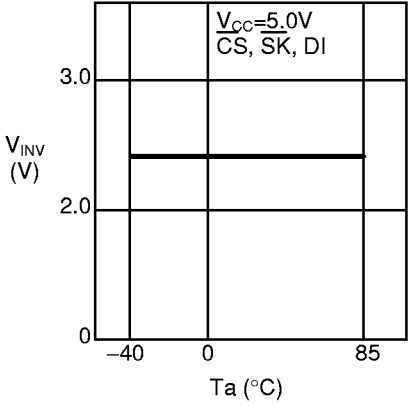
1.20 Low level output current I_{OL} - Ambient temperature T_a



1.21 Input inversion voltage V_{INV} - Power supply voltage V_{CC}

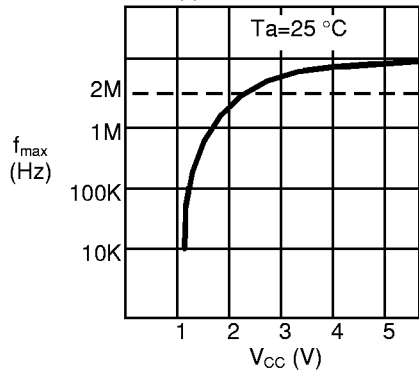


1.22 Input inversion voltage V_{INV} - Ambient temperature T_a

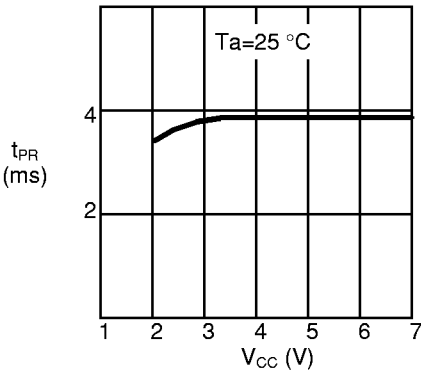


2. AC Characteristics

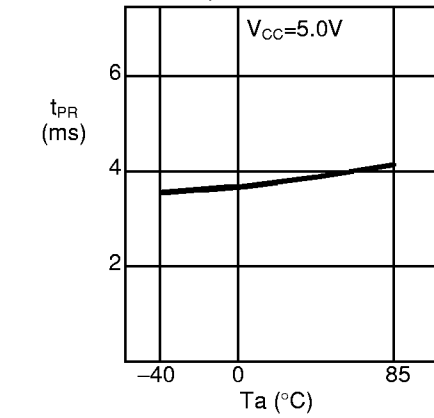
2.1 Maximum operating frequency f_{max} -
Power supply voltage V_{CC}



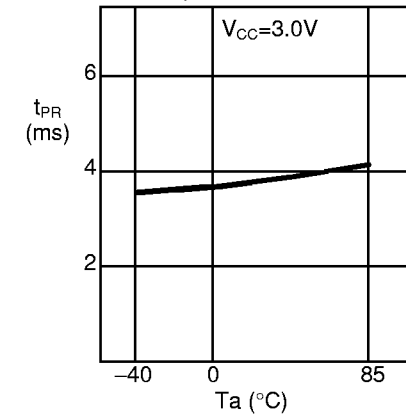
2.2 Program time t_{PR} -
Power supply voltage V_{CC}



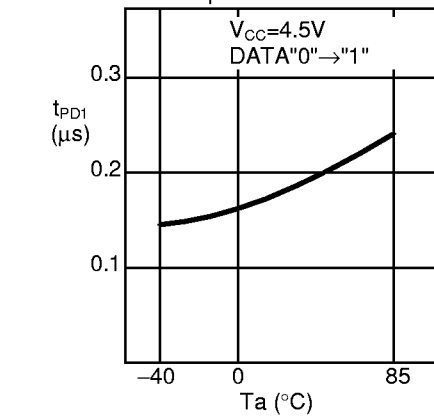
2.3 Program time t_{PR} -
Ambient temperature T_a



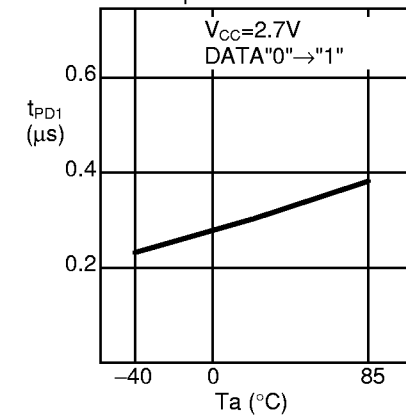
2.4 Program time t_{PR} -
Ambient temperature T_a



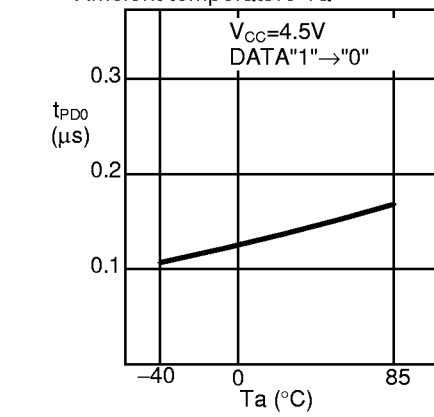
2.5 "1" Data output delay time t_{PD1} -
Ambient temperature T_a



2.6 "1" Data output delay time t_{PD1} -
Ambient temperature T_a



2.7 "0" Data output delay time t_{PD0} -
Ambient temperature T_a



2.8 "0" Data output delay time t_{PD0} -
Ambient temperature T_a

