

# T6L60

## Gate Driver for TFT LCD Panels

The T6L60 is a 150/154-channel output gate driver for TFT LCD panels. This device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. Thus, this device can be used for various TFT LCD panel drive systems.

### Features

- LCD drive output pins : Switchable between 150 and 154 pins
- LCD drive voltage : max VEE + 40 V
- Data transfer method : Bidirectional shift register
- Operating temperature: -20 to 75°C
- Package : Tape carrier package (TCP)

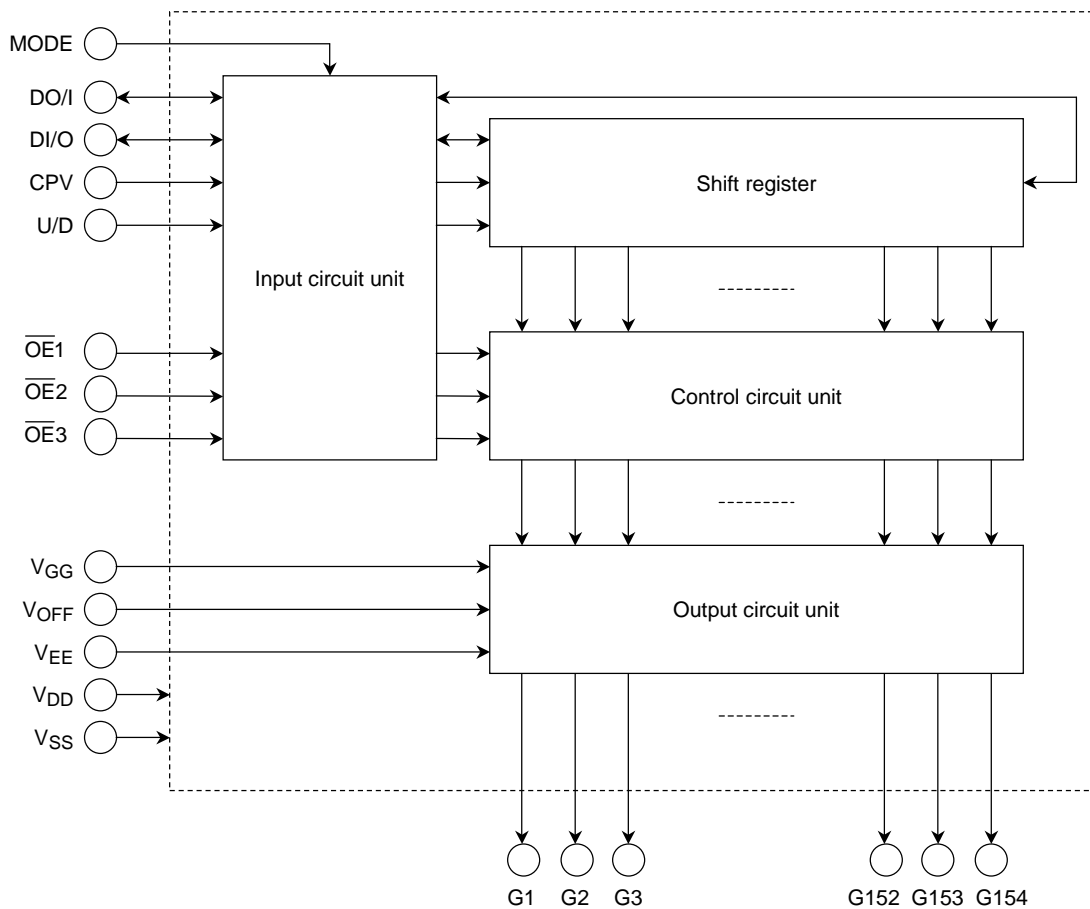
Unit: mm

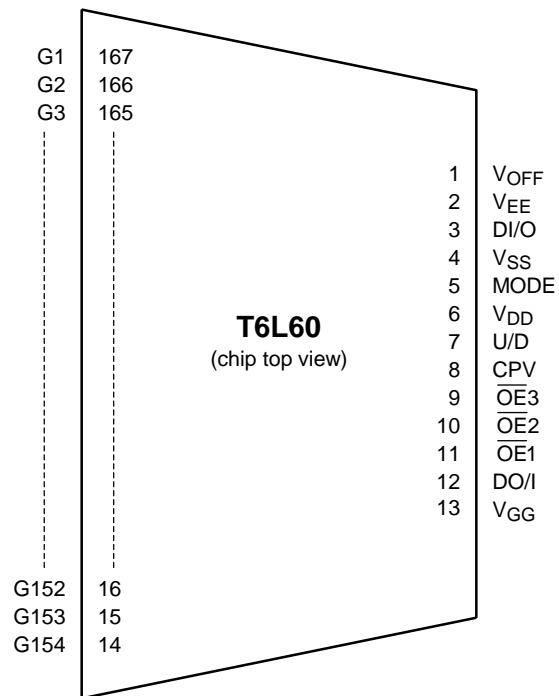
T6L60	User area pitch	
	IN	OUT
(SAN, 3NS)	0.80000	0.14979

Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

### Block Diagram



**Pin Assignment**

The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

## Pin Function

Pin Name	I/O	Function									
DI/O DO/I	I/O	<p>Vertical shift data I/O pins These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>U/D</th> <th>DI/O</th> <th>DO/I</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table> <p>When set for input This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.</p> <p>When set for output When two or more T6L60s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</p>	U/D	DI/O	DO/I	H	Input	Output	L	Output	Input
U/D	DI/O	DO/I									
H	Input	Output									
L	Output	Input									
U/D	I	<p>Transfer direction select pin This pin specifies the direction in which data is transferred through the shift registers. The shift register data is shifted synchronously with each rising edge of CPV as follows: When U/D is high, data is shifted in the direction G1 → G2 → G3 → G4 → ... → G154 When U/D is low, the direction is reversed to give G154 → G153 → G152 → G151 → ... → G1 The voltage applied to this pin must be a DC-level voltage that is either high (V<sub>DD</sub>) or low (V<sub>SS</sub> or V<sub>EE</sub>)</p>									
CPV	I	<p>Vertical shift clock This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</p>									
$\overline{OE}1$ to $\overline{OE}3$	I	<p>Output enable pins These signals control the data appearing at the LCD panel drive pins (G1 through G154). <math>\overline{OE}</math> doesn't synchronize with the CPU. The V<sub>OFF</sub> voltage is output when <math>\overline{OE}1</math> to <math>\overline{OE}3</math> are high; normal shift data is output when <math>\overline{OE}1</math> to <math>\overline{OE}3</math> are low.</p>									
MODE	I	<p>Output channels select pin This signal selects either 150-pin mode or 154-pin mode for the LCD panel driver. When MODE = high, 150-pin mode is selected, in which case G76 through G79 are not used. (V<sub>OFF</sub> level) When MODE = low, 154-pin mode is selected.</p>									
G1 to G154	O	<p>LCD panel drive pins These pins output the shift register data or the voltage applied to V<sub>GG</sub> or V<sub>OFF</sub> depending on the control signals <math>\overline{OE}1</math> to <math>\overline{OE}3</math>.</p>									
V <sub>GG</sub>	—	Power supply for LCD drive									
V <sub>OFF</sub>	—	Analog reference voltage These pins accept as their input the OFF level at the LCD panel drive pins (G1 through G154).									
V <sub>EE</sub>	—	Power supply for LCD drive									
V <sub>DD</sub>	—	Power supply for the internal logic									
V <sub>SS</sub>	—	Power supply for the internal logic									

## Device Operation

### (1) Shift data transfer method

Mode Pin	U/D Pin	Shift Data		Data Transfer Method
		Input	Output	
H (150-out)	H	DI/O	DO/I	G1 → G2 → G3 → ... → G75 → G80 → ... → G154
	L	DO/I	DI/O	G154 → G153 → G152 → ... → G80 → G75 → ... → G1
L (154-out)	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ... → G154
	L	DO/I	DI/O	G154 → G153 → G152 → G151 → ... → G1

The input data (DI/O or DO/I) is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

In the output operation, the data in the last shift register (G154 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the V<sub>DD</sub> level; the output low voltage is the V<sub>SS</sub> level.)

Note: The outputs of G76 to G79 are V<sub>OFF</sub> level in 150 output mode.

### (2) LCD panel drive outputs

The LCD panel drive outputs are controlled by  $\overline{OE1}$  to  $\overline{OE3}$  as shown below.

The following combinations of mode pins and output enable pins don't depend on the polarity of U/D pins; hence, LCD panel drive outputs for LCD panel drive pins controlled by  $\overline{OE}$  are the same when the U/D pins is High or Low.

Mode Pin	Output Enable Pin	LCD Panel Drive Outputs		Output
		LCD Panel Drive Pins Controller by		
H (150-out)	$\overline{OE1} = \text{"H"}$	G1, G4, G7, ...G73, G80 ... G149, G152		V <sub>OFF</sub> level
	$\overline{OE2} = \text{"H"}$	G2, G5, G8, ...G74, G81 ... G150, G153		
	$\overline{OE3} = \text{"H"}$	G3, G6, G9, ...G75, G82 ... G151, G154		
	$\overline{OE1} = \text{"L"}$	G1, G4, G7, ...G73, G80 ... G149, G152		Normal data output
	$\overline{OE2} = \text{"L"}$	G2, G5, G8, ...G74, G81 ... G150, G153		
	$\overline{OE3} = \text{"L"}$	G3, G6, G9, ...G75, G82 ... G151, G154		
L (154-out)	$\overline{OE1} = \text{"H"}$	G1, G4, G7, ...G148, G151, G154		V <sub>OFF</sub> level
	$\overline{OE2} = \text{"H"}$	G2, G5, G8, ...G149, G152		
	$\overline{OE3} = \text{"H"}$	G3, G6, G9, ...G150, G153		
	$\overline{OE1} = \text{"L"}$	G1, G4, G7, ...G148, G151, G154		Normal data output
	$\overline{OE2} = \text{"L"}$	G2, G5, G8, ...G149, G152		
	$\overline{OE3} = \text{"L"}$	G3, G6, G9, ...G150, G153		

### (3) Voltage setting

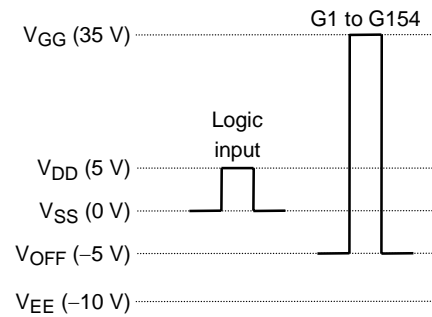
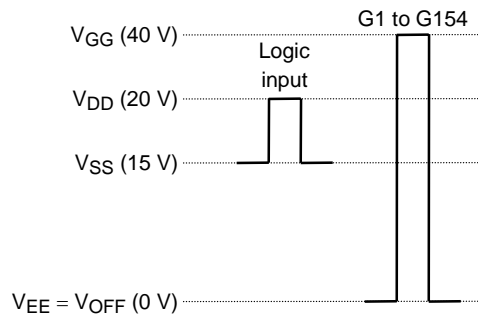
The VOFF level, which sets the LCD panel drive's output low level, can take on any value between VEE to VEE + 6 V.

(Example 1) Positive voltage output

$V_{GG} - V_{OFF} = 40 \text{ V}$   
 $V_{OFF} - V_{EE} = 0 \text{ to } 6 \text{ V}$   
 $V_{SS} - V_{EE} = 5 \text{ to } 15 \text{ V}$

(Example 2) Negative voltage output

$V_{GG} - V_{OFF} = 40 \text{ V}$   
 $V_{OFF} - V_{EE} = -10 \text{ to } -4 \text{ V}$   
 $V_{SS} - V_{EE} = -10 \text{ to } 0 \text{ V}$



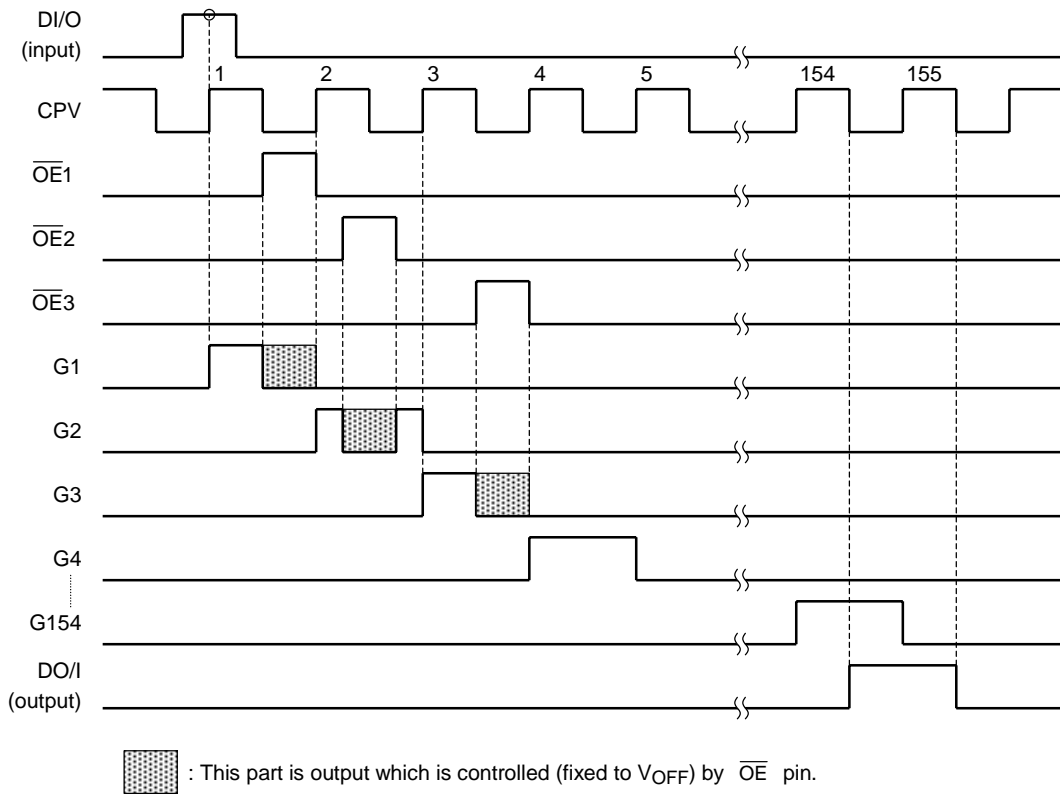
Note: The logic input here means input pins DI/O, DO/I, CPV, MODE and  $\overline{OE}1$  to  $\overline{OE}3$ .

The amplitude between V<sub>SS</sub> and V<sub>DD</sub> is applied to above pins.

Make sure that the voltage applied to the U/D pin is a high (= V<sub>DD</sub>) or low (= V<sub>SS</sub> or V<sub>EE</sub>) DC-level voltage.

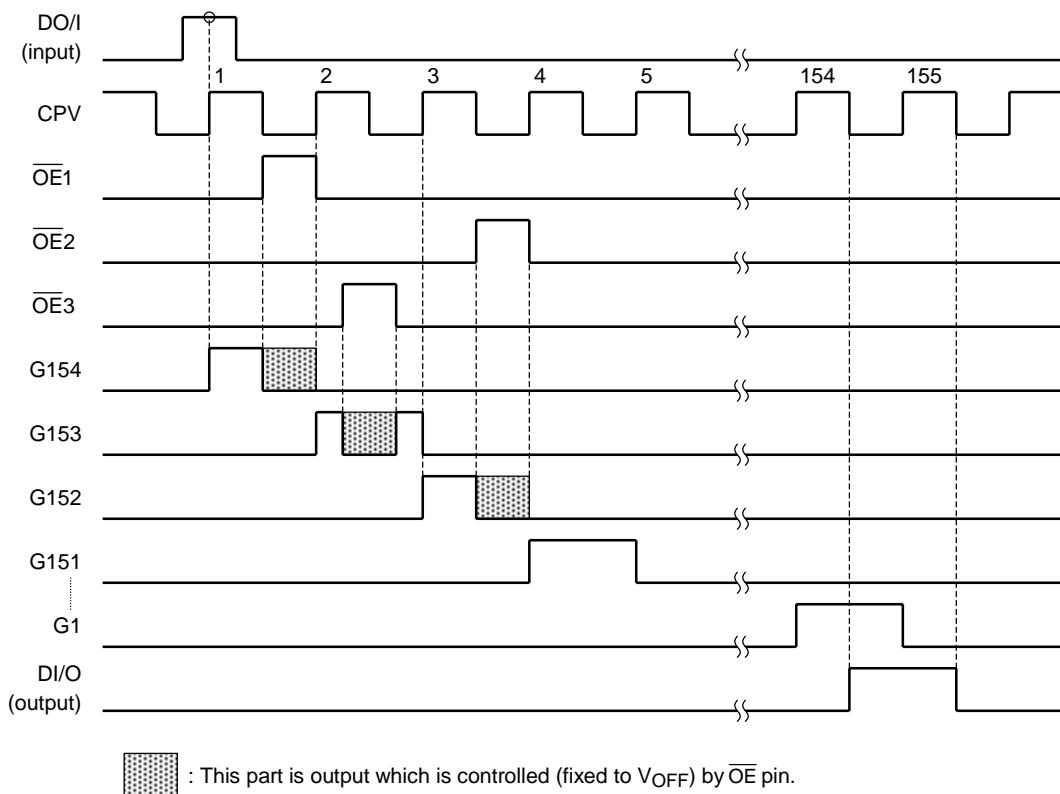
**Timing Diagram 1**

**154-output-pin (MODE = low), UP mode (U/D = high)**



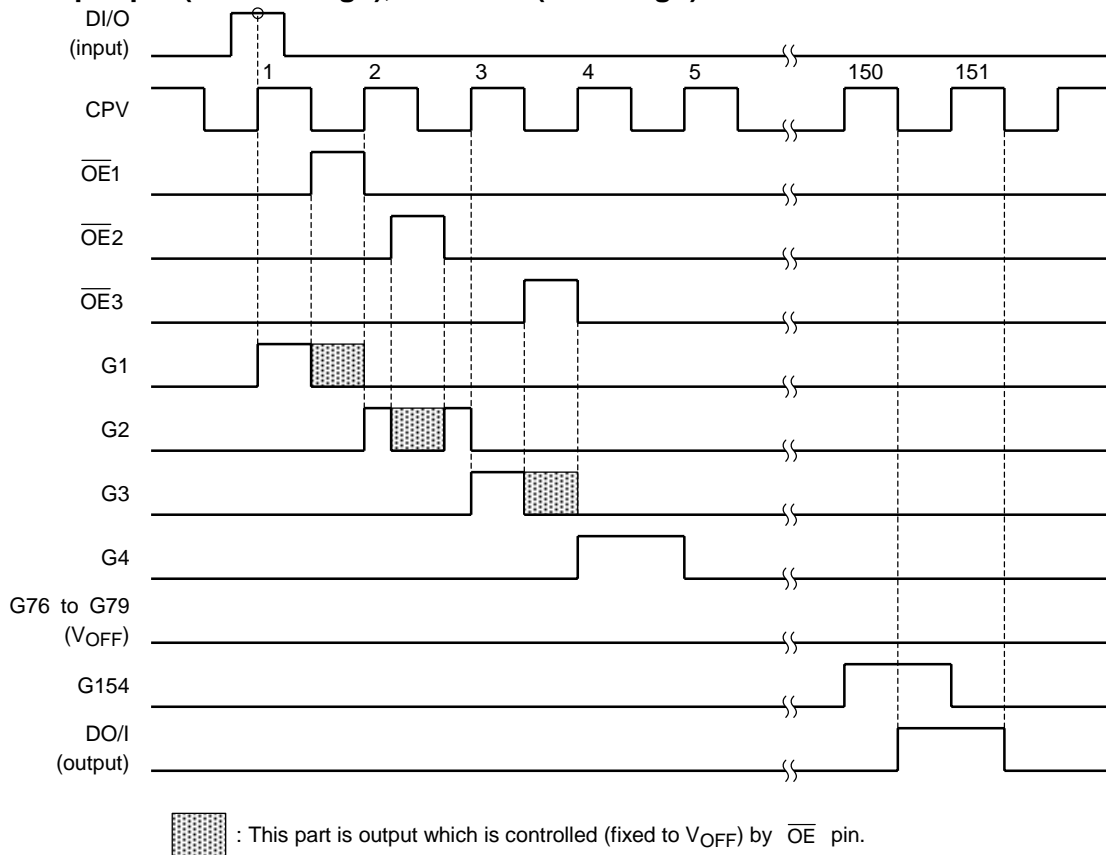
**Timing Diagram 2**

**154-output-pin (MODE = low), DOWN mode (U/D = low)**



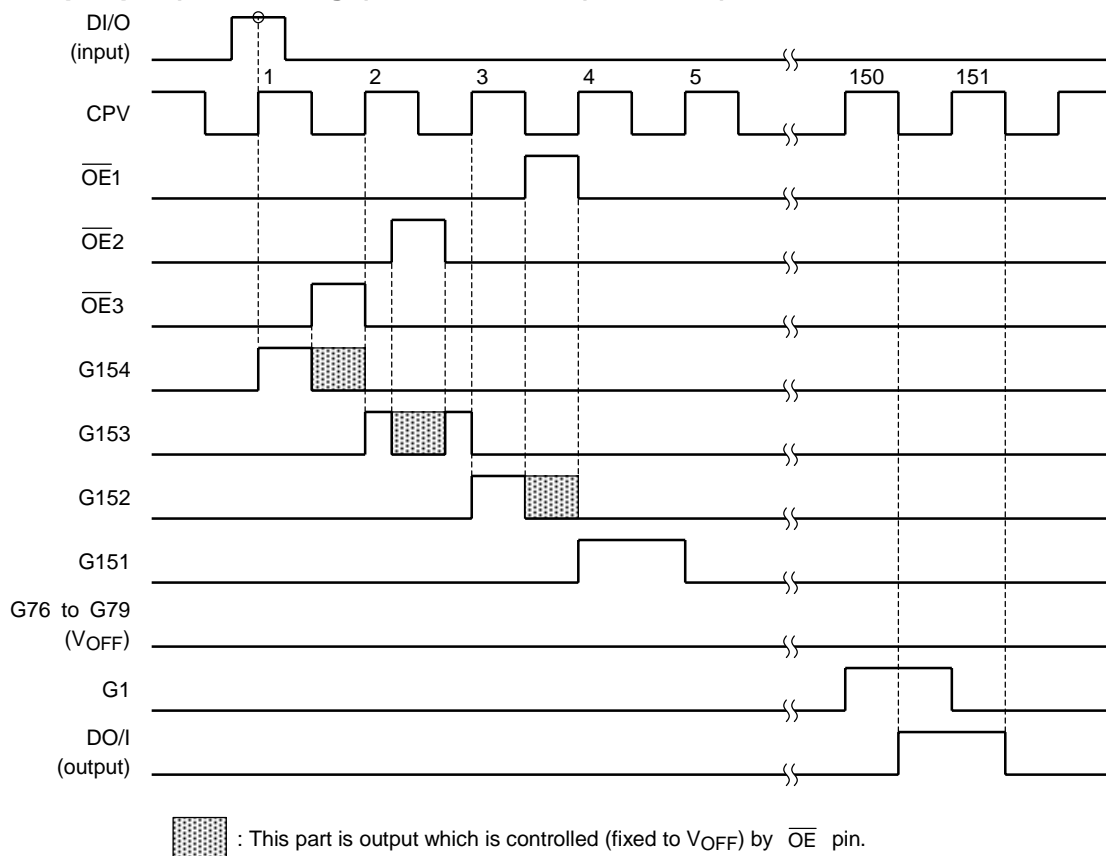
**Timing Diagram 3**

**150-output-pin (MODE = high), UP mode (U/D = high)**



**Timing Diagram 4**

**150-output-pin (MODE = high), DOWN mode (U/D = low)**



## Absolute Maximum Ratings ( $V_{SS} = 0\text{ V}$ )

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	$V_{DD}$	-0.3 to 22.0	V
Supply voltage (2)	$V_{SS}$	-0.3 to 16.5	
Supply voltage (3)	$V_{DD} - V_{SS}$	-0.3 to 7.0	
Supply voltage (4)	$V_{OFF}$	-0.3 to 7.0	
Supply voltage (5)	$V_{GG}$	-0.3 to 45.0	
Supply voltage (6)	$V_{GG} - V_{OFF}$	-0.3 to 45.0	
Input voltage	$V_{IN}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Storage temperature	$T_{stg}$	-55 to 125	°C

## Recommended Operating Conditions ( $V_{SS} = 0\text{ V}$ )

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	$V_{SS}$	5 to 15	V
Supply voltage (2)	$V_{DD}$	$V_{SS} + 3.0$ to $V_{SS} + 5.5$	
Supply voltage (3)	$V_{OFF}$	0 to 6	
Supply voltage (4)	$V_{GG} - V_{SS}$	17 to 25	
Operating temperature	$T_{opr}$	-20 to 75	°C
Operating frequency	$f_{CPV}$	DC to 100	kHz
Output load capacitance	$C_L$	300 (max)	pF/pin

## Electrical Characteristics

**DC Characteristics**  $\left( V_{GG} - V_{SS} = 17 \text{ to } 25 \text{ V}, V_{DD} = 3.0 \text{ to } 5.5 \text{ V}, V_{SS} = 0 \text{ V}, \right.$   
 $\left. T_a = -20 \text{ to } 75^\circ\text{C}, V_{EE} = -15 \text{ to } -5 \text{ V}, V_{OFF} = V_{EE} \text{ to } V_{EE} + 6 \text{ V} \right)$

Characteristics		Symbol	Test circuit	Test Condition	Min	Max	Unit	Relevant Pin
Input voltage	Low level	$V_{IL}$	—	—	$V_{SS}$	$0.1 \times (V_{DD} - V_{SS}) + V_{SS}$	V	(Note 1)
	High level	$V_{IH}$	—	—	$0.9 \times (V_{DD} - V_{SS}) + V_{SS}$	$V_{DD}$	V	(Note 1)
Output voltage	Low level	$V_{OL}$	—	$I_{OL} = 40 \mu\text{A}$	$V_{SS}$	$V_{SS} + 0.4$	V	DI/O, DO/I
	High level	$V_{OH}$	—	$I_{OH} = -40 \mu\text{A}$	$V_{DD} - 0.4$	$V_{DD}$	V	DI/O, DO/I
Output resistance	Low level	$R_{OL}$	—	$V_{OUT} = V_{EE} + 0.5 \text{ V}$ (Note 1)	—	1500	$\Omega$	G1 to G154
	High level	$R_{OH}$	—	$V_{OUT} = V_{GG} - 0.5 \text{ V}$ (Note 1)	—	1500	$\Omega$	G1 to G154
Input leakage current		$I_{IN}$	—	—	-1	1	$\mu\text{A}$	(Note 2)
Current consumption (1)		$I_{DD}$	—	(Note 3)	—	1500	$\mu\text{A}$	
Current consumption (2)		$I_{SS}$	—	(Note 3)	-200		$\mu\text{A}$	
Current consumption (3)		$I_{GG}$	—	(Note 3)	—	150	$\mu\text{A}$	

Note 1:  $V_{GG} - V_{EE} = 25 \text{ to } 35 \text{ V}$

Note 2: Input pins ... DI/O, DO/I, CPV,  $\overline{OE1}$  to  $\overline{OE3}$ , MODE

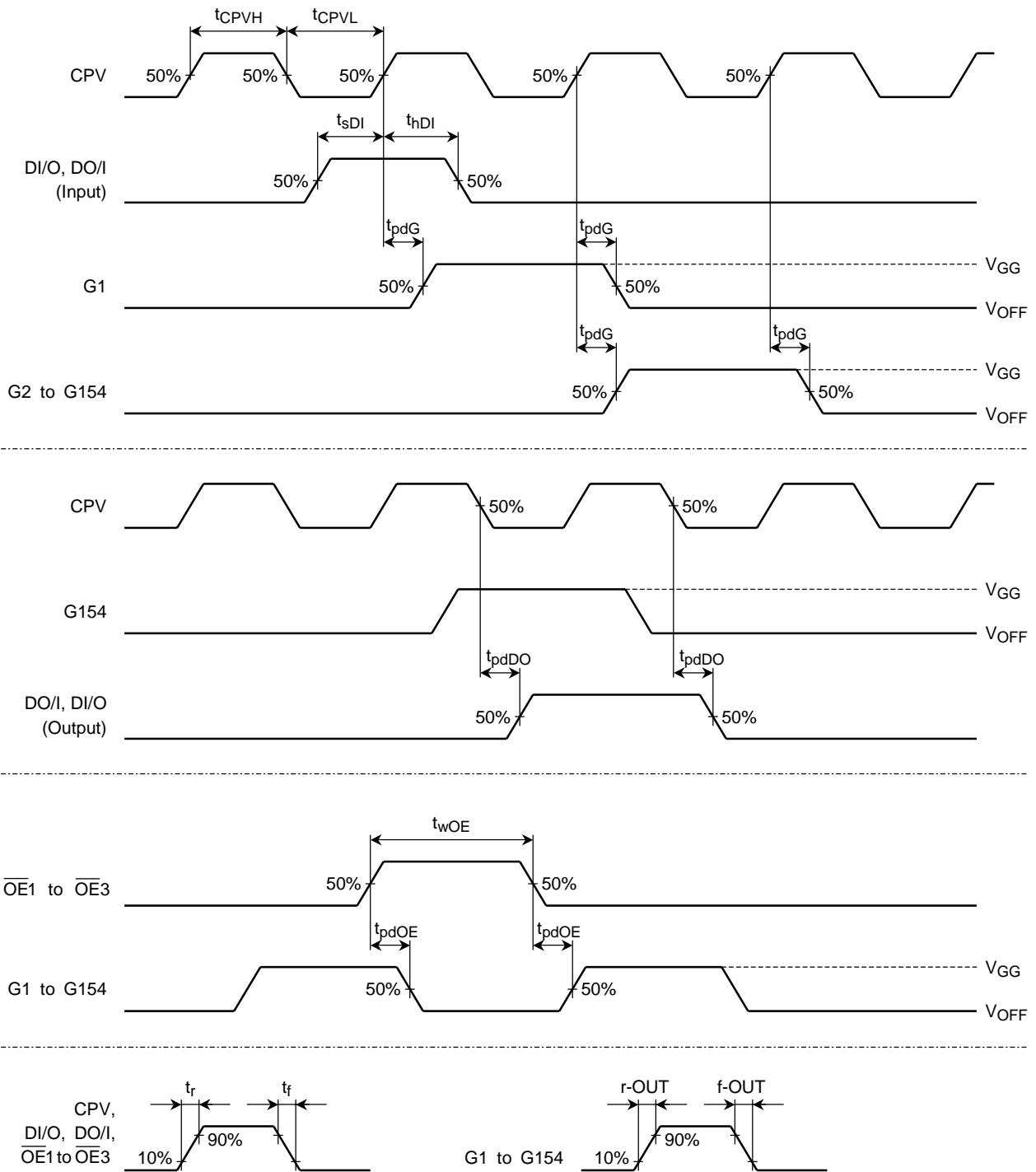
Note 3: Current consumption in 1/600-duty LCD.

Input  $V_{IH} = V_{DD}$ ,  $V_{IL} = V_{SS}$ ,  $f_{CPV} = 100 \text{ kHz}$

Start pulse period = 104.2 Hz,  $\overline{OE1}$  to  $\overline{OE3} = V_{SS}$ , no load

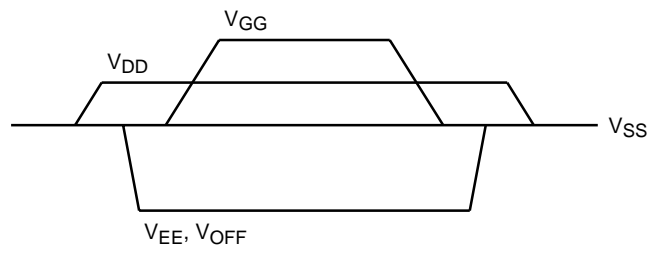
**AC Characteristics**  $\left( V_{GG} - V_{SS} = 17 \text{ to } 25 \text{ V}, V_{DD} = 3.0 \text{ to } 5.5 \text{ V}, V_{SS} = 0 \text{ V}, \right.$   
 $\left. T_a = -20 \text{ to } 75^\circ\text{C}, V_{EE} = -15 \text{ to } -5 \text{ V}, V_{OFF} = V_{EE} \text{ to } V_{EE} + 6 \text{ V} \right)$

Characteristics	Symbol	Test circuit	Test Condition	Min	Max	Unit
Clock period	$t_{CPV}$	—	—	—	100	kHz
CPV pulse width (H)	$t_{CPVH}$	—	—	5	—	$\mu\text{s}$
CPV pulse width (L)	$t_{CPVL}$	—	—	5	—	$\mu\text{s}$
Data set-up time	$t_{sDI}$	—	—	700	—	ns
Data hold time	$t_{hDI}$	—	—	700	—	ns
OE enable time	$t_{wOE}$	—	—	1	—	$\mu\text{s}$
Output delay time (1)	$t_{pdDO}$	—	$C_L = 30 \text{ pF}$	—	1000	ns
Output delay time (2)	$t_{pdG}$	—	$C_L = 300 \text{ pF}$	—	800	ns
Output delay time (3)	$t_{pdOE}$	—	$C_L = 300 \text{ pF}$	—	800	ns
Input rising time	$t_r$	—	$C_L = 300 \text{ pF}$	—	30	ns
Input falling time	$t_f$	—	$C_L = 300 \text{ pF}$	—	30	ns
Output rising time	r-OUT	—	$C_L = 300 \text{ pF}$	—	500	ns
Output falling time	f-OUT	—	$C_L = 300 \text{ pF}, V_{OFF} = V_{EE} = 0 \text{ V}$	—	500	ns



**Power Supply Sequence**

Turn power on in the order  $V_{SS} \rightarrow V_{DD} \rightarrow \text{Input signal} \rightarrow V_{EE} \rightarrow V_{OFF} \rightarrow V_{GG}$ .  
Turn power off in the reverse order.



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