Am2932

Program Control Unit/Push-Pop Stack

DISTINCTIVE CHARACTERISTICS

- **Powerful, 4-bit slice address controller for memories**
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- **Executes 16 instructions**
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- **Eight relative address instructions**
  Including Jump relative and Jump-to-Subroutine relative
- **Seventeen-level push/pop stack**
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- **Separate incrementer for program counter**
  A relative address may be computed and PC may be incremented by one on a single cycle

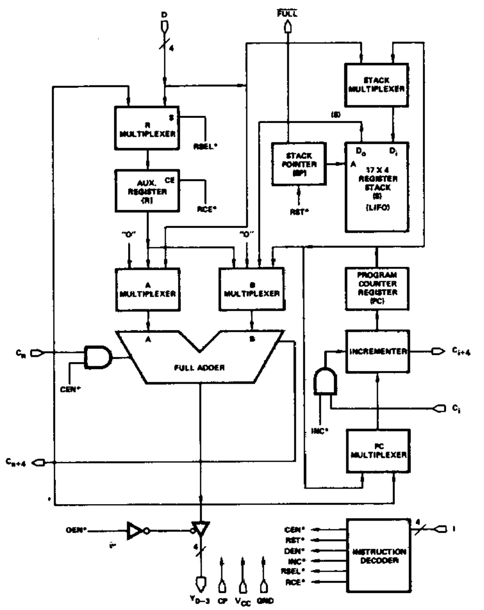
GENERAL DESCRIPTION

The Am2932 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2932s may be interconnected to generate a 16-bit address (64K words). The Am2932 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2932 performs five types of instructions. These are: 1. Fetch; 2. Jump; 3. Jump-to-Subroutine; 4. Return-from-Subroutine; and 5. Miscellaneous Instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1. the Program Counter (PC); 2. the Stack (S); 3. the auxiliary Register (R); and 4. the Direct inputs (D). Under control of the Instruction inputs (I_0-I_3), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register.

BLOCK DIAGRAM



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***INTERNAL**

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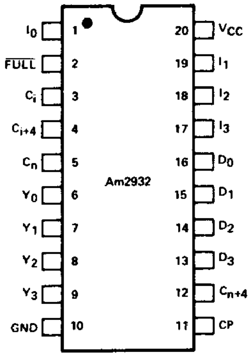
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-20



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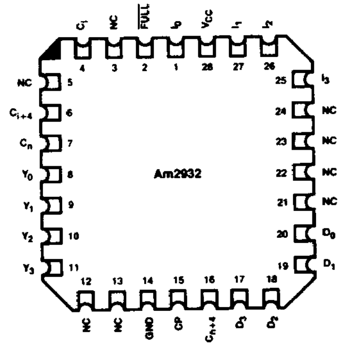

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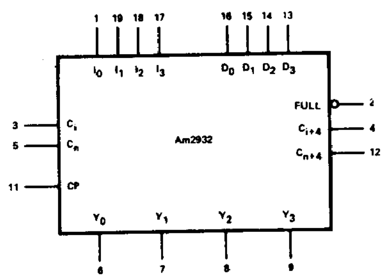
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
(DIP)



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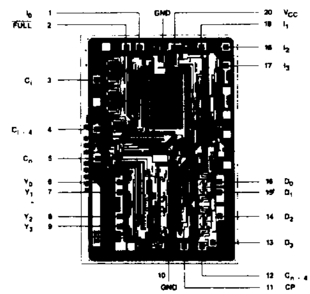
METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.134" x 0.200"
Pad numbers correspond to DIP pinout.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2932 D C B

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (−55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - L – 28-pin leadless chip carrier
  - X – Dice
- **Am2932** — Device type
  - Program Control Unit

Valid Combinations	
Am2932	DC, DCB, DMB LC, LMB XC, XM

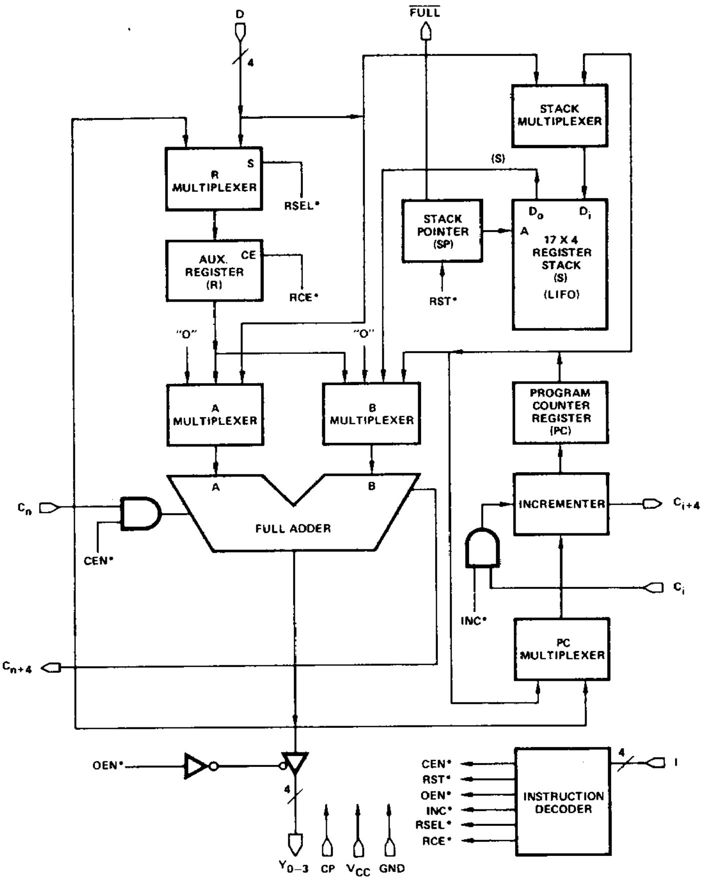
Valid Combinations
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	I_{0-3}	I	The four Instruction control lines to the Am2932, used to establish data paths and enable internal registers.
5	C_n	I	The carry-in to the Full Adder.
12	C_{n+4}	O	The carry-out of the Full Adder.
3	C_i	I	The carry-in to the program counter incrementer.
4	C_{i+4}	O	The carry-out of the program counter incrementer.
	Y_{0-3}	O	The four address outputs of the Am2932. These are three-state output lines. When enabled, they display the outputs of the Full Adder.
	D_{0-3}	I	The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.
2	$\overline{\text{Full}}$	O	The Full output is LOW when the LIFO stack is full - during and after the 17th push operation.
11	CP	I	The clock input to the Am2932. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

BLOCK DIAGRAM



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*INTERNAL

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ARCHITECTURE OF THE Am2932

The Am2932 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1. A full adder with input multiplexers
2. A Program Counter Register with an incrementer and an input multiplexer
3. A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4. An auxiliary register with an input multiplexer
5. An instruction decoder
6. Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition. The carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During the suspend instruction, the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP + 1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Instruction inputs call for it to be loaded.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled under Instruction control.

Am2932 INSTRUCTION SET

The Am2932 Instruction set can be divided into five types of instructions. These are:

- Fetches
- Jumps
- Jumps-to-Subroutine
- Return-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Fetches

As can be seen from Table I, there are four Fetch instructions (Instructions 4, 8, 9, 10). Under control of the Instructions inputs, the desired value is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instruction 10, R is loaded with PC. The RAM and Stack Pointer are not changed during a Fetch instruction.

Jumps

There are three Jump instructions (Instructions 5, 11, 12). Under control of the Instruction inputs, the desired value is placed at the Y outputs. Additionally, the value is incremented if C_i of the least significant device is HIGH and loaded into PC. The RAM, Stack Pointer and R are not changed during these instructions.

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Refer to Page 13-1 for Essential Information on Military Devices

Jumps-to-Subroutine

There are two Jump-to-Subroutine instructions (Instructions 13 and 14). Under control of the Instruction inputs, the desired value is placed on the Y outputs. On the rising edge of the clock the value is incremented* and loaded into PC; PC is loaded into the RAM at location SP + 1; and SP is incremented.

During these instructions, R is not changed.

Return-from-Subroutine (Instruction 7)

Under control of the instruction inputs, S is placed at the Y outputs. Additionally, the value of S is incremented* and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock). During this instruction, R is not changed.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM and R are unchanged.

Load R (Instruction 15)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 6)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 2)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 3)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is not changed.

Suspend (Instruction 1)

The Suspend instruction inhibits any change in PC, SP, R and RAM and forces the Y outputs into the high impedance state.

TABLE I–Am2932 INSTRUCTION SET

Instruction Number	I_3	I_2	I_1	I_0	Mnemonic	Instruction	Y_0-Y_3	Next State (after CP ⎍) - Note 2: PC	R	RAM	SP
0	L	L	L	L	PRST	RESET	"0"	"0" + C_i	–	–	Reset
1	L	L	L	H	PSUS	SUSPEND	Z (Note 1)	–	–	–	–
2	L	L	H	L	PSHD	PUSH D	PC	PC + C_i	–	D→Loc SP + 1	SP + 1
3	L	L	H	H	POPS	POP S	S	PC + C_i	–	–	SP – 1
4	L	H	L	L	FPC	FETCH PC	PC	PC + C_i	–	–	–
5	L	H	L	H	JMPD	JUMP D	D	D + C_i	–	–	–
6	L	H	H	L	PSHP	PUSH PC	PC	PC + C_i	–	PC→Loc SP + 1	SP + 1
7	L	H	H	H	RTS	RETURN S	S	S + C_i	–	–	SP – 1
8	H	L	L	L	FR	FETCH R	R	PC + C_i	–	–	–
9	H	L	L	H	FPR	FETCH PC + R	PC + R + C_n	PC + C_i	–	–	–
10	H	L	H	L	FPLR	FETCH PC→R	PC	PC + C_i	PC	–	–
11	H	L	H	H	JMPR	JUMP R	R	R + C_i	–	–	–
12	H	H	L	L	JPPR	JUMP PC + R	PC + R + C_n	PC + R + C_n + C_i	–	–	–
13	H	H	L	H	JSBR	JSB R	R	R + C_i	–	PC→Loc SP + 1	SP + 1
14	H	H	H	L	JSPR	JSB PC + R	PC + R + C_n	PC + R + C_n + C_i	–	PC→Loc SP + 1	SP + 1
15	H	H	H	H	PLDR	LOAD R	PC	PC + C_i	D	–	–

Notes: 1. Z = High impedance state (outputs "OFF").
2. – = No change.

PC – Program Counter
R – Auxiliary Register
S – Stack Top

SP – Stack Pointer
D – Direct Inputs

*If C_i of the least significant device is HIGH.

APPLICATIONS

The Am2932 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2932 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901Cs via a 16-bit register.

The Address outputs (Y) of the Am2932 are passed to the address bus.

The C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The control inputs of the Am2932 ($I_{0\text{-}3}$, C_i and C_n of the least significant device) are shown originating at the Pipeline Register.

For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

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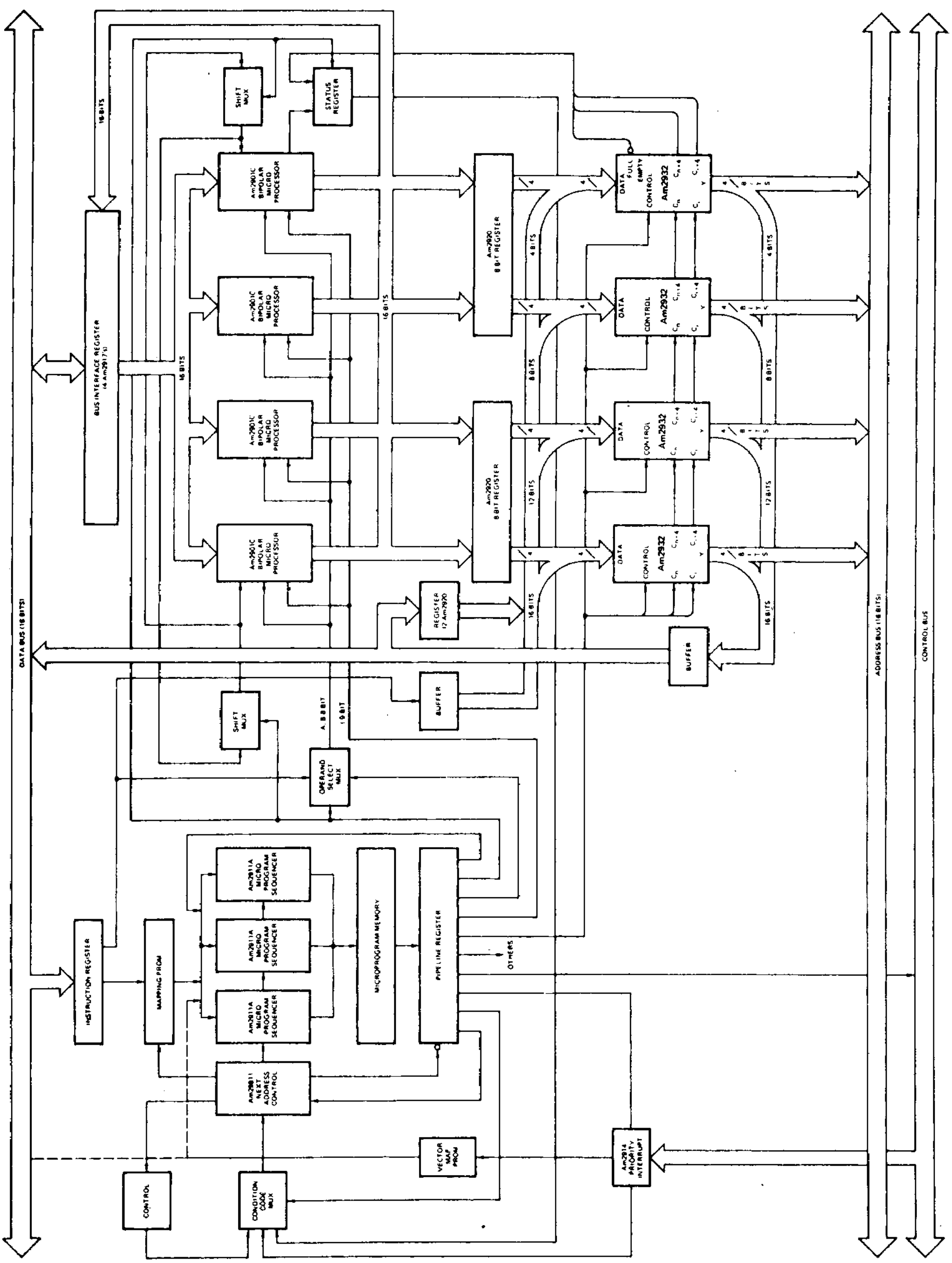

Figure 1. Typical 16-Bit Microcomputer Design.

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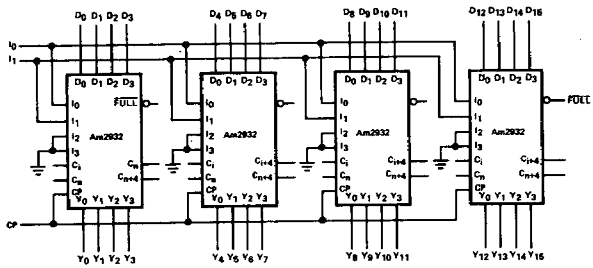

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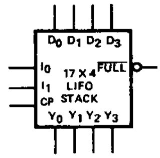
I_1	I_0	INSTRUCTION	Y OUTPUTS
L	L	RESET	"0"
L	H	SUSPEND	Z (HIGH IMPEDANCE)
H	L	PUSH D	SEE NOTE 1
H	H	POP S	TOP OF STACK



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Equivalent Logic Symbol for AM2932 with I_2, I_3 Grounded

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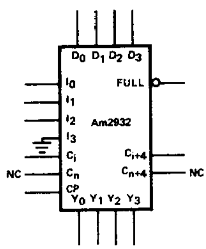
This figure shows the use of four Am2932s as a 17-word by 16-bit LIFO stack by grounding I_2 and I_3. The effect of grounding I_3 is shown in Figure 3.

Note 1. During this instruction, PC is placed on the Y outputs. If C_i is held LOW, the Y outputs will be LOW for this instruction after the device is initialized with a Reset instruction.

Figure 2. Application of Four Am2932s as a 17-Word by 16-Bit LIFO Stack.



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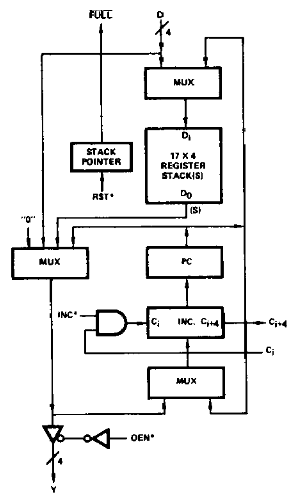
I_2	I_1	I_0	INSTRUCTION
L	L	L	RESET
L	L	H	SUSPEND
L	H	L	PUSH D
L	H	H	POP S
H	L	L	FETCH PC
H	L	H	JUMP D
H	H	L	PUSH PC
H	H	H	RETURN S



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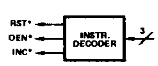

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Figure 3. Equivalent Circuit of Am2932 with I_3 Grounded.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
(Ambient) Temperature Under Bias .... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State .... −0.5V to $+V_{CC}$ max
DC Input Voltage .... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current .... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature .... 0°C to +70°C
Supply Voltage .... +4.75V to +5.25V

Military (M) Devices
Temperature .... −55°C to +125°C
Supply Voltage .... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, $V_{IN} = V_{IL}$ or V_{IH}	Y_0, Y_1, Y_2, Y_3, C_{n+4}, C_{i+4}	$I_{OH} = -1.6mA$	2.4			Volts
			$\overline{FULL}$	$I_{OH} = -1.2mA$	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, $V_{IN} = V_{IL}$ or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			C_{n+4}, C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{FULL}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		D_{0-3}			−.360	mA
				I_{0-3}, CP			−.702	
				C_i			−2.0	
				C_n			−3.69	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		D_{0-3}			20	μA
				I_{0-3}, CP			40	
				C_i			90	
				C_n			250	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX		T_C = −55 to +125°C			210	mA
				T_C = +125°C			145	
				T_A = 0 to 70°C			190	
				T_A = 70°C			160	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

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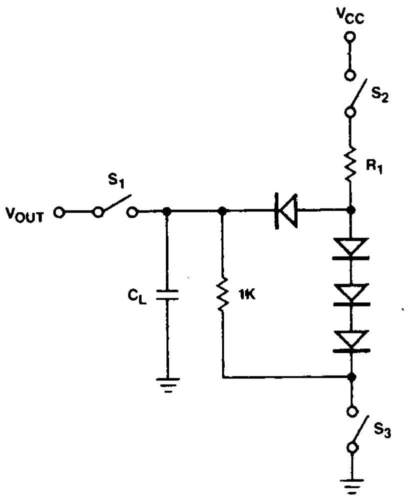
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

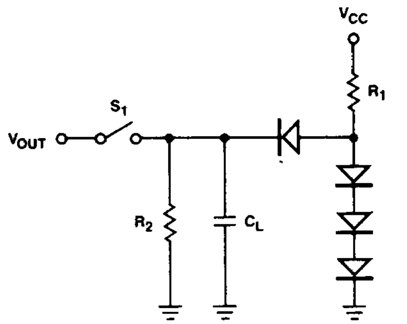
A. THREE STATE OUTPUTS



TCR01350

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}}$$

B. NORMAL OUTPUTS



TCR01370

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}}$$

Notes: 1. $C_L = 50pF$ includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0pF$ for output disabled tests.

TEST OUTPUT LOADS FOR Am2932

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
4	C_{i+4}	B	240	1.5K
6–9	Y_{0-3}	A	240	1K
12	C_{n+4}	B	240	1.5K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

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Am2932 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2932. Measurements are made at 1.5V with $V_{IL} = 0V$ and $V_{IH} = 3.0V$. For three-state disable tests, $C_L = 5.0pF$ and measurement is to 0.5V change on output voltage level.

I. GUARANTEED PERFORMANCE OVER COMMERCIAL OPERATING RANGE.

$V_{CC} = 4.75$ to $5.25V$, $T_A = 0$ to $+70°C$

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IB
Output Enable/Disable Times.
All in ns.
$C_L = 5.0pF$ for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	80	55

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. $C_L = 50pF$.

	To Output				
From Input	Y	C_{i+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	81	77	91	80	69
C_n	32	25	45	–	–
C_i	–	–	22	22	–
CP	69	61	78	43	55
D	39	–	50	–	–

TABLE ID
Set-up and Hold Times.
All in ns.
All relative to clock
LOW-to-HIGH transition.

	CP:	
Input	Set-up Time	Hold Time
C_n	43	0
C_i	32	5
D	52	2
I_{3-0}	114	0

Note: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

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Refer to Page 13-1 for Essential Information on Military Devices

II. GUARANTEED PERFORMANCE OVER MILITARY OPERATING RANGE.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	85	60

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input	To Output				
	Y	C_{i+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{\text{Full}}$
I_{3-0}	88	82	97	87	78
C_n	37	30	46	−	−
C_i	−	−	23	23	−
CP	74	66	84	45	60
D	44	−	55	−	−

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: ↑ Set-up Time	CP: ↑ Hold Time
C_n	52	0
C_i	37	5
D	60	2
I_{3-0}	124	0

Note: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2920	8-Bit Register
Am2922	Condition Code MUX

03641B

Refer to Page 13-1 for Essential Information on Military Devices