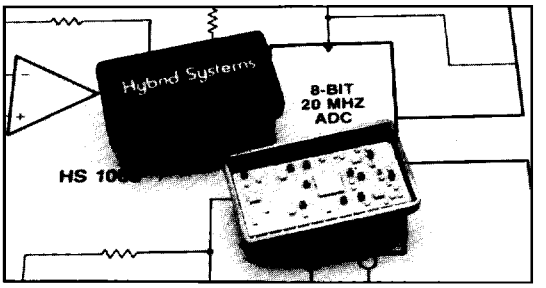
HS1068

FLASH PLUS 8-BIT 20 MSPS A/D CONVERTER

FEATURES

- Complete analog front-end and ADC in a single package
- 20 MHz sampling rate
- Pin strappable unipolar or bipolar input ranges
- Offset and gain adjust pins
- Three-state output



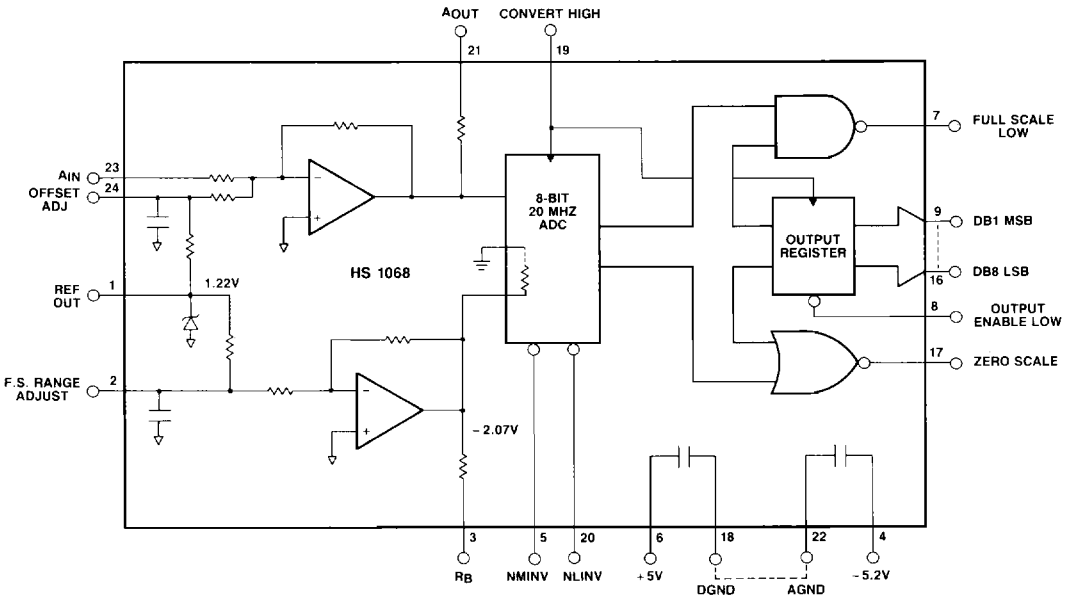
DESCRIPTION

The HS1068 is a complete FLASH ANALOG to DIGITAL CONVERTER that combines all circuitry required to convert high speed analog signals into 8-bit digital data at a rate of 20 mega samples per second. The HS1068 is completely self contained providing an 8-bit, 20 MHz, flash A/D; a wideband analog input amplifier; precision voltage reference and three-state outputs in a single 24-pin package.

Combining all analog support circuitry with the A/D converter offers significant savings of board space; along with component, assembly and design costs.

Designed to meet demanding military applications, the HS1068 is housed in a hermetic 24-pin DIP and operates with guaranteed performance over the full −55°C to +125°C case operating temperature range. Processing in compliance with MIL-STD-883C is available.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{CC}	7.0	V
	V_{EE}	−7.0	V
Digital Input Voltage	$V_{IN}(D)$	5.5	V
Analog Input Voltage	$V_{IN}(A)$	±5.5	V
Reference Voltage Span	—	2.2	V
Applied Output Voltage	—	5.5	V
Junction Temperature	T_J	150	°C
Operating Case Temperature	T_C	140	°C
Storage Temperature	T_{STG}	−65 to +150	°C

*Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEMPERATURE RANGE						UNITS
		0°C to +70°C			−55°C to +125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Analog Supply Voltage	V_{EE}	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
Analog Ground	AGND	−0.1	0	+0.1	−0.1	0	+0.1	V
Analog Input, Range ADJ and OFFSET ADJ Open	$V_{IN}(A)$	−0.5		+0.5	±0.5		+0.5	V
Digital Input Voltage, HIGH	$V_{IN}(D)$	2.0			2.0			V
Digital Input Voltage, LOW				0.8			0.8	V
Applied Output Voltage	V_o			V_{CC}			V_{CC}	V
CONV Pulse Width, LOW	t_{PWL}	18			18			nS
CONV Pulse Width, HIGH	t_{PWH}	22			22			nS
Clock Frequency, Max	f_{CLK}	20			20			MHz
Operating Ambient Temperature	T_A	0		70				°C
Operating Case Temperature	T_C				−55		+125	°C

PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N				8.0			8.0	Bits
Integral Linearity Error	E_{LI}	DC, Best Straight Line					±0.35		LSB
Differential Linearity Error	E_{DI}	DC					±0.25		LSB
Signal-to-Noise Ratio[1]	SNR								
RMS Signal/RMS Noise + Distortion		1.123 MHz Input		47			47		dB
		2.234 MHz Input		46			46		dB
		4.456 MHz Input		43			43		dB
Differential Phase	DP	F_S = 4 x NTSC Carrier		1			1		Degree
Differential Gain	DC	F_S = 4 x NTSC Carrier		2			2		%
Aperture Error	E_{AP}			±60			±60		pS
Code Size	CS		25		175	25		175	%
Full Power Bandwidth	BW	No Spurious Code	7	13		5	13		MHz
Input Amplifier Bandwidth	ABW	Freq −3 dB		20			20		MHz
Settling Time (to 0.4%)	t_S	Full Scale Transition		45			45		nS
Amplifier Overshoot	O_S			1			1		%
Overload Recovery	t_{REC}	±100 mV Overdrive		5			5		nS
Input Amplifier Noise		10 MHz Bandwidth[2]		125			125		μVRMS
Range AMP Bandwidth			100			100			kHz
Range AMP Settling		One Volt Step at R_{BOT}		14	50		14	50	μSec

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Maximum Conversion Rate	F_S	V_{CC}, V_{EE} = MIN	20			20			MHz
Sampling Time Offset	t_{STO}	V_{CC}, V_{EE} = MIN	0	10	10	0	10	10	nS
Digital Output Delay	t_D	V_{CC} = MIN	15		28	15		28	nS
Digital Output Enable	t_{PZL}	V_{CC} = MIN		20			20		nS
Digital Output Disable	t_{PHZ}	V_{CC} = MIN		15			15		nS
Full Scale Flag	t_{CFSL}	V_{CC} = MIN		25			25		nS
Zero Scale Flag	t_{CZSH}	V_{CC} = MIN		29			29		nS
CONV Pulse Width, LOW	t_{PWL}	V_{CC} = MIN	18			18			nS
CONV Pulse Width, HIGH	t_{PWH}	V_{CC} = MIN	22			22			nS

INPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Input Current, Logic LOW	I_{IL}	NMINV, NLINV			−0.6			−0.6	mA
		OE			−0.4			−0.4	mA
		CONV			−0.8			−0.8	mA
Input Current, Logic HIGH	I_{IH}	NMINV, NLINV			50			50	μA
		OE			20			20	μA
		CONV			70			70	μA
Input Voltage, Logic LOW	V_{IL}				0.8			0.8	V
Input Voltage, Logic HIGH	V_{IH}		2.0			2.0			V
Analog Input Resistance	R_{IN}			1K	1.05K		1K	1.05K	Ω
Analog Input Capacitance	C_{IN}			3			3		pF
Input Offset Current	I_B	$I_B = V_{OS} \div$ 1K Ohm			±4			±4	μA
Gain Error	E_G			±0.4			±0.4		%
Bipolar Offset Error	V_{OS}	Offset Open		±1			±1		LSB
Unipolar Offset Error	V_{OS}	Offset ADJ = GND		±1			±1		LSB
Bipolar Offset Error Tempco	T_{CB}	LSB's/°C Case temp rise		+0.05			+0.05		LSB/°C
Unipolar Offset Error Tempco	T_{CU}	LSB's/°C Case temp rise		+0.05			+0.05		LSB/°C

DIGITAL OUTPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Output Leakage Current, Logic LOW	I_{LOL}				−20			−20	μA
Output Leakage Current, Logic HIGH	I_{LOH}				20			20	μA
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 12 mA[3]		0.25	0.4		0.25	0.4	V
Output Voltage, Logic HIGH	V_{OH}	I_{OH} = −1 mA[3]	2.4	3.4		2.4	3.4		V
Short Circuit Output Current	I_{OS}	V_{CC} = MAX, Output HIGH	−30		−130	−30		−130	mA
Output Capacitance	C_{OUT}								

REFERENCE

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{REF} OUT		1.224		1.19	1.224	1.26	V
Reference Current, Sourced	I_{REF}	600Ω, V_{REF} to GND			2.0			2.0	mA
R_{BOT} Adjustment Range	R_{ADJ}	Recommended Range[4]		±0.2			±0.2		V

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POWER SUPPLIES

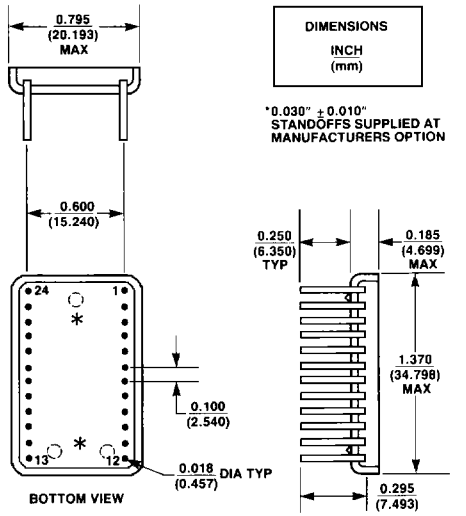
PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Digital Supply Current	I_{CC}	V_{CC} = MAX, Static[5]		101			110		mA
Digital Supply Current	I_{CC}	V_{CC} = MAX, Dynamic[6]		117			125		mA
Analog Supply Current	I_{EE}	V_{EE} = MAX, Static[5]		207			207		mA
Power Dissipation	P_D	V_{CC} = MAX, V_{EE} = MAX Static[5]		1.67			1.75		W
Power Dissipation	P_D	V_{CC} = MAX, V_{EE} = MAX Dynamic[6]		1.75			1.826		W

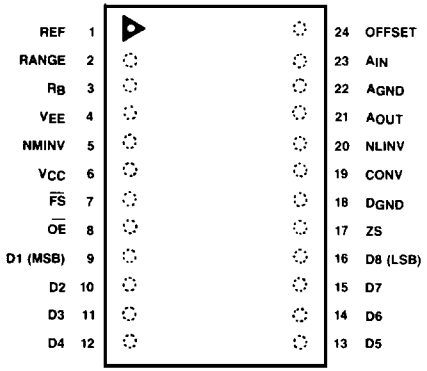
NOTES:
1. SNR = Signal/Noise + Distortion, f_{SAMPLE} = 20 MHz.
2. Referred to input (AV = −2).
3. To minimize power dissipation within the HS 1068 it is better to load the device with a minimal (1LSTTL) load.
4. Operation is possible down to R_{BOT} = −1.1V with reduced dynamic performance specifications.
5. DC input, Output Codes = All low, 1 LSTTL load.
6. 1.1 MHz FS Input, 1 LSTTL load.
7. Specifications subject to change without notice.

PIN ASSIGNMENTS

PIN	SYMBOL	FUNCTION
1	REF	+1.22V Reference Output
2	RANGE	Gain adjust Input, Adjusts −2.0V REF Nominal @Flash
3	R_B	Test Point, −2.0V Nominal @Flash
4	V_{EE}	Negative Supply Voltage, −5.2V
5	NMINV	Not Most Significant Bit Invert
6	V_{CC}	Positive Supply Voltage, +5.0V
7	FS	Full Scale Low, Overflow Detector
8	OE	Output Enable, "High" Tristates Output Data Line
9	D1(MSB)	Data Bit 1
10	D2	Data Bit 2
11	D3	Data Bit 3
12	D4	Data Bit 4
13	D5	Data Bit 5
14	D6	Data Bit 6
15	D7	Data Bit 7
16	D8(LSB)	Data Bit 8
17	ZS	Zero Scale, Underflow Detector
18	DGND	Digital Ground
19	CONV	Convert
20	NLINV	Not Least Significant Bits Invert
21	A_{OUT}	Test Point (Amplifier Output, Flash Input)
22	AGND	Analog Ground
23	A_{IN}	Analog Signal Input
24	OFFSET	Offset Adjust

PACKAGE OUTLINE





APPLICATIONS INFORMATION

THEORY OF OPERATION

The HS 1068 consists of four circuit blocks: the input buffer amplifier, voltage reference, flash converter and digital output logic. Analog and digital grounds are separated to provide flexibility in system grounding and decoupling.

The input amplifier has been designed to be compatible with baseband video signals. The input range is 1 Volt p-p, with pin strap selectable offsets to accommodate 0 to 1 Volt unipolar or ±0.5 Volt bipolar ranges. Typical sources can directly drive the 1 kOhm input impedance, or external resistors to ground can be used to terminate 75 or 50 Ohm cabling. The gain is set to −2 to provide 0 to −2 Volts to the flash converter. A resistor isolated (470 Ohm) analog output test point is available for debugging or for use in application circuits. Settling time is optimized at the factory by an internal variable capacitor.

An internal +1.22 Volt bandgap voltage reference is used to derive a −2.07 Volt nominal reference which drives the flash resistor ladder. The +1.22 Volt reference is capable of sourcing up to 2 mA to drive external application circuits. A resistor isolated (470 Ohms) negative reference output (Rbot) is also available for use in application circuits. These two outputs can be used with external trimpots to obtain calibration of system offset and gain with good power supply rejection. In this case the trimpot ends would go to the two references and the wiper brought through a resistor to the offset or range adjust pins. The HS 1068 is factory trimmed for offset and gain after 15 minute warmup under still room temperature air conditions.

The gain of the converter is set by trimming the reference voltage at the bottom of the flash resistor ladder. This is equivalent to trimming the full scale range at the flash. A maximum adjustment range of ±0.2 Volts is recommended which corresponds to a ±10% gain change. The unit will operate under reduced dynamic performance specifications with the reference as low as 1.5V, corresponding to a gain increase of 33%. Gain decreases can easily be obtained by using a resistive divider at the analog input pin (see Analog Input section).

The A/D is an 8-bit fully parallel flash converter capable of digitizing at rates above 20 MSPS. A single convert (CONV) signal controls the conversion operation. The flash itself consists of 255 sampling comparators, encoding logic and a latched output register. On the rising edge of the CONV signal, the comparators are latched and on the falling edge, the 255 to 8 encoding is performed. The 8 bit value is transferred to a flash-internal data register on the next rising edge. At this time the internal zero scale and fullscale comparisons are made. At the third rising edge the data is latched into the output register. The zero scale and full scale flags will be valid before this third rising edge, to allow over and underflow conditions to be detected simultaneously with the suspect data. This register also improves output fanout capability while providing a high-impedance disable function at the outputs. Data is latched into the output register regardless of whether the output is enabled or disabled.

POWER SUPPLIES

The HS 1068 requires two power supply voltages: V_{CC} at +5.0 Volts and V_{EE} at −5.2 Volts nominal. The return path for I_{EE} is through A_{GND}. The return path for most of I_{CC} is D_{GND}. A small amount of I_{CC} is internally separately routed from the V_{CC} pin to the analog operational amplifiers. A_{GND} and D_{GND} are not internally connected. In normal operation they would be tied together at one point underneath the converter. In systems with unusually noisy digital grounds, some resistive isolation between A_{GND} and D_{GND} may be necessary. In this case a small (0.1 μF) decoupling capacitor may be necessary from V_{CC} to A_{GND} to keep the V_{CC} noise from the op-amps. The voltage differential between A_{GND} and D_{GND} should be less than ±0.5V. An alternate method of isolation would involve keeping the A_{GND} and D_{GND} tied together under the converter and using small resistors in series with ferrite beads to isolate the converter's D_{GND} from noise-generating bus drivers. These resistors cannot be too large as they will degrade the noise margin at the non-isolated TTL inputs.

NAME	FUNCTION	VALUE	PIN
V_{CC}	Positive Power Supply	+5.0V	6
V_{EE}	Negative Power Supply	−5.2V	4
A_{GND}	Analog Ground	0.0V	22
D_{GND}	Digital Ground	0.0V	18

ANALOG INPUT

The HS 1068 has a nominal input impedance of 1K Ohm and an input voltage range of 1 Volt p-p. The HS 1068 can accept either unipolar 0 to 1V or bipolar ±0.5V. Both the input impedance and input voltage range may be changed for operation in other modes. The values of two external input resistors can determine the input impedance and voltage range of the device. Suggested values for various input impedances and voltage ranges are shown in Table 1.

For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate series input resistor R1 and shunt resistor R2 (used to form an input "T" attenuator).

$$R2 = \frac{1}{\frac{VR}{Z_{IN}} - \frac{1}{1000}}$$

$$R1 = Z_{IN} - \frac{1000\ R2}{R2 + 1000}$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is the input resistor R_{IN} (internal).

NAME	FUNCTION	VALUE	PIN
A_{IN}	Analog Input Voltage	See Text	23

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CONTROL INPUTS

Two control inputs are provided for changing the format of the output data. When NMINV is tied to logic "0" the most significant bit of the output data is inverted. When the NLINV is tied to logic "0" the seven least significant bits of the output data are inverted. By using these DC controls, the output data can be read in binary, inverted binary, two's complement or inverted two's complement formats. Output data versus input voltage and control input state is illustrated in Table 2.

NAME	FUNCTION	VALUE	PIN
NMINV	Not Most Significant Bits Invert	TTL	5
NLINV	Not Least Significant Bits Invert	TTL	20

REFERENCE

The HS 1068 includes circuitry for generating the negative voltage necessary for the flash converter. Two reference voltages are made available for application circuits. The actual bandgap reference (+1.22 Volts) is brought out directly. The fullscale reference at the bottom of the flash resistor ladder is brought out through a 470 Ohm isolation resistor. If external trimpots are to be used to trim out system errors, these pins provide tracking sources exhibiting good power supply rejection for that purpose.

NAME	FUNCTION	VALUE	PIN
REF	Reference Output	1.22V	1
R_{BOT}	Negative REF	−2.07V	3

CONVERT

The HS 1068 samples within 10 nS of the rising edge of the "CONV" signal. Data is latched into the flash data resigter on the next rising edge, then into the output register on the next rising edge. Note that there are minimum width requirements on the waveshape of the CONV signal. If these requirements are met, sampling frequencies higher than 20 MHz can be obtained. However, the performance specifications are only tested with a squarewave 20 MHz convert clock and therefore are only guaranteed under these conditions.

NAME	FUNCTION	VALUE	PIN
CONV	A/D Clock Input	TTL	19

DATA OUTPUTS

The outputs of the HS 1068 are LSTTL compatible and are capable of driving ten STTL loads to 50 LSTTL loads. The outputs can be put into the high impedance state by use of the output enable (low) control pin. A TTL low will enable the outputs. Note that the zeroscale and fullscale flags are unaffected by outenlow.

NAME	FUNCTION	VALUE	PIN
D1 (MSB)	Most Significant Data Bit	TTL	9
D2		TTL	10
D3		TTL	11
D4		TTL	12
D5		TTL	13
D6		TTL	14
D7		TTL	15
D8 (LSB)	Least Significant Data Bit	TTL	16

CALIBRATION

The HS 1068 is trimmed after warmup at room temperature with still air. Operation in different ambient temperatures or different airflows may require offset voltage adjustment if absolute DC accuracy is important. The offset adjust pin is used for this purpose, as well as for choosing the unipolar/bipolar range of the converter. The recommended factory-trimmed bipolar range is obtained by leaving this pin "open" (NC). The factory trimmed unipolar range is obtained by shorting this pin to ground.

The Thevenin model of this pin consists of 600 Ohms in series with a +0.6 Volt voltage source. When shorted to ground 1mA flows through this pin. Note also that this 1mA "uses up" 1mA of the current which would be available for application circuit use out the V_{REF} pin. V_{REF} loading should be kept under 1mA when the converter is used in unipolar mode. When adjusting offset in the unipolar mode it is necessary to construct a circuit which can sink 1mA to some delta voltage around ground. A simple circuit would use a trimpot connected as a rheostat to obtain 1600 Ohms nominal between the offset pin and −2.07V (R_{BOT}) (Figure 1). A rheostat connection depends upon absolute resistor stability over temperature for its' temperature stability. Moreover, with 1mA through it the trimpot will incur self-heating errors. A more elegant circuit would use less current in a resistor ratio with an opamp buffer as shown in Figure 2.

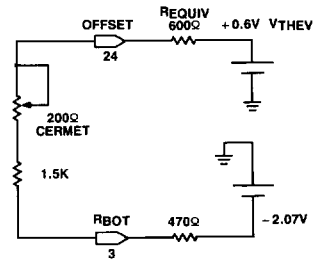

Figure 1. Unipolar Mode — External Offset Adjustment

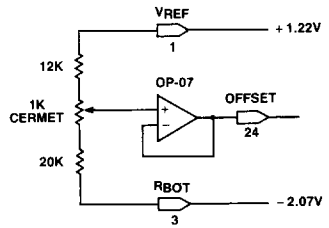

Figure 2. Unipolar Mode — Stable External Offset Adjustment

The bipolar mode offset adjust requires a source sitting close to +0.6 Volts with fairly high impedance. A ±30mV range at the amplifier output requires a ±18mV change into the Thevenin network implying ±30μA currents. A 5K Ohm potentiometer from +V_{REF} (1.22V) to ground can be used with a 20K Ohm resistor from wiper to offset pin to provide ±30μA into 0.6 Volts for a 30mV offset adjust range when in bipolar mode. This loads the +V_{REF} by only 0.25mA while using a resistor ratio for better temperature stability. If the range at the potentiometer

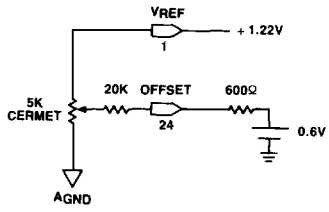

Figure 3. Bipolar Mode — External Offset Adjustment

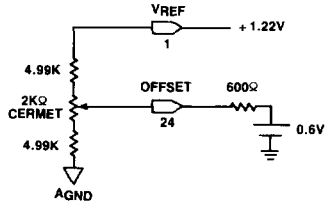

Figure 4. Bipolar Mode — Stable External Offset Adjustment

wiper was limited to ±20mV by pad resistors at each end, the 10K series resistor can be eliminated entirely for true ratiometric operation (see Figures 3 & 4).

The HS 1068 has been laser trimmed under typical conditions for a quantization range of 0.992 Volts p-p. In unipolar mode, for example, input voltages below +2mV output code "0" and input voltages above +0.994 Volts output code "255". System gain may be recalibrated at the converter by use of the range adjust pin. The recommended adjustment range should not exceed ± 10%. In practice, power dissipation considerations make it more practical to use this pin solely for gain increases, as this tends to reduce the power dissipated in the flash resistor ladder. Gain reduction can be accomplished over a wide range by use of resistor padding at the input.

The Thevenin model of the range adjust pin is 933 Ohms to +1.035V nominal. This point drives an inverting gain of two amplifier which supplies the −2.07V reference (at up to 40 mA) to the bottom of the flash resistor ladder. Thus converter gain is adjusted by directly adjusting the full scale range of the flash itself. A gain increase of 10% can be obtained by loading down the voltage at the range adjust pin by 10%. A simple 1 to 10% gain increase control could consist of a 8.6k Ohm resistor in series with a 100k rheostat-connected trimpot to ground (Figure 5). This adjustment rapidly becomes less sensitive as the rheostat approaches zero Ohms. A more elegant approach is shown in Figure 6.

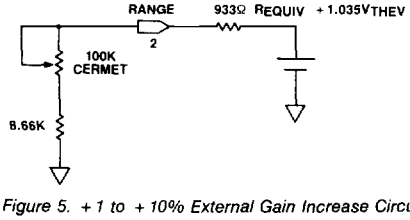

Figure 5. +1 to +10% External Gain Increase Circuit

A negatively offset input range is available for an input range of −1.0V to zero volts. This can be accomplished by tying the REF OUT pin to the OFFSET ADJ pin.

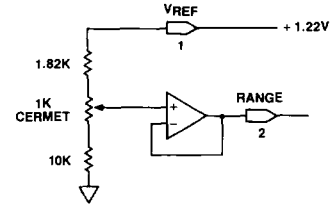

Figure 6. +8% to −1% External Gain Adjust Circuit

NAME	FUNCTION	VALUE	PIN
Range	Gain Adjustment		2
Offset	Offset Adjustment		24

ZERO AND FULLSCALE FLAGS

The endpoint codes of well behaved converters are of indeterminate width — that is they remain "clipped" for large values of out-of-range input voltage. The zero and fullscale flags are separate TTL signals to indicate that the input voltage is within/outside of the quantization range of the converter. They can be used to flag input protection circuitry when out-of-range values are applied, or as start or stop flags to begin processes after input-value conditions are met. They are gated from data within the pipeline of the converter, so that generally they will be valid before the data is valid. This allows an external decision to be made based on these flags before the data enters the rest of the user's system.

When the flash converter is running in the binary mode (and assuming unipolar offsets) the zero scale flag will detect the presence of zero or less than zero Volts at the input to the HS 1068 (all zeroes on the internal data bus). Similarly the fullscale flag corresponds to voltages of 0.994 Volts or greater at the input in binary mode (all ones on the internal data bus). When the flash converter is run in any of its other three possible coding formats, the meanings of these flags will change accordingly. The first one to consider is complementary binary (NMINV, NLIMV = low). In this mode the flags' meanings are interchanged. "Zeroscale" becomes active (high) at 0.994 Volts or greater and "Fullscale" becomes active (low) with inputs more negative than 2mV.

Note that "Fullscale" is an LSTTL output, while the "Zeroscale" is an LSTTL open collector gate with an internal 1.1KΩ pull up resistor.

A_{OUT}

The A_{OUT} pin is primarily used as a testpoint in calibrating the HS 1068. It supplies an inverted gain of two version of the input signal, exhibiting the offsetting necessary for unipolar or bipolar operation. A 470 Ohm isolation resistor protects the internal amplifier from ground shorts. Note that a −50mV nominal offset will be found here even in unipolar mode. It is added in at the input amplifier to compensate for offsets in the flash resistor ladder. This output can be buffered, even into a virtual ground, with minimal effect on the digitized signal.

Input Voltage Range										
Z_{IN}	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	open	499	1k	750	332	806	249	909	110

Table 1. Input Resistor Selection Table (Values in Ohms)

Input Voltage Code Center In Unipolar Mode	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV-1 NLINV-1	0 0	0 1	1 0
0.0000	00000000	11111111	10000000	01111111
+0.0039	00000001	11111110	10000001	01111110
*	*	*	*	*
*	*	*	*	*
*	*	*	*	*
+0.4960	01111111	10000000	11111111	00000000
+0.5000	10000000	01111111	00000000	11111111
*	*	*	*	*
*	*	*	*	*
*	*	*	*	*
+0.9920	11111110	00000001	01111110	10000001
+0.9960	11111111	00000000	01111111	10000000

Table 2. Output Coding Table[1]

Note: 1. Input voltages are at code centers and buffer amplifier offset voltage is nulled.

TIMING DIAGRAMS

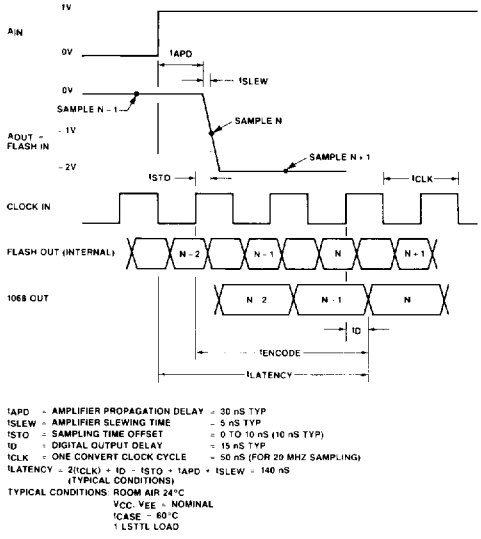

Figure 7. Output Data Timing Diagram

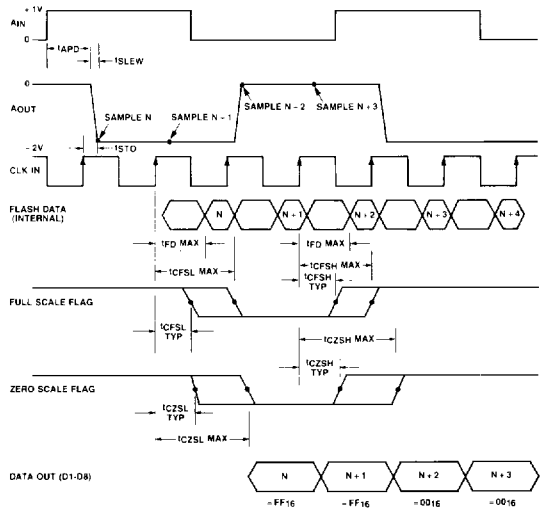

Figure 8. Zero Scale/Full Scale Flags Timing Diagram

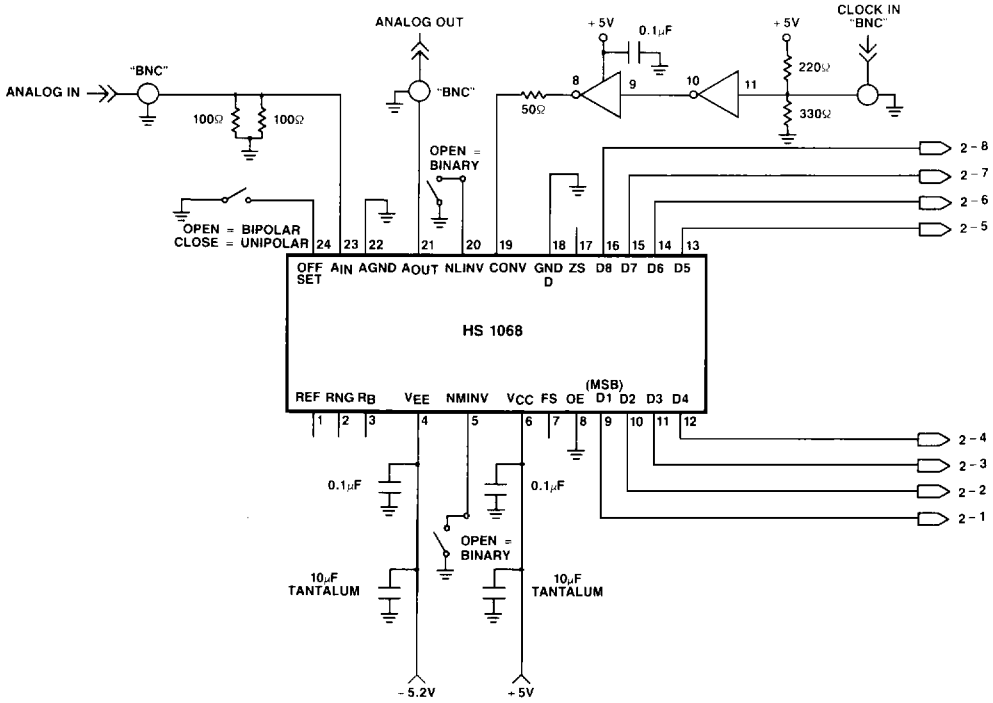

Figure 9. HS 1068 Connection Diagram

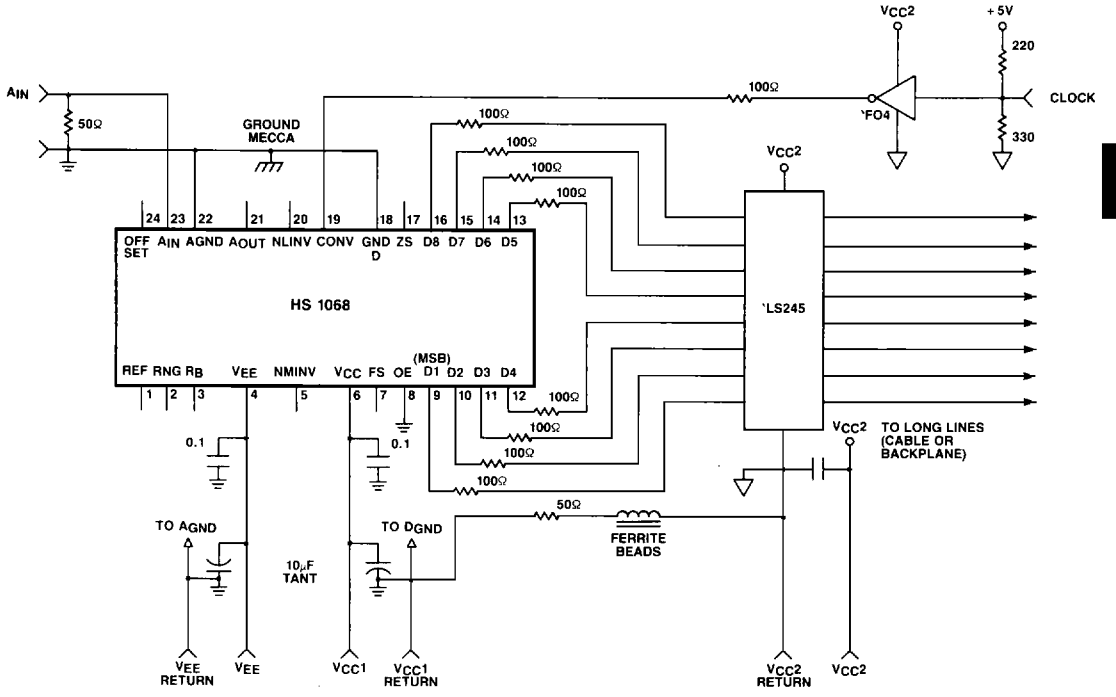

Figure 10. Isolating Digital Ground Noise From Converter Using RL Isolation at Digital Grounds (100Ω Resistors Used to Series Terminate Long Runs)

DYNAMIC TESTING OF THE HS 1068

The HS 1068 has been designed to minimize the dynamic distortions normally found in high speed digitizers. Its excellent dynamic performance is due to the low aperture jitter in the flash converter and the wide gain-bandwidth of the input amplifier. Dynamic distortion tests can be compared to the Total Harmonic Distortion, Noise and Intermodulation Distortion measurements usually made on audio information-carrying channels.

The dynamic tests done at Hybrid Systems utilize a low distortion oscillator, passive filters to insure signal purity, a 20-25 MS/sec fifo buffer and a computer. A flat-topped pulse generator is also used, without filtering, to measure settling times.

The SNR test is the primary measurement of signal fidelity. As performed at Hybrid, the test sequence involves running the converter under typical still room air conditions at 20 MS/s and grabbing a buffer of 4k points length. The data is multiplied by a Von Hann window, then a 4k point FFT is computed. The resulting spectrum is very carefully measured. The fundamental frequency is first identified, then the rms "Voltage" of the entire window-smeared fundamental section of the spectrum is computed. This section of the spectrum is then "notched out" by manually setting these frequency bins to zero. The rms sum of the rest of the spectrum is then computed and is designated the "noise". Note that any distortions or spurious signals (i.e. oscillations or power supply beats etc.) will be included as "noise". A linear spectrum approximating the Fourier Integral is the result of an FFT. Any non-harmonic component in the data will faithfully be reproduced, without the ambiguity associated with a Fourier Series expansion, which assumes a signal may be completely described by its harmonics.

Sampling theory can be used to derive the SNR of an ideal converter, one whose only error is due to the quantization of the numbers describing each point. The result is the well known formula:

SNR (rms sig to rms "noise") = 6.02 x N + 1.76 dB

where N = number of bits in quantized number

In this formula the 1.76 dB applies for all practical cases where the quantization noise will be uncorrelated (white) with respect to the input signal. (This number approaches zero as the input signal approaches DC compared to the sampling frequency — in so-called "coarse quantization").

Figure 11 shows the excellent agreement between theory and the SNR algorithm when ideal computer-generated data is measured. Remember that 49.92 dB SNR is the ideal number for an 8 bit converter with no linearity errors and is due to the quantization noise alone. If a converter were to exhibit ½ LSB of linearity errors, its SNR would be expected to show 3 dB less SNR. At 1 LSB of linearity error, 6 dB less SNR is expected. The HS 1068 under typical conditions exhibits ½ LSB linearity at up to 1.1 MHz (Figure 12) inputs and is still showing 1 LSB error at 4.0 MHz fullscale inputs. For less than fullscale input levels or when cooled, the HS 1068 can exhibit lower total linearity errors.

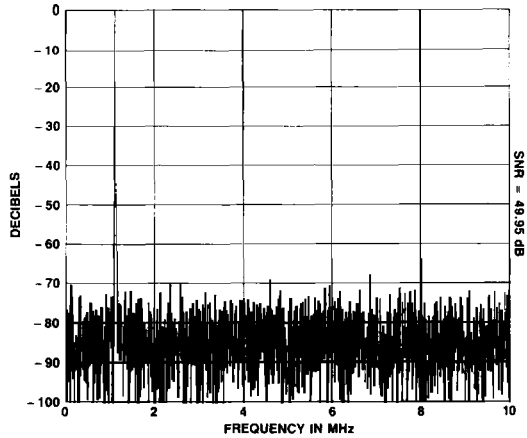

Figure 11. FFT of Ideal 8-Bit Converter

The SNR vs. Input Level graph (Figure 14) points out one of the design compromises at the input buffer. Fullscale high frequency signals generate some (up to 1.25%) harmonic distortion when the buffer is internally compensated for settling time optimization.

The converter power bandwidth is defined separately from the −3 dB frequency of the input amplifier. Power bandwidth here means the frequency at which a full scale input sinewave causes spurious codes. As such it is related to a slew rate, above which the differential delay through the flash comparators can cause a gross encoding error. At room temperature conditions, the power bandwidth is typically 13 MHz, well above the normal Nyquist bandlimit for 20 MS/sec encoding. Spurious codes are detected by measuring the variance in 10 SNR measurements, representing 40,960 samples. A variance of 0.1 dB or more indicates that a spurious code was present. (Some variance will always occur due to the random start points of the sampled sine waves — typically sigma squared equals 0.01 dB or less.)

The beat frequency test is another powerful dynamic test technique, and is used at Hybrid Systems to measure settling times, as well as a graphical tool for "seeing" spurious codes (Figure 15). A stable frequency oscillator is set to a small delta frequency over the sampling rate. The resulting output data "walks through" the input wave with very small time steps. The frequency is picked to produce one full cycle of this beat frequency in one buffer (4k points) of data. Settling times may be measured very accurately because the very low aperture jitter of the flash converter ensures the accuracy of the resulting "walked through" data points.

Histogram testing is a useful tool to evaluate the dynamic differential linearity of a video speed converter. A filtered sine wave is applied to the converter and 10 buffers of 4k points are stored. The number of occurences of each code is then determined, and this histogram is compared with an ideal quantized sine wave of the same gain and offset. The ratio of the real number of occurences to the ideal number of occurences yields an effective code width for each code. The ideal code width (one) is subtracted from this ratio to yield the dynamic differential linearity error as shown in Figures 16 thru 18. The excellent dynamic perfor-

mance of this part shows up as near ideal dynamic differential linearity, even as the input frequency approaches and exceeds the Nyquist bandlimit. Other flash converters must utilize internal grey scale encoders to limit the extent of dynamic differential linearity errors at frequencies as low as one half the Nyquist bandlimit — and still cannot guarantee no missing codes at these frequencies — caveat emptor!

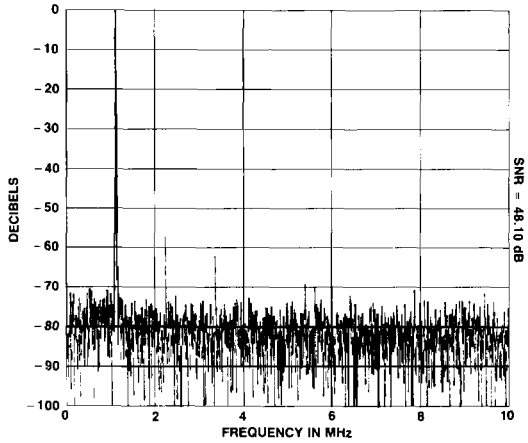

Figure 12. FFT of HS 1068, F_{IN} = 1.123 MHz, F_{SAMPLE} = 20 MHz

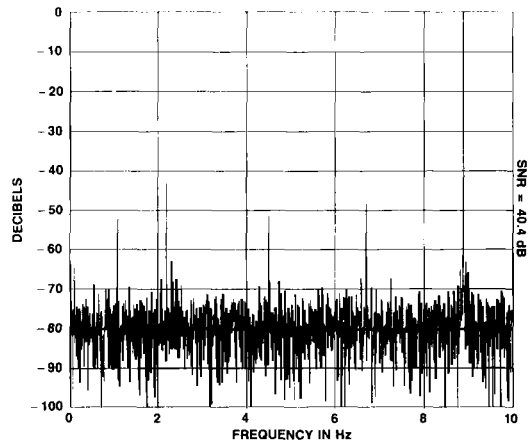

Figure 13. FFT of HS 1068, F_{IN} = 8.9 MHz, F_S = 20 MHz

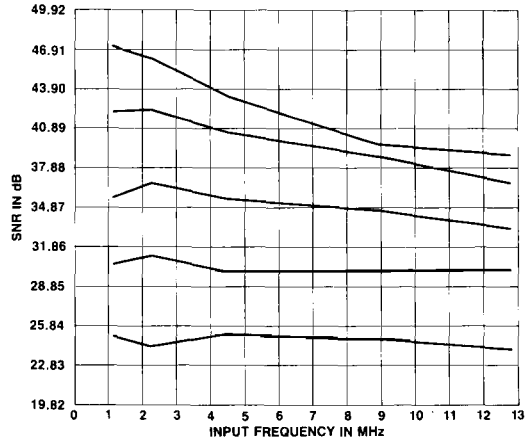

Figure 14. HS 1068 SNR Vs. Frequency Showing 0 to −24 dB Input Levels, F_S = 20 MHz

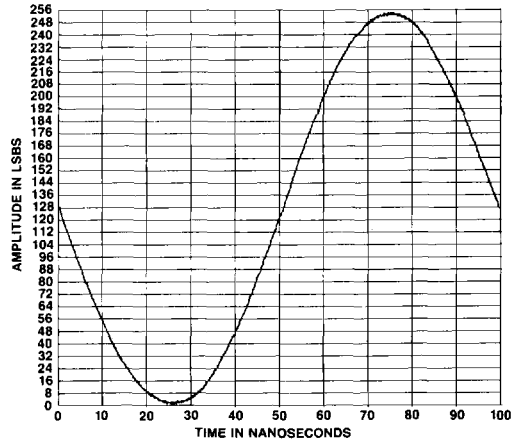

Figure 15. HS 1068 Beat Frequency Test F_{IN} = 10+ MHz, F_S = 20 MHz

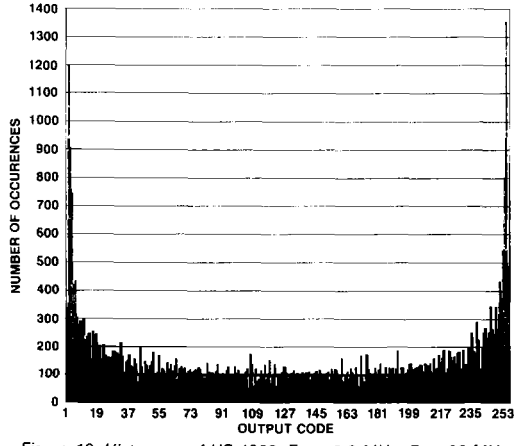

Figure 16. Histogram of HS 1068, F_{IN} = 8.9 MHz, F_S = 20 MHz

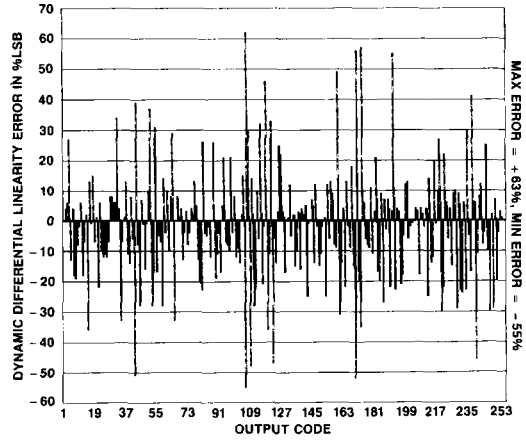

Figure 17. HS 1068 Dynamic Differential Linearity Error, F_{IN} = 8.9 MHz, F_S = 20 MHz

8

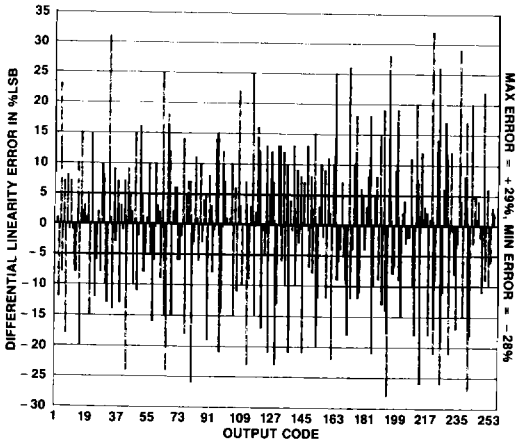

Figure 18. HS 168 Dynamic Differential Linearity Error Low Frequency Input, $F_S = 20$ MHz

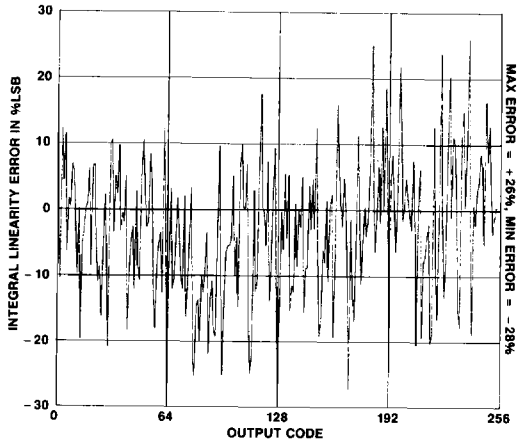

Figure 19. HS 168 Dynamic Integral Linearity Error Low Freuency Input, $F_S = 20$ MHz

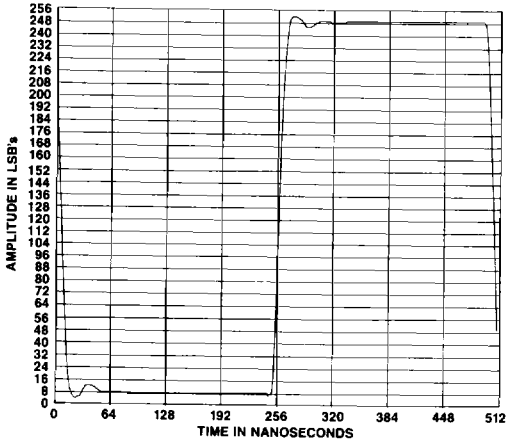

Figure 20. HS 1068 Beat Frequency Input Amplifier Settling Time $F_{IN} = 2+$ MHz, $F_S = 20$ MHz

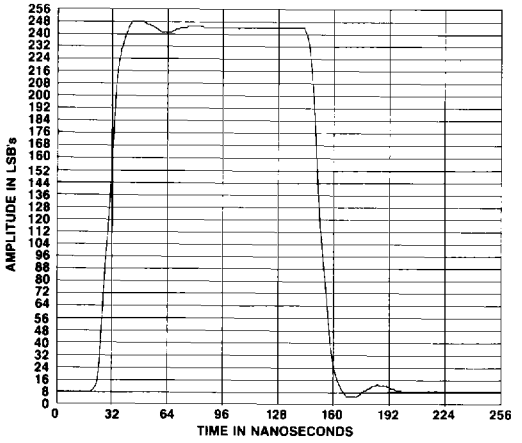

Figure 21. HS 1068 Beat Frequency Input Amplifier Settling Time $F_{IN} = 4+$ MHz, $F_S = 20$ MHz

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 1068C	−0°C to +70°C	8-Bit, 20 MHz ADC
HS 1068B	−55°C to +125°C	8-Bit, 20 MHz ADC, MIL-STD-883C Screening