D2984, JANUARY 1987 · REVISED NOVEMBER 1989

- Each Device Drives 32 Lines
- −120-V P-N-P Open-Collector Parallel Outputs
- High-Speed Serially Shifted Data Inputs
- CMOS-Compatible Inputs
- Strobe and Sustain Inputs Provided
- Serial Data Output for Cascade Operation

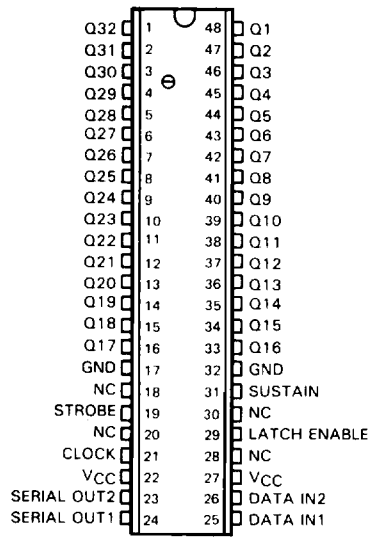
## description

The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed circuit board layout.

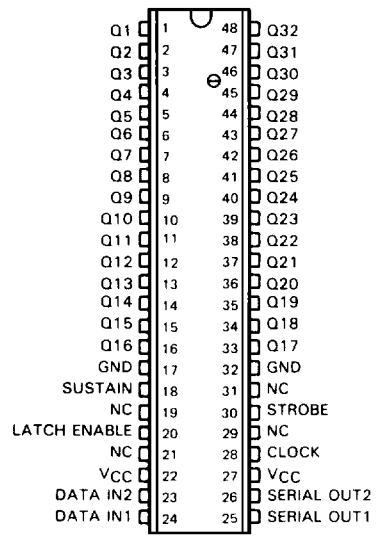
Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 P-N-P open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high will be placed on the data input of the output AND gates. When STROBE is low, and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN will force all outputs to their off state. Drivers may be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.

**SN751508 . . . FT PACKAGE**
**(TOP VIEW)**




**SN751518 . . . FT PACKAGE**
**(TOP VIEW)**




NC—No internal connection





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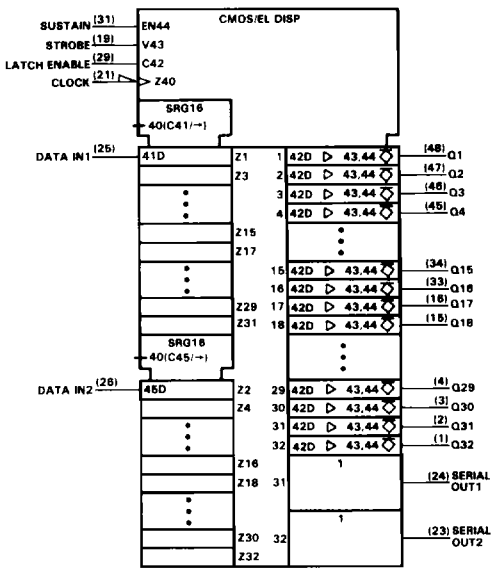
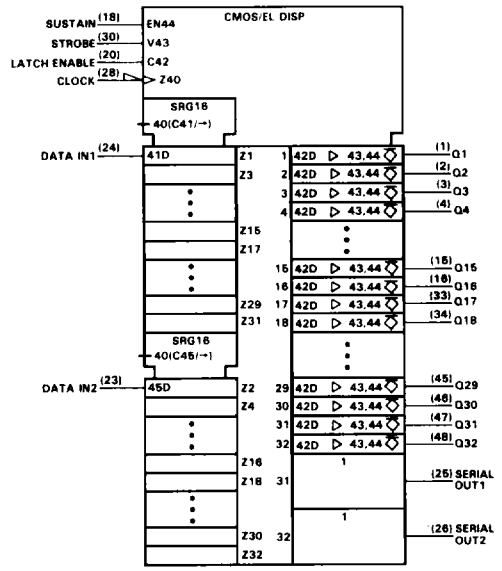
## logic symbols†

SN751508




SN751518




†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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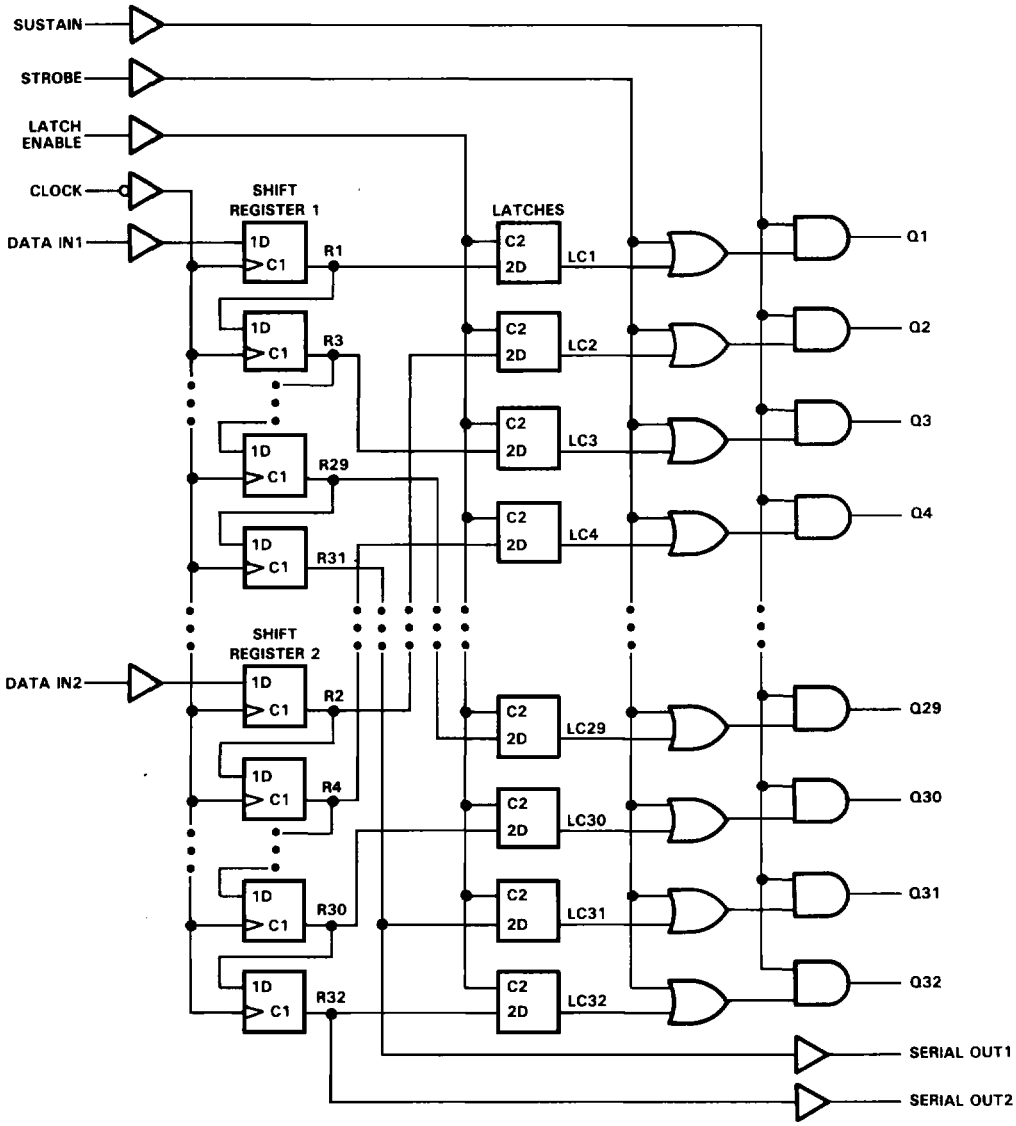
## logic diagram (positive logic)



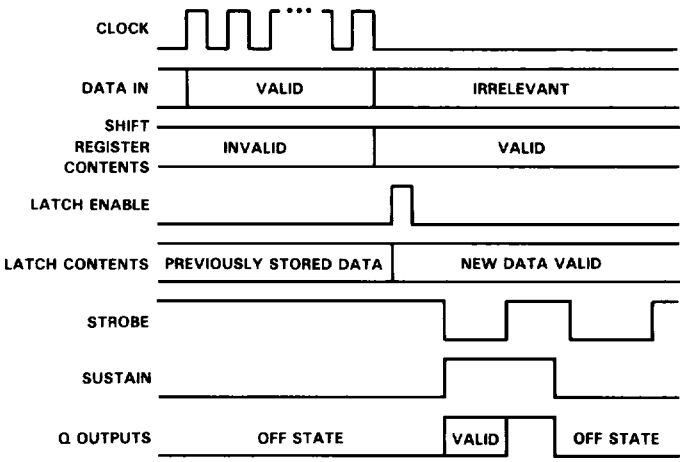
| FUNCTION | CONTROL INPUTS | | | | SHIFT REGISTERS | LATCHES | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| | CLOCK | LATCH ENABLE | STROBE | SUSTAIN | R1 THRU R32 | LC1 THRU LC32 | SERIAL SO1 | SERIAL SO2 | Q1 THRU Q32 |
| LOAD | ↓ | X | X | X | Load and shift† | Determined by | R31 | R32 | Determined by |
| | No ↓ | X | X | X | No change | LATCH ENABLE‡ | | | SUSTAIN and STROBE |
| LATCH ENABLE | X | L | X | X | As determined | Stored data | R31 | R32 | Determined by |
| | X | H | X | X | above | New data | | | SUSTAIN and STROBE |
| STROBE | X | X | L | H | As determined | Determined by | R31 | R32 | LC1 thru LC32 |
| | X | X | H | H | above | LATCH ENABLE‡ | | | All on (high) |
| SUSTAIN | X | X | X | L | As determined above | Determined by LATCH ENABLE‡ | R31 | R32 | All off |

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

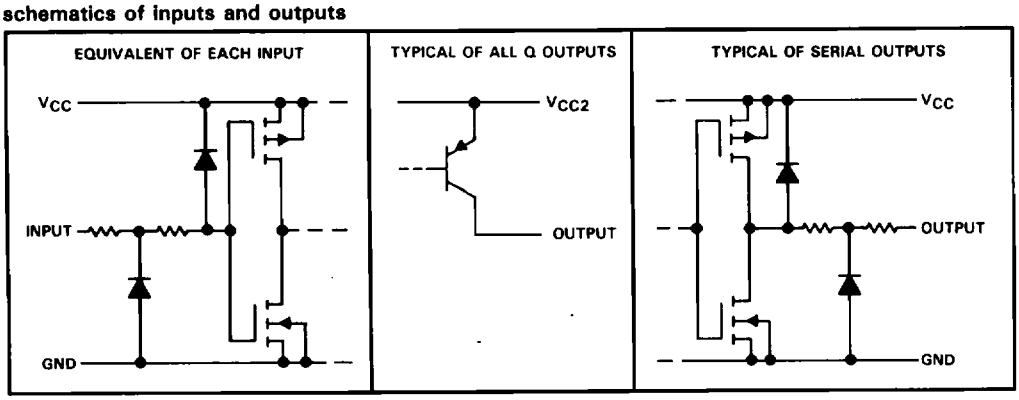
† Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, . . . R4 takes on the state of R2, R2 takes on the state of Data In2, R31 takes on the state of R29, R29 takes on the state of R27, . . . R3 takes on the state of R1, and R1 takes on the state on Data In1.

‡ New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

### typical operating sequence



## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . −0.4 to 7 V
On-state Q output voltage, $V_O$ . . . . . −120 V to $V_{CC}$ + 0.4 V
Input voltage . . . . . −0.4 V to $V_{CC}$ + 0.4 V
Serial output voltage . . . . . −0.4 V to $V_{CC}$ + 0.4 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1025 mW
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltages values are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | | 4.5 | 5 | 5.5 | V |
| Output voltage, $V_O$ | | | | | −75 | V |
| High-level input voltage, $V_{IH}$ | | $V_{CC}$ = 4.5 V | 3.6 | | | V |
| | | $V_{CC}$ = 5.5 V | 4.4 | | | |
| Low-level input voltage, $V_{IL}$ | | $V_{CC}$ = 4.5 V | | | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | | | 1 | |
| Output current, $I_O$ ($T_A$ = 25°C) | | | | | −1.2 | mA |
| Clock frequency, $f_{clock}$ | | | | | 5 | MHz |
| Pulse duration, $t_w$ (see Figure 1) | CLOCK | | 75 | | | ns |
| | DATA IN | | 160 | | | |
| | LATCH ENABLE | | 90 | | | |
| | STROBE | | 2 | | | μs |
| | SUSTAIN | | 2 | | | |
| Setup time, $t_{su}$ (see Figure 1) | DATA IN before CLOCK↓ | | 20 | | | ns |
| | CLOCK low before LATCH ENABLE↑ | | 50 | | | |
| | LATCH ENABLE low before CLOCK↓ | | 0 | | | |
| | LATCH ENABLE high before STROBE↓ | | 0 | | | |
| | LATCH ENABLE high before SUSTAIN↑ | | 0 | | | |
| Hold time, DATA IN after CLOCK↓, $t_h$ (see Figure 1) | | | 50 | | | μs |
| Operating free-air temperature, $T_A$ | | | 0 | | 70 | °C |

## electrical characteristics, $V_{CC}$ = 5 V, $T_A$ = 0°C to 70°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ High-level output voltage | Q outputs | $I_{OH}$ = −0.5 mA | | 4 | 4.5 | | V |
| | Serial Outputs | $V_{CC}$ = 5.5 V | $I_{OH}$ = −100 μA | 4.3 | 4.6 | | |
| | | | $I_{OH}$ = −20 μA | 4.4 | | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −100 μA | 3.4 | 3.6 | | |
| | | | $I_{OH}$ = −20 μA | 3.6 | | | |
| $V_{OL}$ Low-level output voltage | Serial Outputs | $V_{CC}$ = 5.5 V | $I_{OL}$ = 100 μA | | 0.9 | 1.2 | V |
| | | | $I_{OL}$ = 20 μA | | | 1.1 | |
| | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 100 μA | | 0.9 | 1.1 | |
| | | | $I_{OL}$ = 20 μA | | | 0.9 | |
| $I_{OH}$ High-level Q output current | | $T_A$ = 25°C, | $V_O$ = 3 V | −1.2 | | | mA |
| $I_{OL}$ Low-level Q output current | | $T_A$ = 25°C, | $V_O$ = −75 V | | | −500 | μA |
| $I_{IH}$ High-level input current | | $T_A$ = 25°C, | $V_I$ = $V_{CC}$ | | | 1 | μA |
| $I_{IL}$ Low-level input current | | $T_A$ = 25°C, | $V_I$ = 0 | | | −1 | μA |
| $I_{CC}$ Supply current | | All Q outputs high, | $V_{CC}$ = 5.5 V | | 17 | 25 | mA |
| | | All Q outputs low | | | | 3 | |
| $C_i$ Input capacitance | | | | | | 15 | pF |

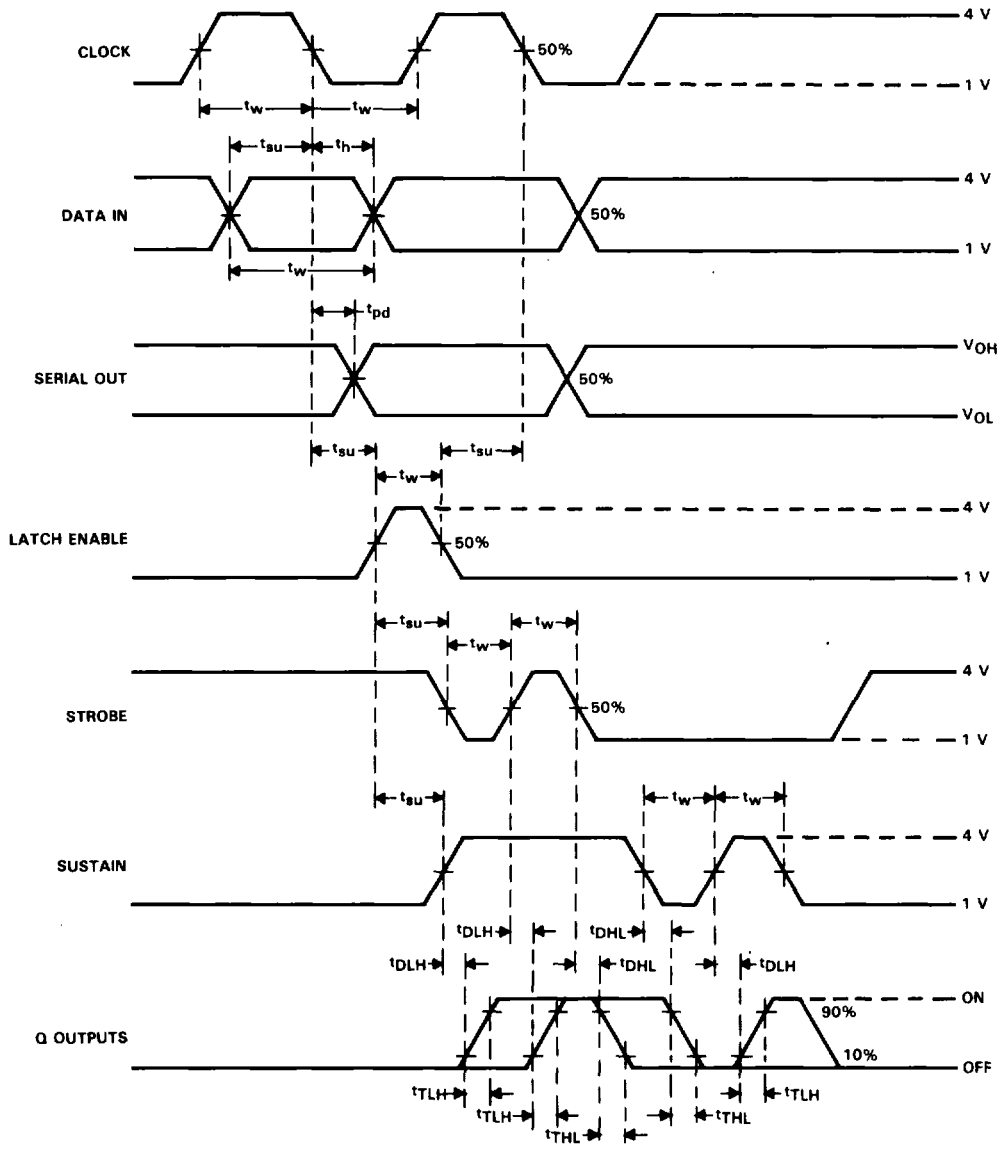
†All typical values are at $T_A$ = 25°C.

## switching characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time, CLOCK to Serial Outputs | $C_L$ = 15 pF | | 100 | 150 | ns |
| $t_{DLH}$ | Delay time, low-to-high-level Q output from SUSTAIN or STROBE | $C_L$ = 15 pF, $R_L$ = 91 kΩ, See Figures 1 and 2 | | 0.3‡ | 1 | μs |
| $t_{DHL}$ | Delay time, high-to-low-level Q output from SUSTAIN or STROBE | | | 1‡ | 2.5 | μs |
| $t_{TLH}$ | Transition time, low-to-high-level Q output | | | 2 | 5 | μs |
| $t_{THL}$ | Transition time, high-to-low-level Q output | | | 11 | 18 | μs |

‡Typical values for delay times are measured from the SUSTAIN input.

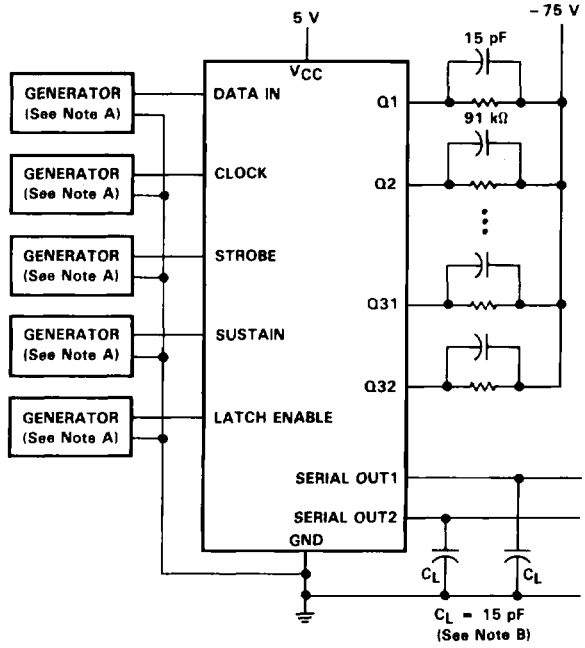
## PARAMETER MEASUREMENT INFORMATION




NOTE: Input $t_r$ and $t_f$ are less than or equal to 10 ns.

**FIGURE 1. INPUT TIMING AND SWITCHING TIME VOLTAGE WAVEFORMS**

## PARAMETER MEASUREMENT INFORMATION




**TEST CIRCUIT**

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_w$ = 100 ns, PRR ≤ 5 MHz, $t_r$ ≤ 10 ns, $t_f$ ≤ 10 ns, $Z_o$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**FIGURE 2**



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## TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

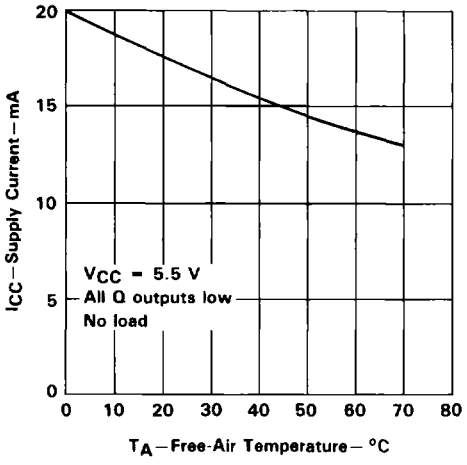


FIGURE 3

DELAY TIME, CLOCK TO SERIAL OUTPUT
vs
FREE-AIR TEMPERATURE

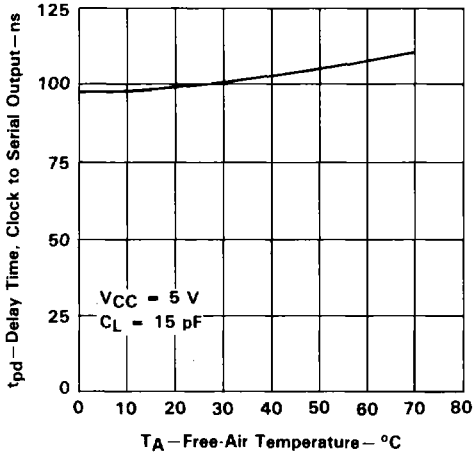


FIGURE 4

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT, LOW TO HIGH
vs
FREE-AIR TEMPERATURE

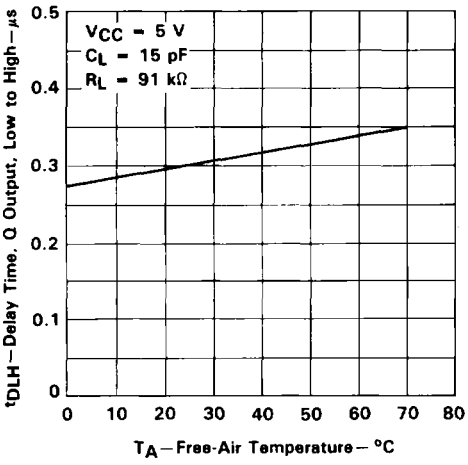


FIGURE 5

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT, HIGH TO LOW
vs
FREE-AIR TEMPERATURE

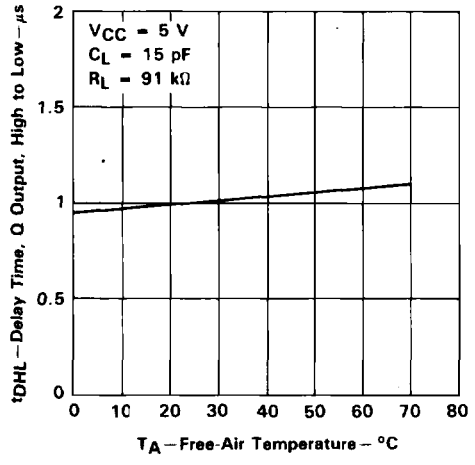


FIGURE 6

## TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT,
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

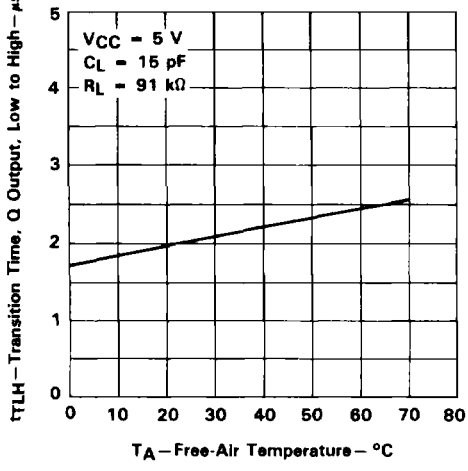


FIGURE 7

TRANSITION TIME, Q OUTPUT,
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

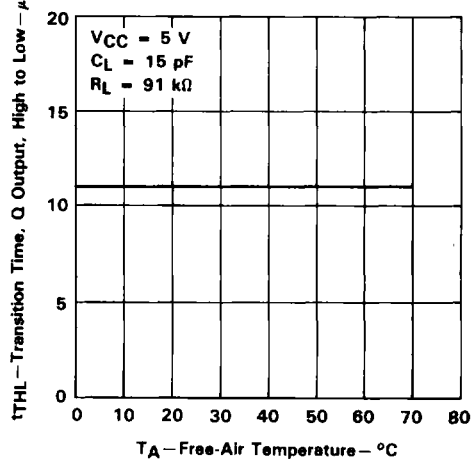


FIGURE 8



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