To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

PRELIMINARY

Notice ; This is not a final specification.
        Some parametric limits are subject to change.

DESCRIPTION

The M61130FP is a semiconductor integrated circuit consisting of Tuner signal processing for NTSC color TV sets and VCRs. The circuit includes Mixer circuit in Tuning system, Oscillator circuit, PLL frequency synthesizer and VIF/SIF, which permits a smaller tuner system.

FEATURES

• VIF/SIF
  Inter carrier type for NTSC
  Coil-less VCO
  Adjustment free AFT
  High-speed IF AGC
• PLL
  Low phase noise and High-speed lock-up
  Built-in band switch driver (4 port)
  I²C bus control
  Available for both XO and external reference
• Mixer/Oscillator
  Built-in U&V oscillator and mixer
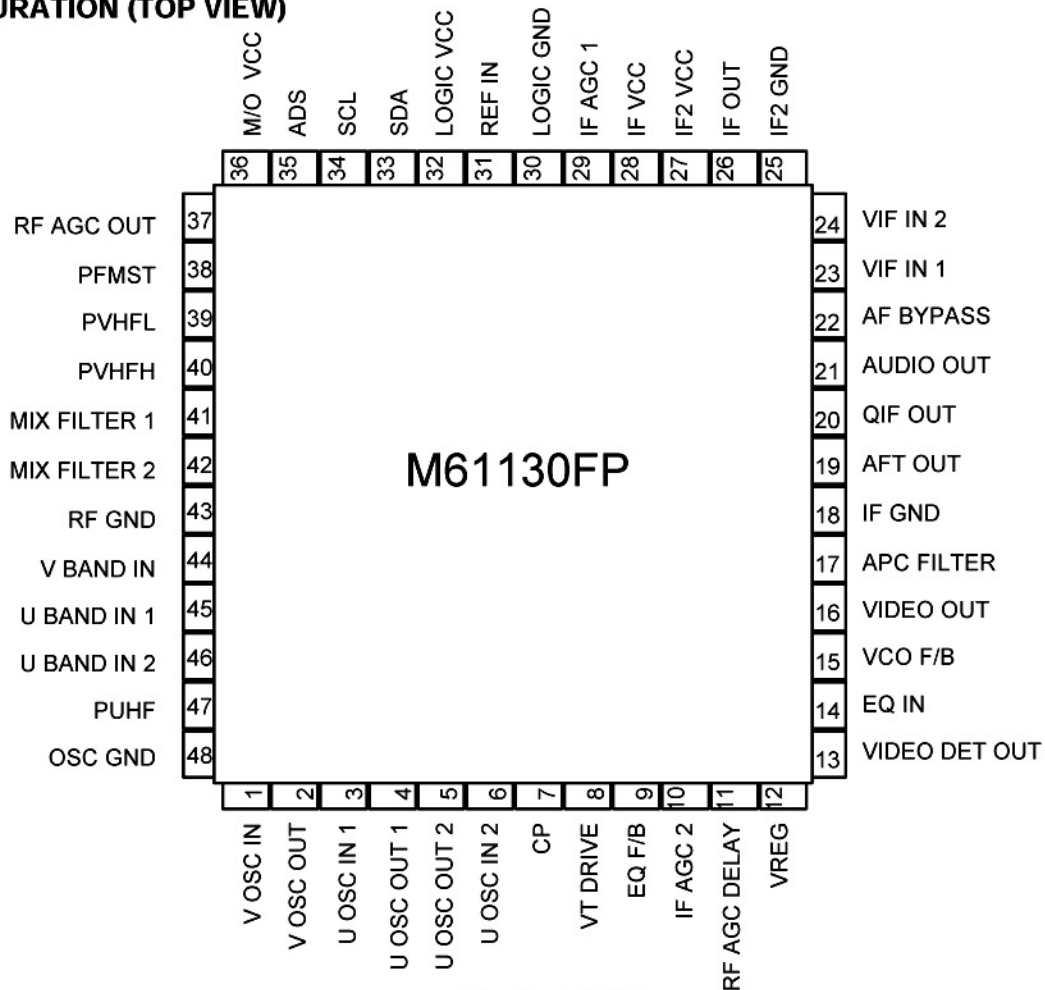 Built-in UV band switch

APPLICATION

TV, VTR

RECOMMENDED OPERATING CONDITIONS

Supply voltage range……………………..4.75 to 5.25V
Recommended supply voltage…………………..5.0V

PIN CONFIGURATION (TOP VIEW)

Top pins (left to right): 36 M/O VCC, 35 ADS, 34 SCL, 33 SDA, 32 LOGIC VCC, 31 REF IN, 30 LOGIC GND, 29 IF AGC 1, 28 IF VCC, 27 IF2 VCC, 26 IF OUT, 25 IF2 GND

Left pins (top to bottom):
37 RF AGC OUT
38 PFMST
39 PVHFL
40 PVHFH
41 MIX FILTER 1
42 MIX FILTER 2
43 RF GND
44 V BAND IN
45 U BAND IN 1
46 U BAND IN 2
47 PUHF
48 OSC GND

Right pins (top to bottom):
24 VIF IN 2
23 VIF IN 1
22 AF BYPASS
21 AUDIO OUT
20 QIF OUT
19 AFT OUT
18 IF GND
17 APC FILTER
16 VIDEO OUT
15 VCO F/B
14 EQ IN
13 VIDEO DET OUT

Center: M61130FP

Bottom pins (left to right):
1 V OSC IN
2 V OSC OUT
3 U OSC IN 1
4 U OSC OUT 1
5 U OSC OUT 2
6 U OSC IN 2
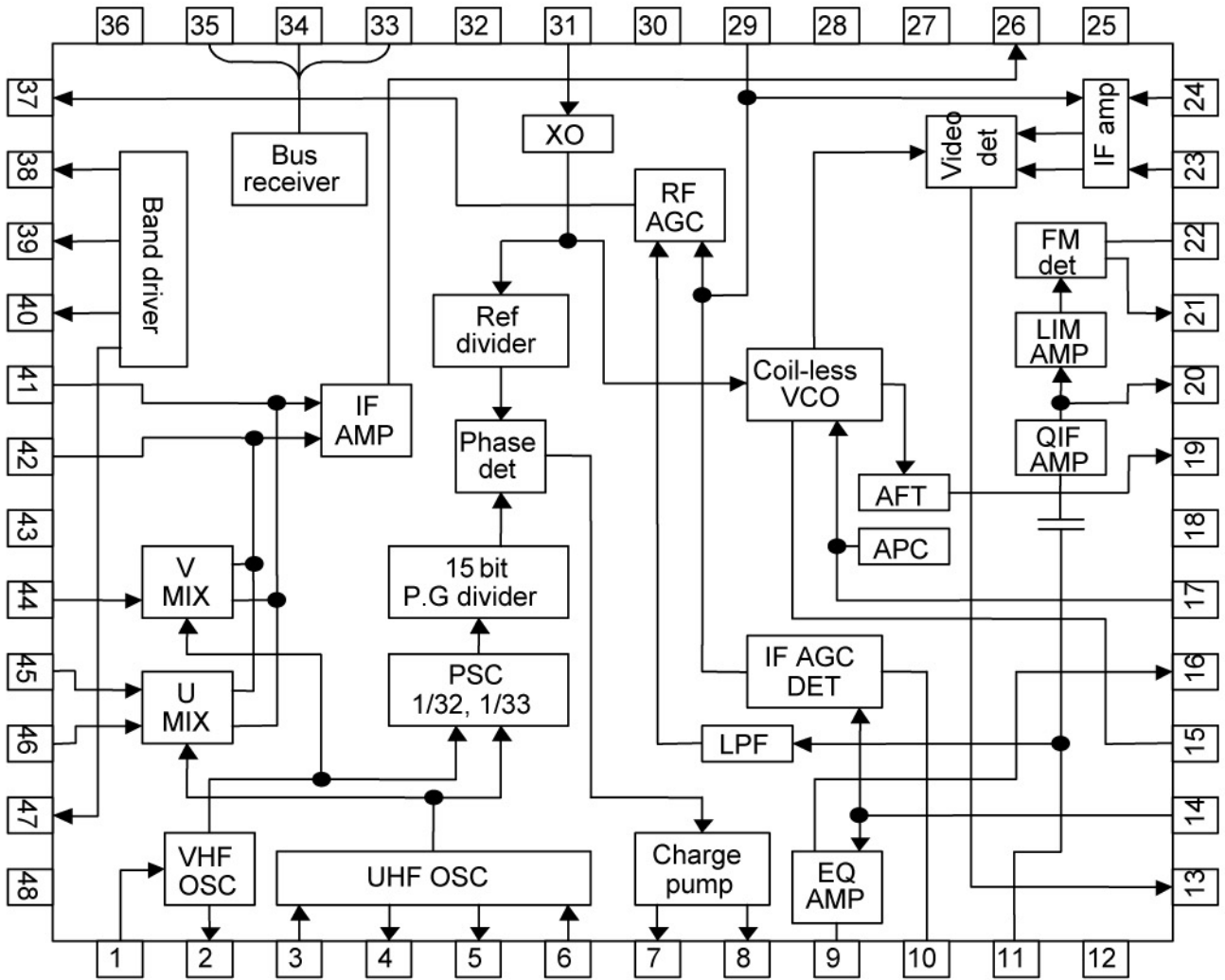7 CP
8 VT DRIVE
9 EQ F/B
10 IF AGC 2
11 RF AGC DELAY
12 VREG

Outline 48P6Q

PRELIMINARY

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BLOCK DIAGRAM
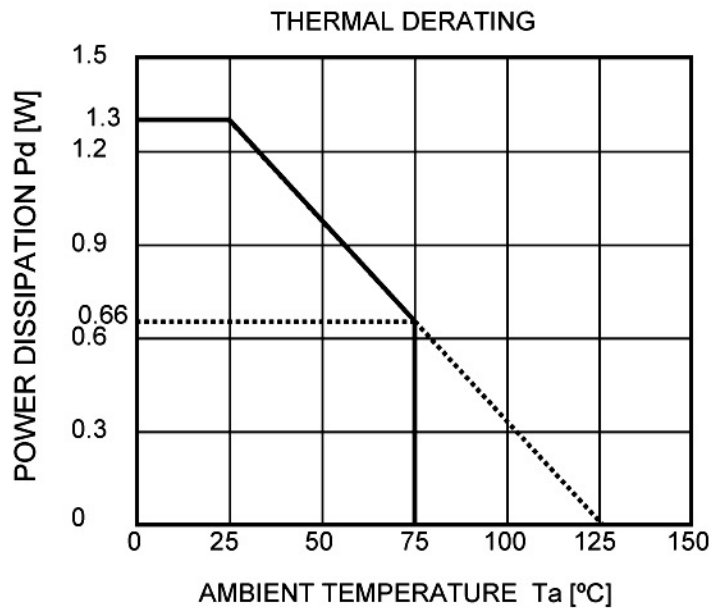
PRELIMINARY

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ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Raitings	Unit
Vcc	Supply Voltage	6.0	V
Pd	Power Dissipation	658	mW
Topr	Operating temperature	-20 to +75	°C
Tstg	Storage temperature	-40 to +150	°C

TYPICAL CHARACTERISTICS

THERMAL DERATING

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Measure Point	Test conditions	Limits			Unit
				Min	Typ	Max	
IF Icc	IF Vcc current	28		-	70	84	mA
MO Icc	M/O Vcc current	36		-	21	25	mA
Log Icc	Logic Vcc current	32	Port output off	-	14	20	mA
Log Icc(U)	Logic Vcc current(UHF)	32	Io_{BS}=-22mA	-	40	46	mA
Log Icc(V)	Logic Vcc current(VHF)	32	Io_{BS}=-25mA	-	43	50	mA
Log Icc(F)	Logic Vcc current(FM(	32	Io_{BS}=-15mA	-	32	38	mA
Ibavideo	Video out bias current	16		1.4	1.9	2.4	mA
IbaAudio	Audio out bias current	21		1.0	1.3	1.6	mA
IbaQIF	4.5MHz QIF out bias current	20		0.9	1.2	1.5	mA
Vreg	Regulator voltage	12		2.65	2.8	2.95	V
fxosc	X'tal frequency	31	PLL function range	3.0	4.0	4.8	MHz
frefin	Ref. signal frequency	31	PLL function range	3.0	4.0	5.0	MHz
Vifrefin	Ref. signal input level	31		50	-	600	mVp-p

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ELECTRICA CHARACTERISTICS (cont.)

M/O

Symbol	Parameter	Measure Point	Test conditions	Limits			Unit
				Min	Typ	Max	
Band VHF Mixer			RL=75Ω				
GpVHF1	Conversion gain1	26,44	fRF=57.5MHz	16	19	22	dB
GpVHF2	Conversion gain2	26,44	fRF=357.5MHz	16	19	22	dB
NFVHF	Noise figure	26,44	fRf=57.5~357.5MHz		11		dB
CM1VHF	1% cross modulation1	26,44	fRF=55.25MHz	90			dB□V
CM2VHF	1% cross modulation2	26,44	fRF=361.25MHz	90			dB□V
Band UHF Mixer			RL=75Ω				
GpUHF1	Conversion gain1	26,45,46	fRF=369.5MHz	26	29	32	dB
GpUHF2	Conversion gain2	26,45,46	fRF=803.5MHz	26	29	32	dB
NFUHF	Noise figure	26,45,46	fRF=369.5~803.5MHz		10		dB
CM1UHF	1% cross modulation1	26,45,46	fRF=367.25MHz	80			dB□V
CM2UHF	1% cross modulation2	26,45,46	fRF=801.25MHz	80			dB□V
Band VHF Oscillator							
foVHF	Operation range	26		101		407	MHz
fosc(v)	Supply voltage drift	26	Vcc=5%		100		KHz
foV(t)	SW ON drift	26	3sec~3min after SW ON		200		KHz
Band UHF Oscillator							
foUHF	Operation range	26		413		847	MHz
fosc(U)	Supply voltage drift	26	Vcc=5%		100		KHz
foU(t)	SW ON drift	26	3sec~3min after SW ON		200		KHz

PLL

Symbol	Parameter	Measure Point	Test conditions	Limits			Unit
				Min	Typ	Max	
Input terminals							
ViH	Hi input voltage	33,34		3.0	-	Vcc +0.3	V
ViL	Lo input voltage	33,34		-	-	1.5	V
IiH1	Hi input current	33,34	Vcc=5.5V,Vi=4.0V	-	-	10	□A
IiL1	Lo input current	33,34	Vcc=5.5V,Vi=0.4V	-	-	-10	□A
SDA output							
VsiL	Lo output voltage	34	Vcc=5.5V,Io=3mA	-	-	0.4	V
IsLK	Leakage current	34	Vcc=5.5V,Vo=5.5V	-	-2	-10	□A
ADS input							
IiH2	Hi input current	35	Vcc=5.5V,Vi=5.0V	-	-	10	□A
IiL2	Lo input current	35	Vcc=5.5V,Vi=1.5V	-	-15	-30	□A
Band output							
VoBS1	Output voltage1	39,40	Vcc=5.0V,Io=-25mA PVHFL,PVHFH	4.6	4.8	-	V
VoBS2	Output voltage2	47	Vcc=5.0V,Io=-22mA,PUHF	4.6	4.8	-	V
VoBS3	Output voltage3	38	Vcc=5.0V,Io=-5mA,PFMST	4.6	4.8	-	V
IoBSLK	Leakage current	38,39,40 47	Vcc=5.5V,Output is OFF	-	-	10	□A
Charge pump							
IcpH	Hi output current	7	Vcc=5.5V,Vo=2.5V,CP=1	160	270	360	□A
IcpL	Lo output current	7	Vcc=5.5V,Vo=2.5V,CP=0	50	70	110	□A
IcpLK	Leakage current	7	Vcc=5.5V,Vo=5.5V,T2,T1=0	-	-	50	nA

PRELIMINARY

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ELECTRICA CHARACTERISTICS (cont.)

VIF/SIF

Symbol	Parameter	Measure Point	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
VoDET	Video output level	16	IF 77.78%, 15.7KHz AM, 90dB□	1.1	1.3	1.5	Vp-p
Vsync	Sync tip voltage	13		1.1	1.3	1.5	V
VSN	Video S/N	13	with 6MHz LPF, 90dB□V	48	50	-	dB
BW	Video out freq. response	16	loss 6MHz	-	3	5	dB
VINMIN	Input sensitivity	13,23,24	-3dB down point		45	49	dB□V
VINMAX	Max. IF input	13,23,24	+3dB up point	101	105	-	dB□V
GR	AGC range	-		54	60	-	dB
V10	IF AGC voltage	10		2.7	2.9	3.1	V
V10L	IF AGC min. voltage	10	110dB□V	1.9	2.1	2.3	V
CL-U	Capture range U	23,24	45.75MHz, 90dB□V	1.5	2.5	-	MHz
CL-L	Capture range L	23,24	45.75MHz, 90dB□V	1.5	1.9	-	MHz
D/G	D/G	13		-	3	5	%
D/P	D/P	13		-	3	5	deg
RINV	VIF input impedance	23,24	DC	-	2k	-	Ω
CINV	VIF input capacitance	23,24	40MHz	-	5	-	pF
foC1	AFT Center freq. 45.75MHz	19,23,24	pin19 voltage = Vcc/2	-30	fo	+30	KHz
foC2	AFT Center freq. 58.75MHz	19,23,24	pin19 voltage = Vcc/2	-30	fo	+30	KHz
V19H	Hi output voltage	19	Vcc=5.0V	4.3	4.7	5.0	V
V19L	Lo output voltage	19		0	0.3	0.7	V
V19C	Center voltage	19	45.75MHz	2.3	2.5	2.7	V
□	Sensitivity	19	360KΩ//360KΩ	10	24	36	mV/KHz
VRFH	RFAGC Hi output voltage	37	open	4.4	4.7	5.0	V
VRFLV	RFAGC Lo output voltage	37	open	0	0.3	0.6	V
RFDLY	RFAGC Delay point	23,24,37	@11pin 2V	87	90	93	dB□V
VoAF	Audio out level	21	4.5MHz±25kHz 1kHz	660	770	880	mVrms
THDAF	Audio out THD	21	4.5MHz±25kHz 1kHz	-	0.2	0.9	%
AFSN	Audio out S/N	21	4.5MHz±25kHz 1kHz	54	57	-	dB
LIM	Limiting sensitivity	11,21		-	50	55	dB□V
AMR	AMR	21		50	55	-	dB
VoQIF	QIF output	20		94	100	-	dB□V

PRELIMINARY

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CONTROL TABLE

VIF frequency select

	VIF frequency	20pin condition
US	45.75 MHz	none
JAPAN	58.75 MHz	pull down (1.5K)

Ref input

Ref in (31pin)	31pin condition
INT	none
EXT	pull down (2K)

BUS CONTROL

1)ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Measure Point	Test conditions	Limits			Unit
				Min	Typ	Max	
fSCL	Clock frequency	33		0	100	400	KHz
tBUF	Bus free time	34		1.3	-	-	□sec
tHDSTA	Data hold time	34		0.6	-	-	□sec
tLOW	SCL LOW hold time	33		1.3	-	-	□sec
tHIGH	SCL HIGH hold time	33		0.6	-	-	□sec
tSUSTA	Set up time	33,34		0.6	-	-	□sec
tHDDAT	Data hold time	33,34		0	-	-	□sec
tSUDAT	Data set up time	33,34		100	-	-	nsec
tR	Rise time	33,34		-	-	300	nsec
tF	Fall time	33,34		-	-	300	nsec
tSUSTO	Set up time	33		0.6	-	-	□sec

Timing Chart 1
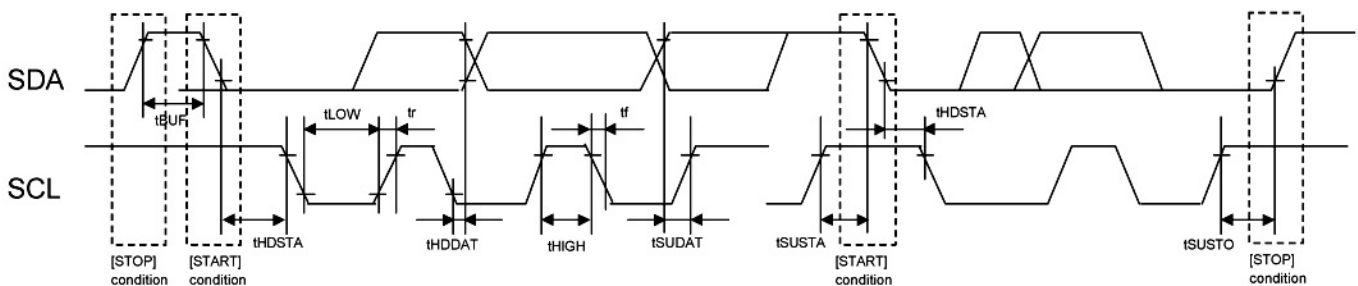
2)Setting Data

The input information consisting of data of 2 or 4 bytes after chip address is received into I²C bus receiver. The definition of bus protocol admitted is shown as below.

Mode_1 STA CA DB1 DB2 CB1 CB2 STO
Mode_2 STA CA CB1 CB2 DB1 DB2 STO
Mode_3 STA CA DB1 DB2 STO
Mode_4 STA CA CB1 CB2 STO

STA : Start condition
STO : Stop condition
CA : Chip address
DB1 : Divider data byte 1
DB2 : Divider data byte 2
CB1 : Control data byte 1
CB2 : Band data byte 2

The information of 5 bytes required for circuit operational chip address, control data and band SW data of 2 bytes and divider data of 2 bytes. After the chip address input, 2 or 4 bytes can be received. Function bit is contained in the first and the third data byte to distinguish between divider and 'control data/band SW data', with "0" going ahead of divider data, and "1" going ahead of control data/band SW data'.

The timing of Writing data for bus protocol Mode is shown in the figure below. Divider data uses 15 bits and is read in at the rise of the eighth clock bit of the second byte divider data (D2).

Control data (CB) and band SW-data (BB) are each read in at the rise of their eighth clock bit.

Timing Chart 2
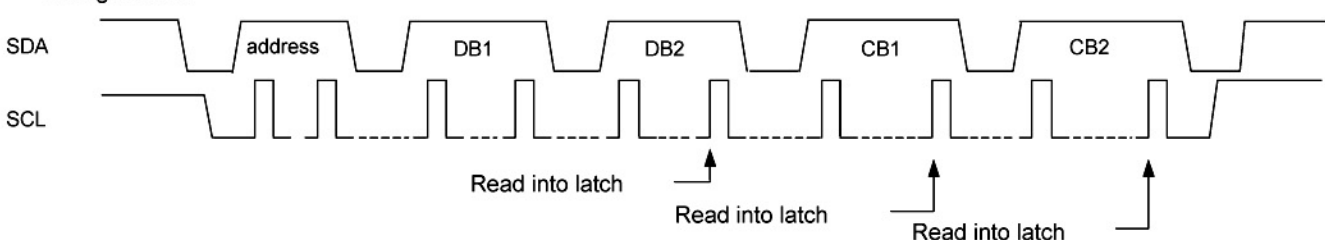
PRELIMINARY

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TUNER SINGLE CHIP

Write mode data format

Byte	MSB							LSB	
Address Byte (CA)	1	1	0	0	0	MA1	MA0	R/W=0	A
Divider Byte1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider Byte2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte (CB1)	1	CP	T2	T1	T0	Rsa	Rsb	OS	A
Band Byte (CB2)	RE	AFT	X	X	PUHF	PFMST	PVHFH	PVHFL	A

MA1,MA0 : Programmable Address Bit

Address input voltage applied to ADS [V]	MA1	MA0
0 to 0.1×Vcc	0	0
Always Valid	0	1
0.4×Vcc to 0.6×Vcc	1	0
0.9×Vcc to Vcc	1	1

N14 to N0 : How to set division ratio of the programmable divider

Division ratio N: $N = N14(2^{14}) + N13(2^{13}) + \cdots + N0(2^{0})$

Range of division ratio N: N=1,024 to 32,767

Frequency of VCO fvco: $fvco = fref \times N$

CP : Set up the charge pump current

CP	Charge pump current
0	70□A
1	270□A

In the case of setting current 270□A, when PLL is locked, charge pump current is automatically switched to CP=O (70□A).

T2,T1,T0 : Set up for test mode

CP	T2	T1	T0	Charge pump	Test output	Test SW	Mode
0	0	0	X	CP switched off	-	OFF	Normal mode
1	0	0	X	CP switched on	-	OFF	Normal mode
X	0	1	X	High impedance	-	OFF	Test mode
0	1	1	0	Sink, CP current "Low"	-	OFF	Test mode
1	1	1	0	Sink, CP current "High"	-	OFF	Test mode
0	1	1	1	Source, CP current "Low"	-	OFF	Test mode
1	1	1	1	Source, CP current "High"	-	OFF	Test mode
0	1	0	0	High impedance	fREF	OFF	Test mode
1	1	0	X	CP switched on	-	ON	Test mode
0	1	0	1	High impedance	f1/N	OFF	Test mode

Note : fREF and f1/N is available on pin PFMST

: Test SW is for the mix filter damping switch

Rsa,Rsb : Set up tuning step

Rsa	Rsb	Division ratio	tuning step frequency	
0	1	1/128	31.25KHz	
1	1	1/64	62.5KHz	
X	0	1/80	50.0KHz	@4MHz X'tal

OS : Set up drive output

OS	Drive output	Mode
0	ON	Normal mode
1	OFF("L")level	Test mode

RENESAS

7

PRELIMINARY

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RE: Select of Reference frequency for automatic adjustment of VIF VCO free-running frequency.

RE	Reference frequency
0	3.58MHz
1	4.00MHz

AFT:Set up AFT mute

AFT	AFT mute voltage
0	Low
1	center

PFMST , PUHF , PVHFL,PVHFH : PORT

FMST,PUHF,PVHFL,PVHF	Output
0	OFF
1	ON

PNP open collector output. When PUHF is "OFF",
Mixer and Oscillator active VHF mode.

Read mode data format

Byte	MSB							LSB	
Address Byte	1	1	0	0	0	MA1	MA0	R/W=1	A
Status Byte	POR	FL	ACPS	X	X	X	X	X	A

X: 0 or 1 Don't care
POR: Power on reset flag. Output is "1" at power-on
FL: Lock detector flag. Output is "1" at locked, output is "0" at unlocked.
ACPS: Automatic charge pump current flag. Output is "0" at charge pump
current automatically switched mode , output is "1" at other mode.

Power on reset
The initial status are shown as below when supply voltage is turned on.
If supply voltage becomes less than about 3.0V, the initial status is set.

Byte	MSB							LSB
Divider Byte1 (DB1)	0	X	X	X	X	X	X	X
Divider Byte2 (DB2)	X	X	X	X	X	X	X	X
Control Byte (CB1)	1	1	0	1	X	1	1	1
Band Byte (CB2)	0	0	X	X	0	0	0	0

PRELIMINARY

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APPLICATION EXAMPLE
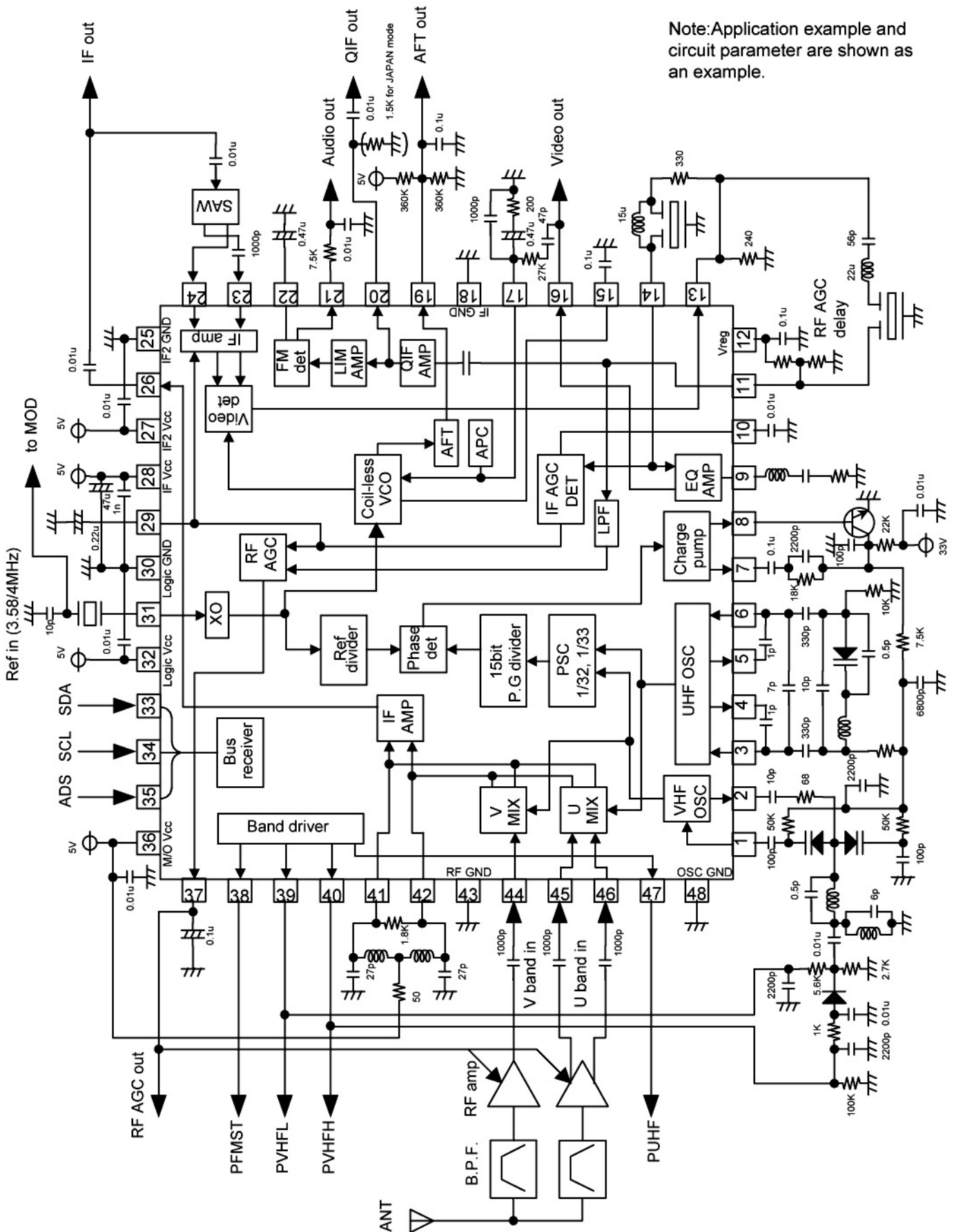
Note:Application example and circuit parameter are shown as an example.

PRELIMINARY
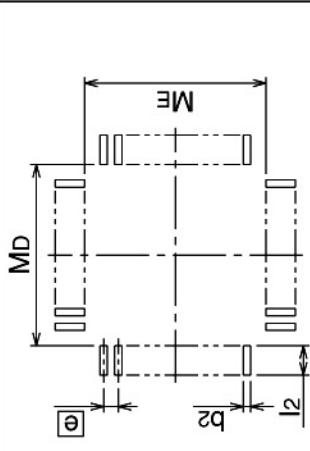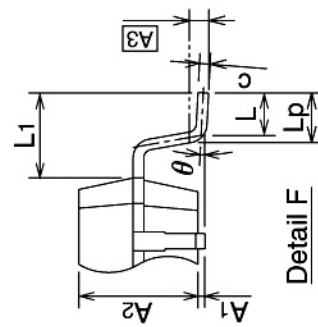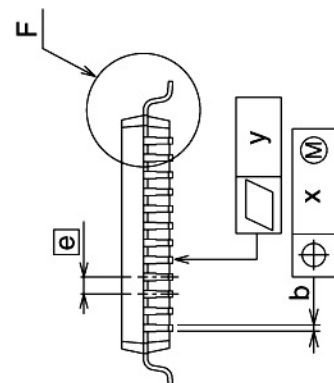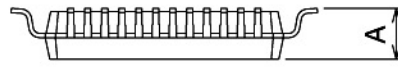
TUNER SINGLE CHIP

DETAILED DIAGRAM OF PACKAGE OUTLINE

Plastic 48pin 7 7mm body LQFP

Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.5	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

48P6Q-A (MMP)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	–	–	Cu Alloy

Detail F

Keep safety first in your circuit designs!

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