128Kx8 MONOLITHIC FLASH

*PRELIMINARY**

FEATURES

- Access Times of 60, 70, 90, 120 and 150nS
- Packaging
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
- 10,000 Erase/Program Cycles
- Sector Erase Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS, 20mA Read Current, Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time.

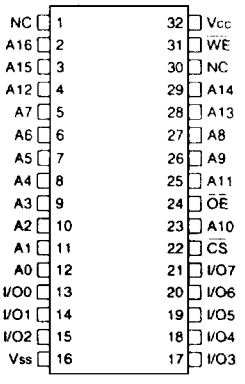
* *This data sheet describes a product under development and is subject to change or cancellation without notice.*

Note: Programming information available upon request.

PIN CONFIGURATION FOR WMF128K8-XXX5

32 DIP
32 CSOJ

TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (Vcc)	-2.0 to +7.0	V
Signal voltage range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention	10 years	
Endurance (write/erase cycles)	10,000 cycles min.	
A9 Voltage for sector protect (VID) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot Vss to -2.0 V for periods of up to 20nS. Maximum DC voltage on output and I/O pins is Vcc + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20nS.
3. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20nS. Maximum Dc input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20nS.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	4.5	5.5	V
Input High Voltage	VIH	2.0	Vcc + 0.3	V
Input Low Voltage	VIL	-0.5	+0.8	V
Operating Temp. (Mil.)	TA	-55	+125	°C
Operating Temp. (Ind.)	TA	-40	+85	°C
A9 Voltage for Sector Protect	VID	11.5	12.5	V

CAPACITANCE

(TA = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	CAD	VI/O = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	COE	VIN = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	CWE	VIN = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	CCS	VIN = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	CI/O	VI/O = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

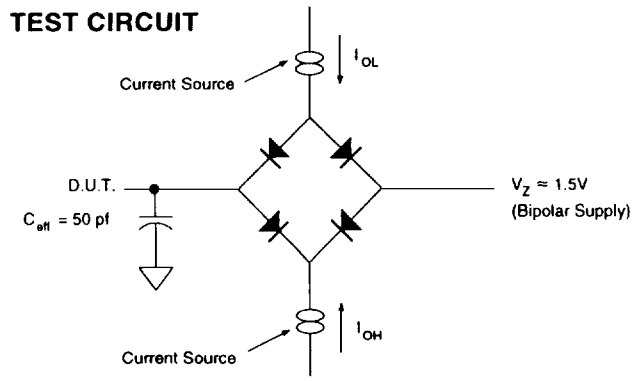
DC CHARACTERISTICS - CMOS COMPATIBLE

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	ILI	Vcc = 5.5, VIN = GND to Vcc		10	µA
Output Leakage Current	ILO	Vcc = 5.5, VIN = GND to Vcc		10	µA
Vcc Active Current for Read (1)	ICC1	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH		35	mA
Vcc Active Current for Program or Erase (2)	ICC2	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH		50	mA
Vcc Standby Current	ICC3	Vcc = 5.5, $\overline{CS}$ = VIH, f = 5MHz		1.6	mA
Output Low Voltage	VOL	IOL =12.0 mA, Vcc = 4.5		0.45	V
Output High Voltage	VOH1	IOH = -2.5 mA, Vcc = 4.5	0.85 x Vcc		V
Output High Voltage	VOH2	IOH = -100 µA, Vcc = 4.5	Vcc - 0.4		V
Low Vcc Lock Out Voltage	VLKO		3.2		V

NOTES:
1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at VIH.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: VIL = 0.3V, VIH = Vcc - 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	VIL = 0, VIH = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	60		70		90		120		150		nS
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		0		nS
Write Enable Pulse Width	t_{WLWH}	t_{WP}	35		35		45		50		50		nS
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		0		nS
Data Setup Time	t_{DVWH}	t_{DS}	30		30		45		50		50		nS
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		nS
Address Hold Time	t_{WLAX}	t_{AH}	45		45		45		50		50		nS
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		0		0		nS
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		nS
Duration of Byte Programming Operation (min)	t_{WHWH1}		14		14		14		14		14		µS
Chip and Sector Erase Time	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	Sec
Read Recovery Time Before Write	t_{GHWL}		0		0		0		0		0		µS
V_{CC} Setup Time		t_{VCS}	50		50		50		50		50		µS
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	Sec
Output Enable Setup Time		t_{OES}	0		0		0		0		0		nS
Output Enable Hold Time (1)		t_{OEH}	10		10		10		10		10		nS

1 For Toggle and $\overline{Data}$ Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	60		70		90		120		150		nS
Address Access Time	t_{AVQV}	t_{ACC}		60		70		90		120		150	nS
Chip Select Access Time	t_{ELQV}	t_{CE}		60		70		90		120		150	nS
$\overline{OE}$ to Output Valid	t_{GLQV}	t_{OE}		30		35		40		50		55	nS
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		25		30		35	nS
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		25		30		35	nS
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		0		0		0		0		nS

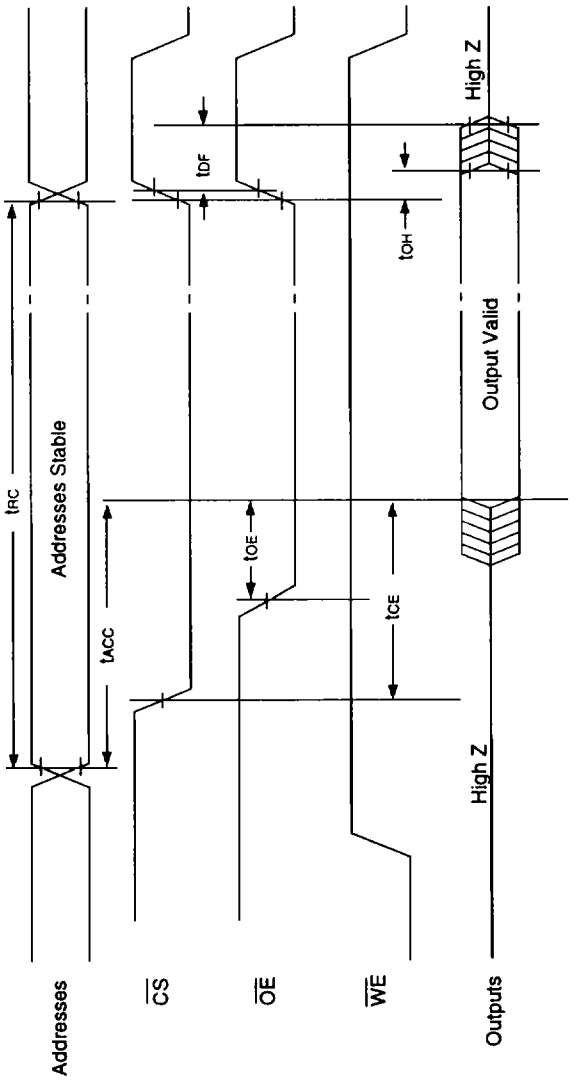
1 Guaranteed by design, not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

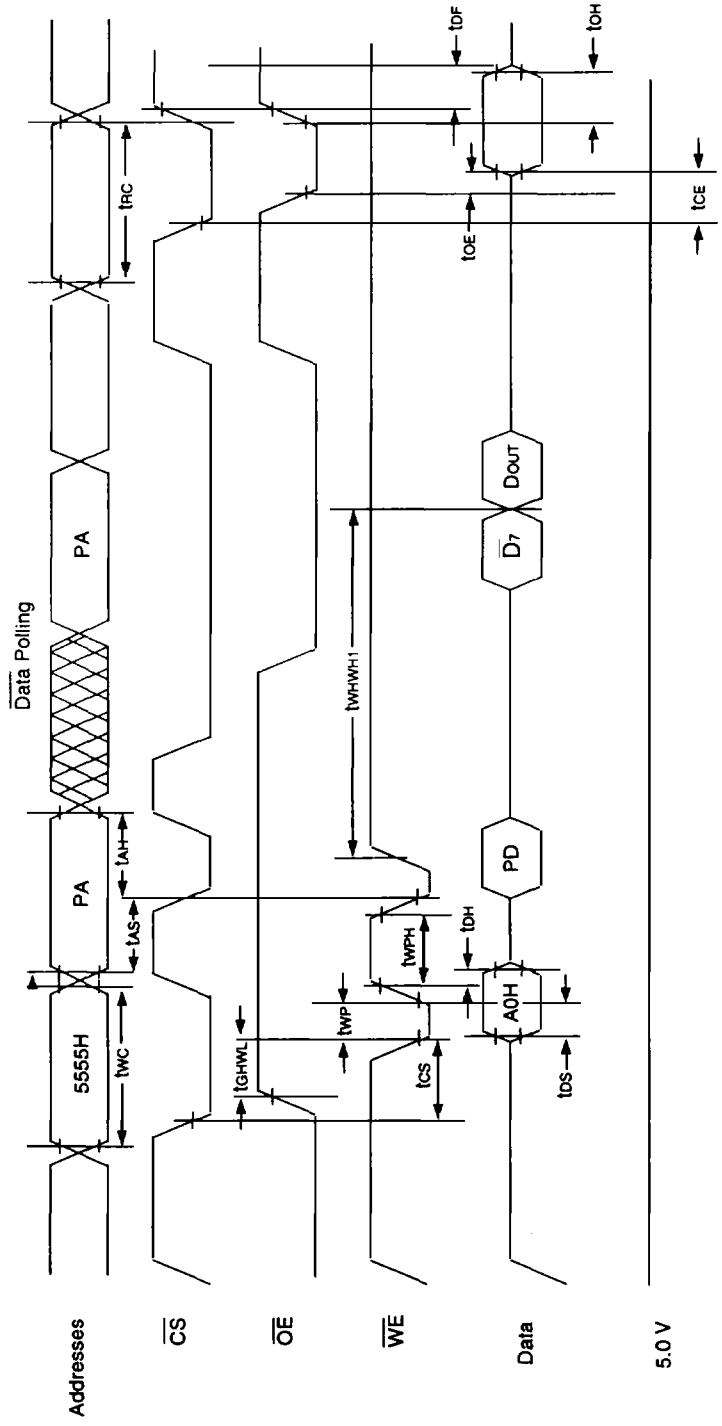
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	60		70		90		120		150		nS
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		nS
$\overline{CS}$ Pulse Width	t_{ELEH}	t_{CP}	30		35		45		50		55		nS
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		nS
Data Setup Time	t_{DVEH}	t_{DS}	30		30		45		50		55		nS
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		nS
Address Hold Time	t_{ELAX}	t_{AH}	45		45		45		50		55		nS
$\overline{WE}$ Hold from $\overline{WE}$ High	t_{EHWH}	t_{WH}	0		0		0		0		0		nS
$\overline{CS}$ Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		nS
Duration of Programming Operation	t_{WHWH1}		14		14		14		14		14		µS
Duration of Erase Operation	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	Sec
Read Recovery before Write	t_{GHEL}		0		0		0		0		0		nS
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	Sec

AC WAVEFORMS FOR READ OPERATIONS

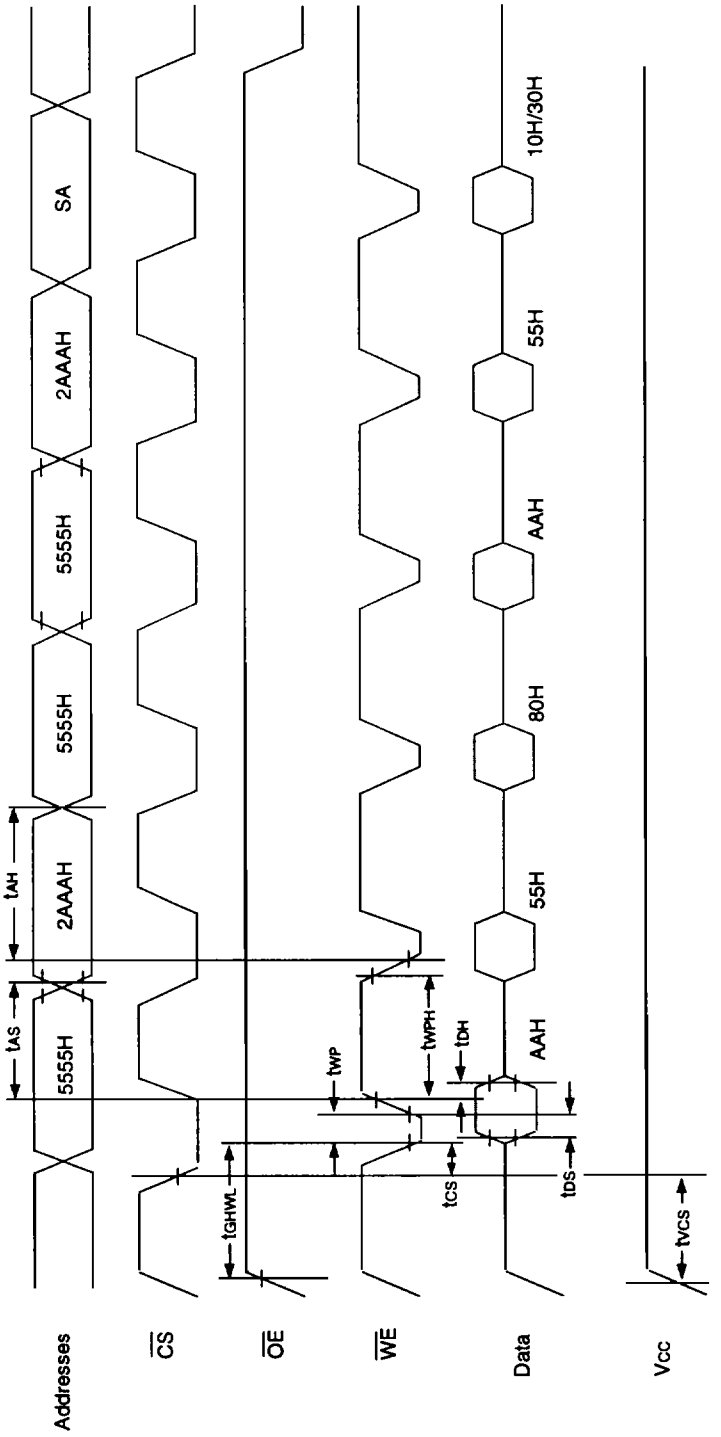


WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



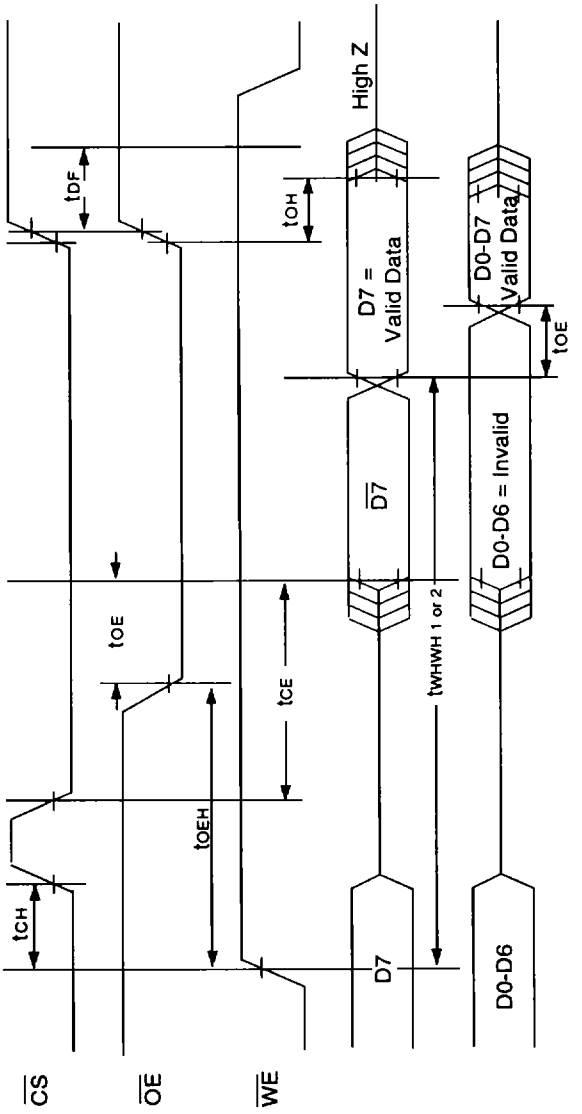
NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

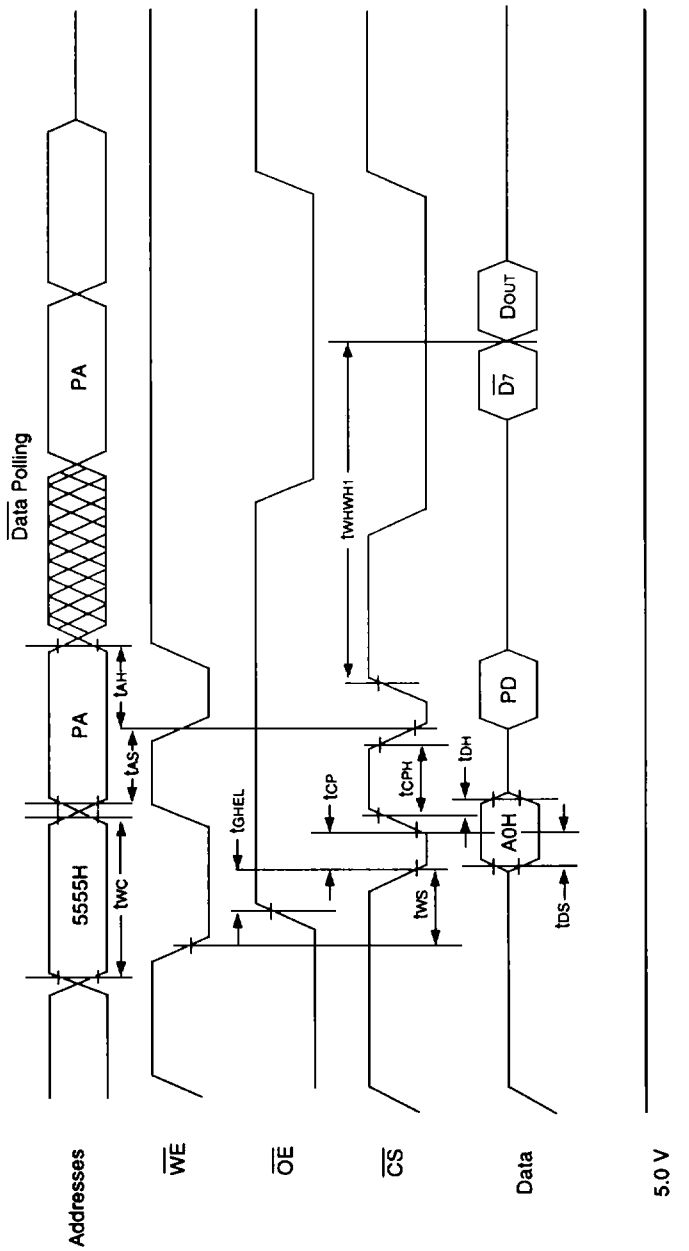


NOTES:
1. SA is the sector address for Sector Erase.

AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

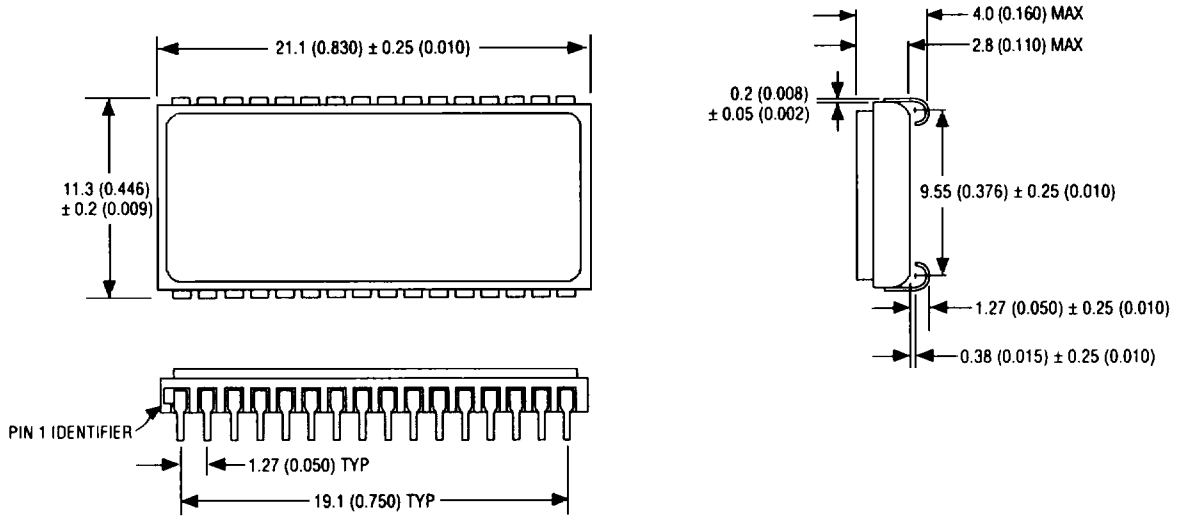


WRITE/ERASE/PROGRAM OPERATION, $\overline{CS}$ CONTROLLED



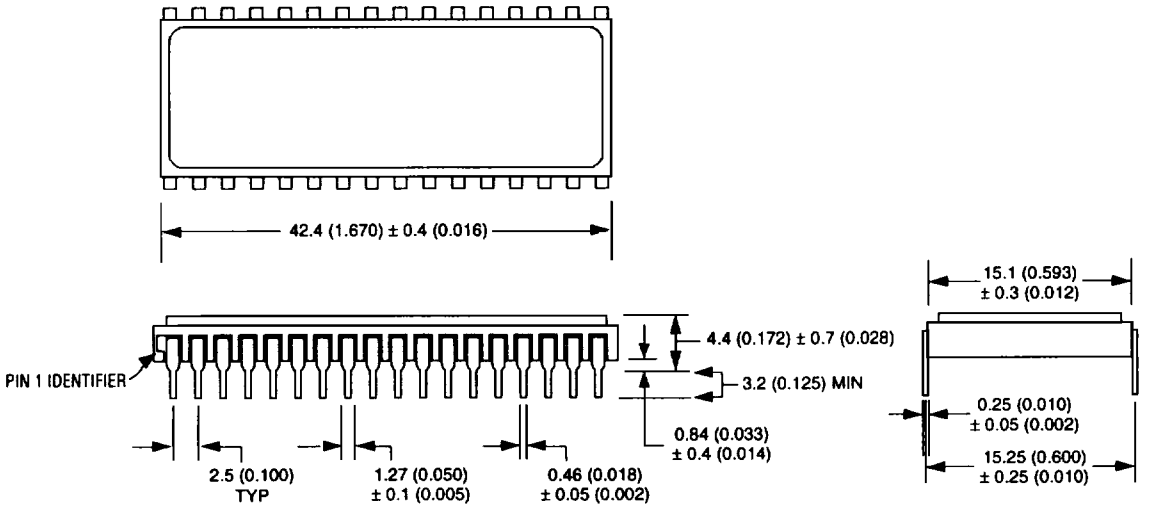
NOTES:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION