



Dear customers,

**About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.**

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", "Oki Electric", and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008  
OKI Semiconductor Co., Ltd.

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# OKI Semiconductor

## MSM54V16258B/BSL

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

### DESCRIPTION

The MSM54V16258B/BSL is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM54V16258B/BSL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM54V16258B/BSL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

### FEATURES

- Single 3.3V power supply,  $\pm 0.3V$  tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 512 cycles/64ms
- Fast page mode with EDO, read modify write capability
- Byte wide control: 2 CAS control
- CAS before RAS refresh, Hidden refresh, RAS only refresh capability
- CAS before RAS self-refresh capability (SL Version.)
- Package : 40-Pin 400 mil plastic SOJ (SOJ40-P-400)

(Product : MSM54V16258B/BSL-xxJS)

44/40-Pin 400 mil plastic TSOP (TSOP44/40-P-400/0.8-K) (Product : MSM54V16258B-xxTS-K)

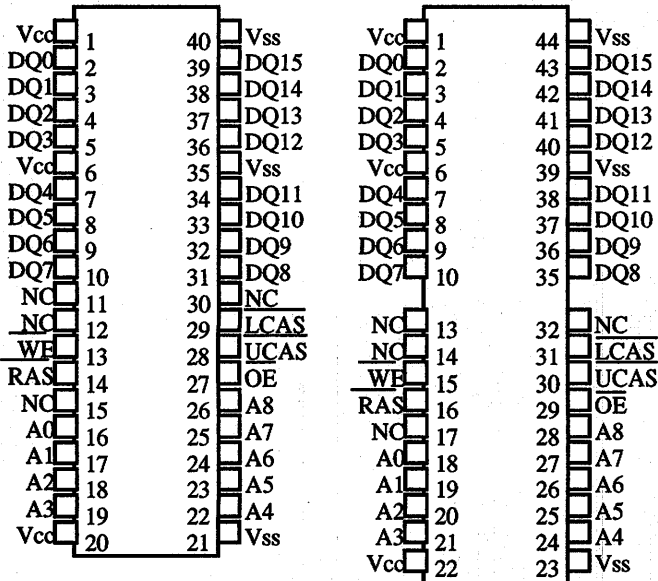
(Product : MSM54V16258BSL-xxTSK)

xx : indicates speed rank.

### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t <sub>TRC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>	t <sub>RC</sub>	t <sub>HPC</sub>	
MSM54V16258B/BSL-40	40ns	22ns	10ns	10ns	80ns	15ns	432mW
MSM54V16258B/BSL-45	45ns	24ns	12ns	12ns	90ns	17ns	396mW
MSM54V16258B/BSL-50	50ns	26ns	12ns	14ns	100ns	20ns	360mW

### PIN CONFIGURATION ( TOP VIEW )



40Pin 400mil SOJ

44/40Pin 400mil TSOP

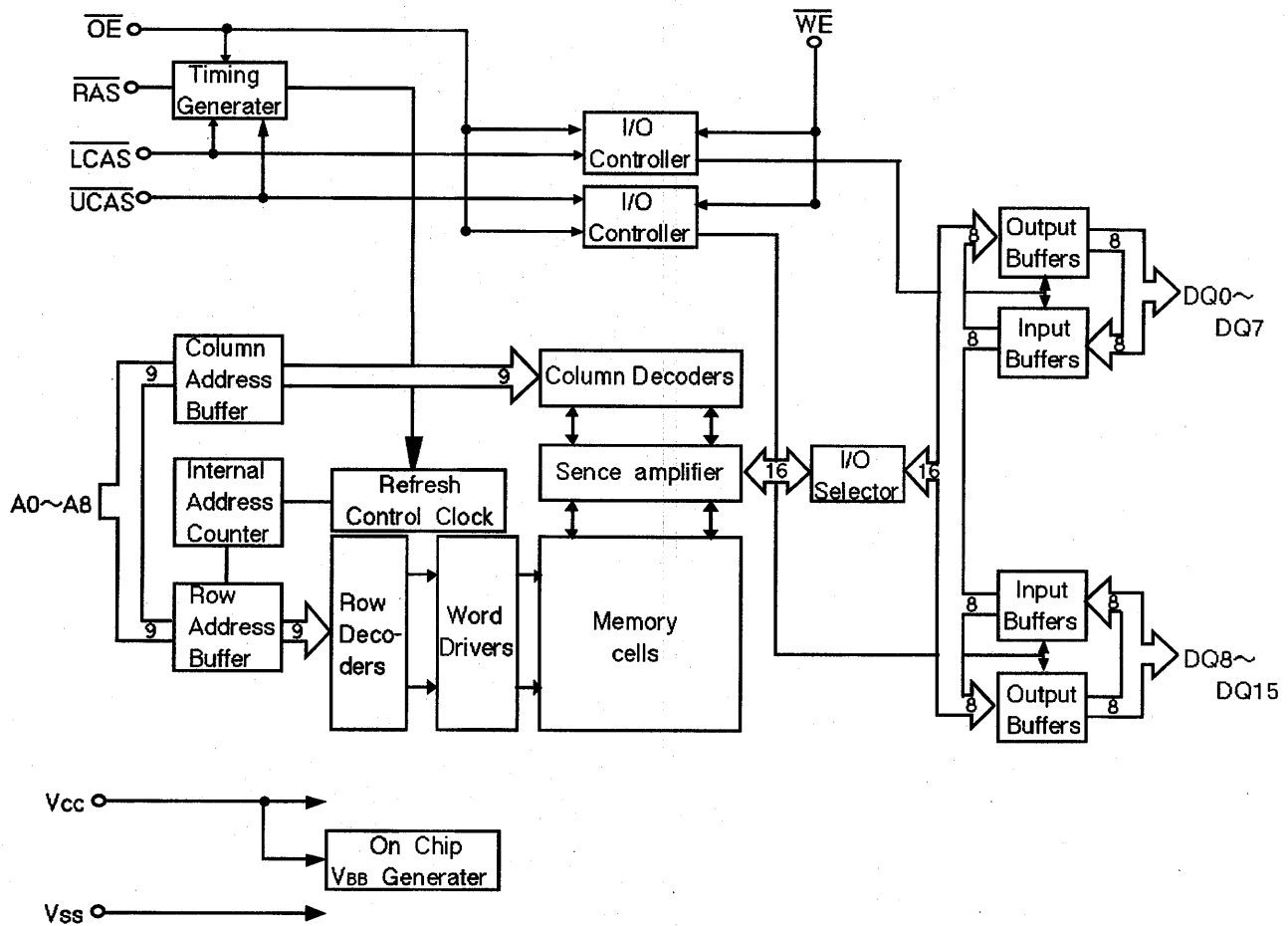
Pin Names	Function
A0-A8	Address Input
RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
WE	Write Enable
OE	Output Enable
Vcc	Power Supply ( 3.3V )
Vss	Ground ( 0V )
NC	No Connection

#### Note 1 :

The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

REVISION-3 1998. 2. 16

## BLOCK DIAGRAM



## FUNCTION TABLE

Input Pin					DQPin		Functional Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	Dout	Upper Byte Read
L	L	L	H	L	Dout	Dout	Word Read
L	L	H	L	H	Din	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	Din	Upper Byte Write
L	L	L	L	H	Din	Din	Word Write
L	L	L	H	H	High-Z	High-Z	—

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25°C	-0.5~+4.6	V
Short circuit output current	Ios	Ta=25°C	50	mA
Power dissipation	Pd	Ta=25°C	1	W
Operating temperature	Topr	—	0~+70	°C
Storage temperature	Tstg	—	-55~+150	°C

### Recommended Operating Conditions

(Ta=0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	3.0	3.3	3.6	V
	Vss	—	0	0	0	V
Input high voltage	Vih	—	2.4	—	Vcc+0.3	V
Input low voltage	Vil	—	-0.3	—	0.8	V

### Capacitance

(Vcc=3.3V±0.3V, Ta=25°C, f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	CIN1	—	—	8	pf
Input capacitance (RAS, LCAS, UCAS, WE, OE)	CIN2	—	—	8	pf
Input / output capacitance (DQ0~DQ15)	CIO	—	—	9	pf

## DC CHARACTERISTICS

( $V_{CC}=3.3V \pm 0.3V$ ,  $T_a=0$  to  $70^\circ C$ )

Parameter	Symbol	Condition	MSM54V16258 B/BSL-40		MSM54V16258 B/BSL-45		MSM54V16258 B/BSL-50		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	$I_{OH} = -1.0mA$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.0mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{II}$	$0V \leq V_{IN} \leq V_{CC}$	-10	10	-10	10	-10	10	$\mu A$	
Output Leakage Current	$I_{LO}$	DQi Disable $0V \leq V_o \leq 5.5V$	-10	10	-10	10	-10	10	$\mu A$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = \text{Min.}$	—	120	—	110	—	100	mA	1,2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{RAS}, \overline{CAS} = V_{IH}$	—	2	—	2	—	2	mA	1
Average Power Supply Current (RAS only Refresh)	$I_{CC3}$	$\overline{RAS} = \text{Cycling}$ $\overline{CAS} = V_{IH}$ $t_{RC} = \text{Min.}$	—	110	—	100	—	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	$I_{CC4}$	$\overline{RAS} = V_{IL}$ $\overline{CAS}$ Cycling $t_{HPC} = \text{Min.}$	—	70	—	65	—	60	mA	1,3
Average Power Supply Current (CAS Before RAS Refresh)	$I_{CC5}$	$\overline{RAS} = \text{Cycling}$ $\overline{CAS}$ Befor $\overline{RAS}$	—	100	—	90	—	80	mA	1,2
Average Power Supply Current (Battery Backup)	$I_{CC6}$	$t_{RC} = 125 \mu s$ $\overline{CAS}$ Befor $\overline{RAS}$ $t_{RAS} \leq 1 \mu s$	—	300	—	300	—	300	$\mu A$	1,2,4,5
Average Power Supply Current (CAS Before RAS Self-Refresh)	$I_{CC5}$	$\overline{RAS} = V_{IL}$ $\overline{CAS} = V_{IL}$	—	300	—	300	—	300	$\mu A$	1,2,4,5

- Notes :
1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for the output open condition
  2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .
  3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .
  4.  $V_{CC} - 0.2V \leq V_{IH} \leq 6.5V$ ,  $-1.0V \leq V_{IL} \leq 0.2V$ .
  5. SL version.

# AC CHARACTERISTICS (1/2)

(V<sub>cc</sub> = 3.3V ± 0.3V, T<sub>a</sub> = 0~70°C)

Parameter	Symbol	MSM54V16258 B/BSL-40		MSM54V16258 B/BSL-45		MSM54V16258 B/BSL-45		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t <sub>RC</sub>	80	—	90	—	100	—	ns	
Read/Write cycle time	t <sub>RMW</sub>	115	—	130	—	145	—	ns	
Fast page mode cycle time	t <sub>HPC</sub>	15	—	17	—	20	—	ns	
Fast page mode read/write cycle time	t <sub>PRMW</sub>	55	—	60	—	65	—	ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	40	—	45	—	50	ns	7,12,13
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	10	—	12	—	14	ns	7,12
Access time from column address	t <sub>AA</sub>	—	22	—	24	—	26	ns	7,13
Access time from $\overline{\text{OE}}$	t <sub>DEA</sub>	—	10	—	12	—	14	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>	—	24	—	26	—	28	ns	7,12
Output low impedance time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	
Data hold after $\overline{\text{CAS}}$ low	t <sub>COH</sub>	3	—	3	—	3	—	ns	17
Output buffer turn-off delay time	t <sub>OFF</sub>	3	8	3	8	3	8	ns	8
Output buffer turn-off delay time from $\overline{\text{OE}}$	t <sub>OEZ</sub>	3	8	3	8	3	8	ns	8
Output buffer turn-off delay time from $\overline{\text{RAS}}$	t <sub>REZ</sub>	3	8	3	8	3	8	ns	8
Output buffer turn-off delay time from $\overline{\text{WE}}$	t <sub>WEZ</sub>	3	8	3	8	3	8	ns	8
Transition time	t <sub>T</sub>	2	35	2	35	2	35	ns	
Refresh period	t <sub>REF</sub>	—	64	—	64	—	64	ms	
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	30	—	35	—	40	—	ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	40	10,000	45	10,000	50	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t <sub>RASP</sub>	40	100,000	45	100,000	50	100,000	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	8	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ hold time reference to $\overline{\text{OE}}$	t <sub>ROH</sub>	8	—	8	—	10	—	ns	
$\overline{\text{CAS}}$ precharge time	t <sub>CP</sub>	5	—	6	—	7	—	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	6	10,000	7	10,000	8	10,000	ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RC<math>\overline{\text{D}}</math></sub>	18	30	18	33	20	38	ns	12
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	13	18	13	21	15	24	ns	
Row address set-up time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	13
Row address hold time	t <sub>RAH</sub>	8	—	8	—	10	—	ns	
Column address set-up time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column address hold time	t <sub>CAH</sub>	5	—	6	—	8	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t <sub>AR</sub>	30	—	30	—	35	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	22	—	24	—	26	—	ns	
Read command set-up time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read command hold time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	9
Read command hold time reference to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	9
$\overline{\text{WE}}$ pulse width	t <sub>WEP</sub>	10	—	10	—	10	—	ns	

## AC CHARACTERISTICS (2/2)

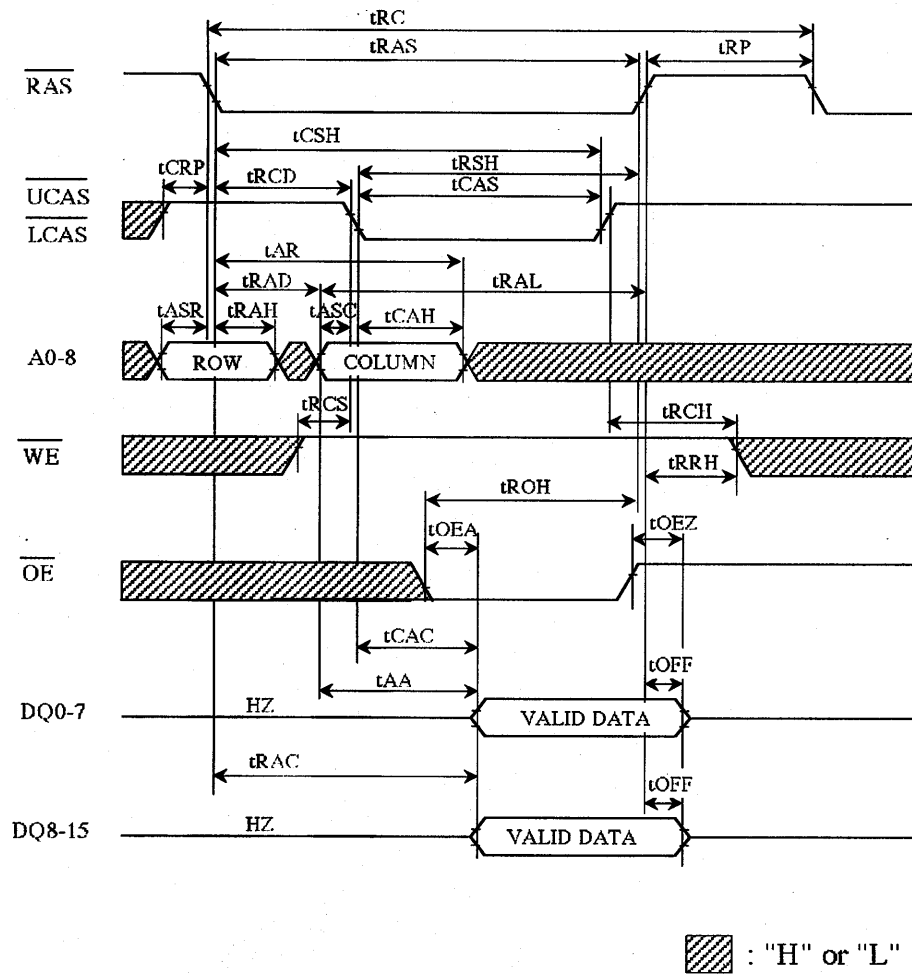
(V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>a</sub> = 0~70°C)

Parameter	Symbol	MSM54V16258 B/BSL-40		MSM54V16258 B/BSL-45		MSM54V16258 B/BSL-50		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write command set-up time	twcs	0	—	0	—	0	—	ns	
Write command hold time	twch	7	—	8	—	9	—	ns	
Write command pulse width	twp	7	—	8	—	9	—	ns	
Write command hold time from $\overline{\text{RAS}}$	twcr	30	—	30	—	35	—	ns	
$\overline{\text{OE}}$ command hold time	toeh	7	—	8	—	9	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	tcwl	7	—	8	—	9	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	trwl	8	—	12	—	14	—	ns	
Data to $\overline{\text{CAS}}$ delay time	tdzc	0	—	0	—	0	—	ns	
Data to $\overline{\text{BE}}/\overline{\text{OE}}$ delay time	tdzo	0	—	0	—	0	—	ns	
Data-in set-up time	tds	0	—	0	—	0	—	ns	10
Data-in hold time	tdh	6	—	7	—	8	—	ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tdhr	30	—	30	—	35	—	ns	
$\overline{\text{OE}}$ to Data delay time	toed	8	—	8	—	8	—	ns	
$\overline{\text{OE}}$ "L" to $\overline{\text{CAS}}$ "H" lead time	toch	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ "H" to $\overline{\text{OE}}$ "L" lead time	tcho	10	—	10	—	10	—	ns	
Hi-Z command pulse width	toep	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	tcwd	28	—	30	—	32	—	ns	11
Column address to $\overline{\text{WE}}$ delay time	tawd	38	—	40	—	44	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	trwd	55	—	60	—	65	—	ns	11
$\overline{\text{CAS}}$ active delay time from $\overline{\text{RAS}}$ precharge	trpc	0	—	0	—	0	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	tcsr	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	tchr	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh)	trass	100	—	100	—	100	—	us	19
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh)	trps	100	—	100	—	100	—	ns	19
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh)	tchs	-40	—	-40	—	-40	—	ns	19

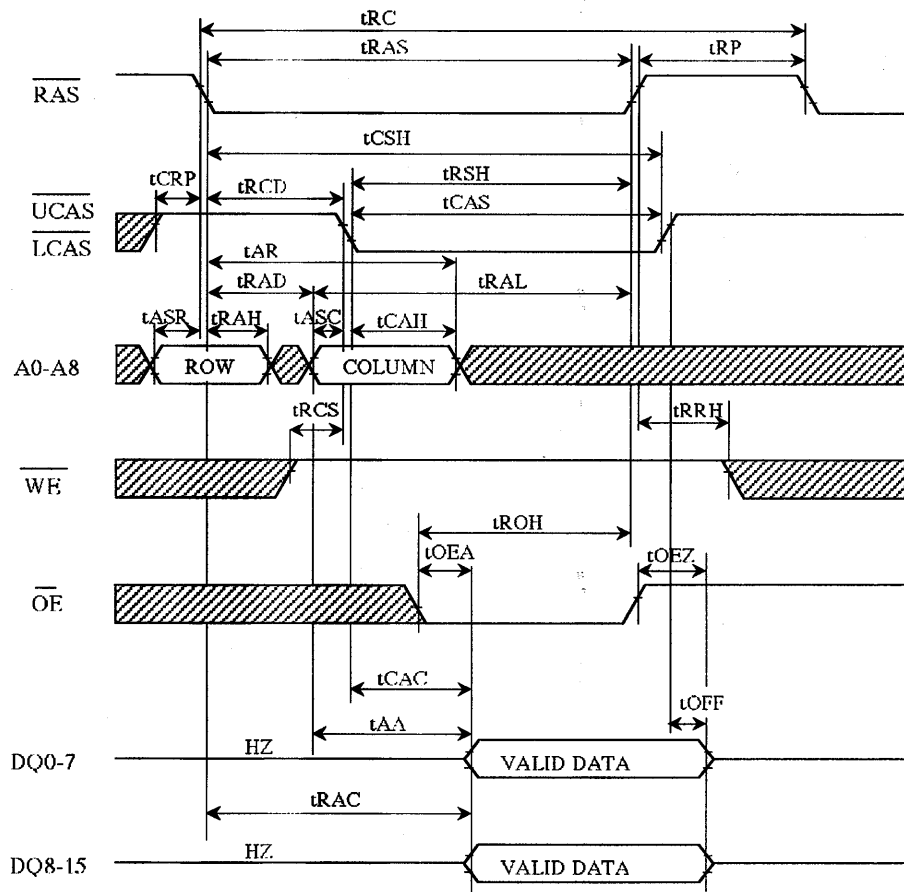
## Notes:

1. All voltages are referenced to V<sub>SS</sub>.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200  $\mu$ s is required after power-up, followed by any  $8\overline{\text{RAS}}$  cycles. (Example:  $\overline{\text{RAS}}$ -only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of  $8\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles instead of  $8\overline{\text{RAS}}$  cycles are required.
5. The AC characteristics assume  $t_r=5\text{ns}$ .
6. V<sub>IH</sub> (Min.) and V<sub>IL</sub> (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
7. Data outputs are measured with a load of 30 pF.  
DOUT reference levels: V<sub>OH</sub>/V<sub>OL</sub>=1.8V/1.4V.
8. t<sub>REZ</sub> (Max.), t<sub>OFF</sub> (Max.), t<sub>WEZ</sub> (Max.) and t<sub>OEZ</sub> (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t<sub>RCH</sub> or t<sub>RRH</sub> must be satisfied for a read cycle.
10. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge of early write cycles and to  $\overline{\text{WE}}$  leading edge in  $\overline{\text{OE}}$ -controlled write cycles and read-modify-write cycles.
11. t<sub>WCS</sub>, t<sub>WRD</sub>, t<sub>CWD</sub> and t<sub>AWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{Min.})$ , the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If  $t_{WRD} \geq t_{WRD}(\text{Min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{Min.})$  and  $t_{AWD} \geq t_{AWD}(\text{Min.})$ , the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the t<sub>RCD</sub> (Max.) limit insures that t<sub>RAC</sub> (Max.) can be met. t<sub>RCD</sub> (Max.) is specified as a reference point only. If t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (Max.) limit, then access time is controlled by t<sub>CDC</sub>.
13. Operation within the t<sub>RAD</sub> (Max.) limit ensures that t<sub>RAC</sub> (Max.) can be met. t<sub>RAD</sub> (Max.) is specified as a reference point only. If t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub> (Max.) limit, then access time is controlled by t<sub>AA</sub>.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while  $\overline{\text{RAS}} = V_{IL}$ .
16. Addresses (A0 - A8) may be changed once or less while  $\overline{\text{CAS}} = V_{IH}$  and  $\overline{\text{RAS}} = V_{IL}$ .
17. This is guaranteed by design. (t<sub>COH</sub>=t<sub>CAC</sub> - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.
19. SL version.

## READ CYCLE (RAS output control)

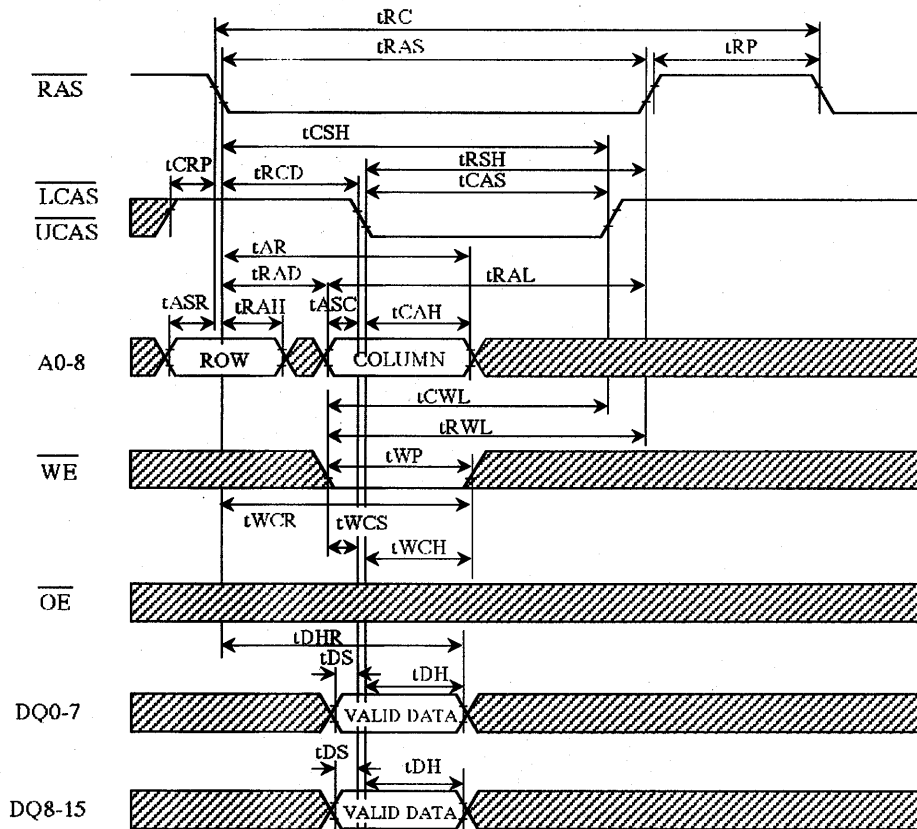


# READ CYCLE ( $\overline{\text{CAS}}$ output control)



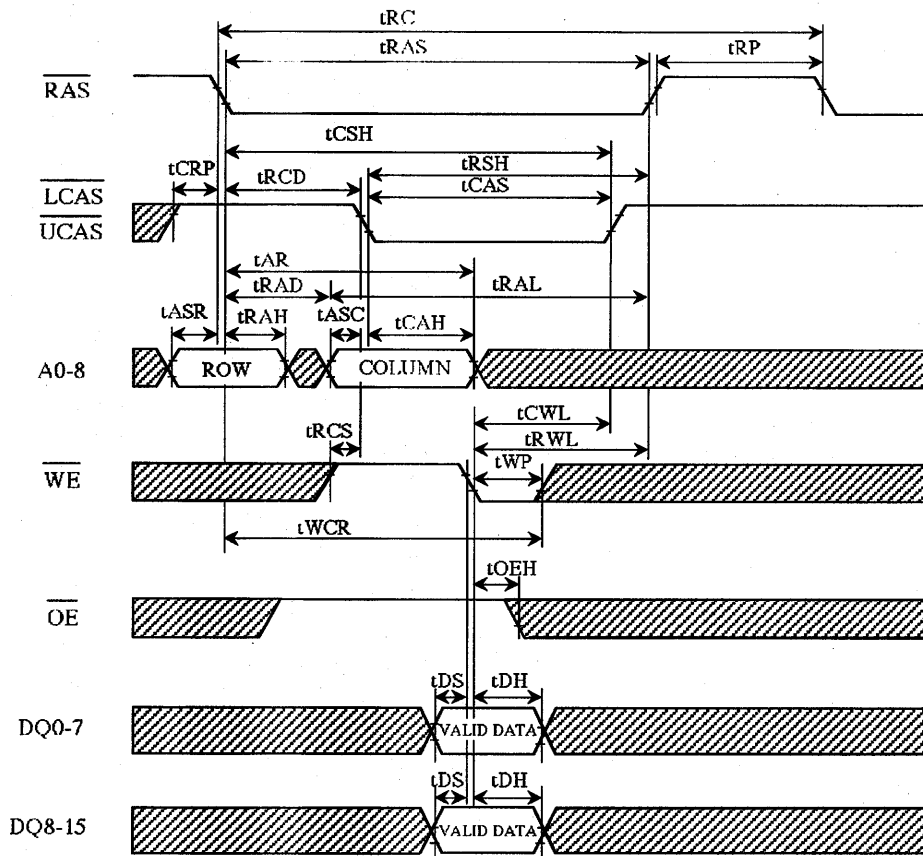
▨ : "H" or "L"

**EARLY WRITE CYCLE ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  active)**



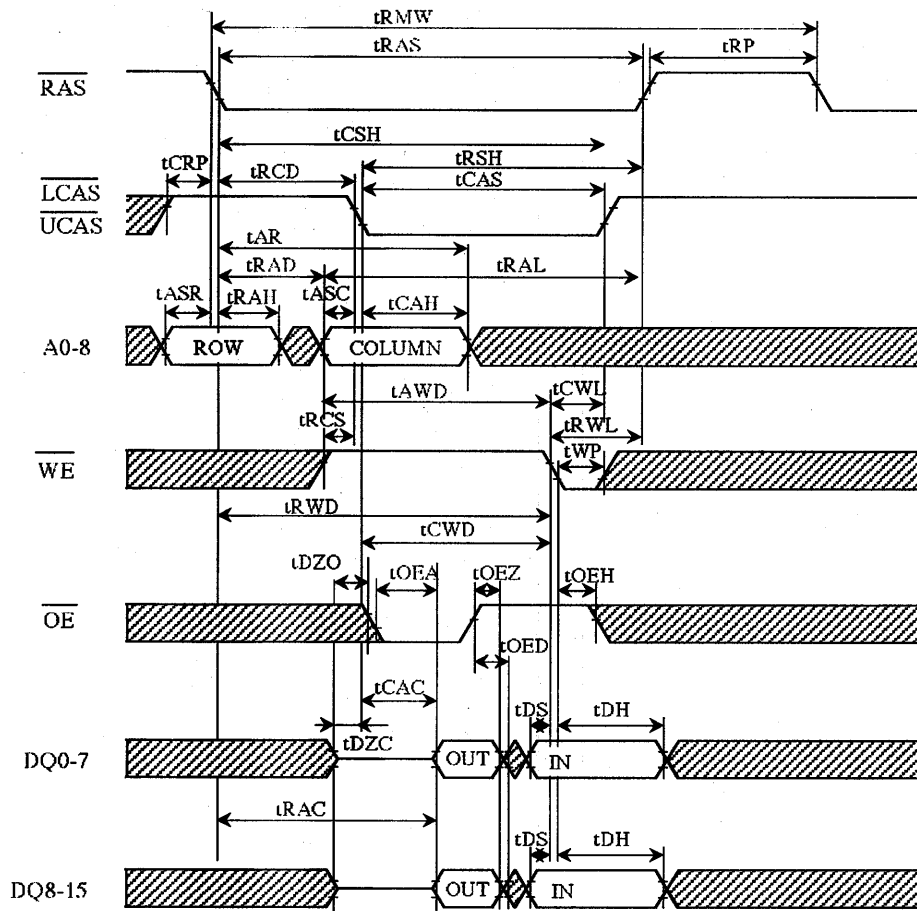
▨ : "H" or "L"

**LATE WRITE CYCLE ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  active)**



▨ : "H" or "L"

# READ MODIFY WRITE CYCLE (LCAS and UCAS active)



▨ : "H" or "L"

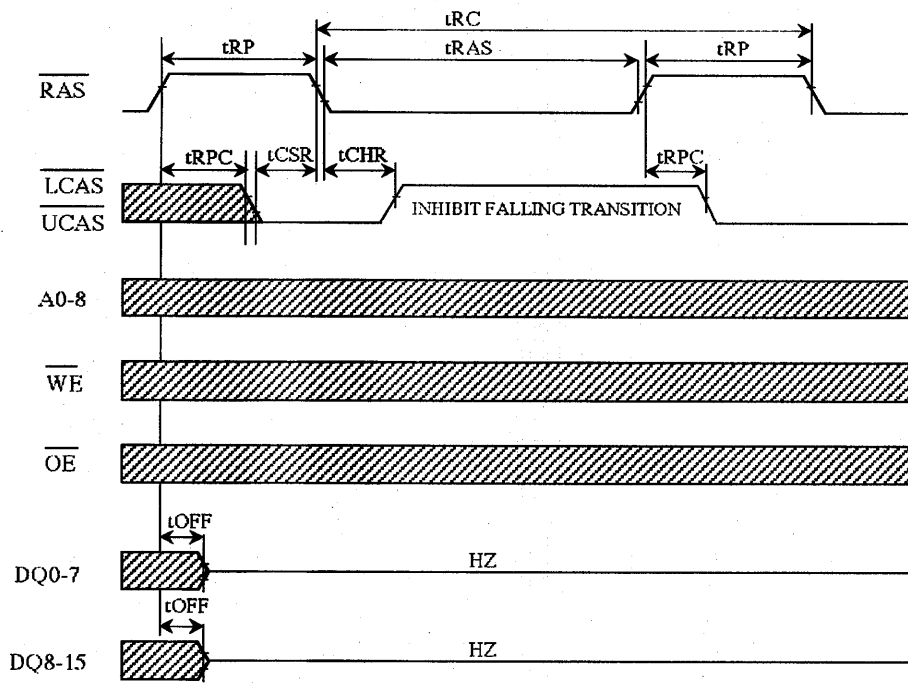






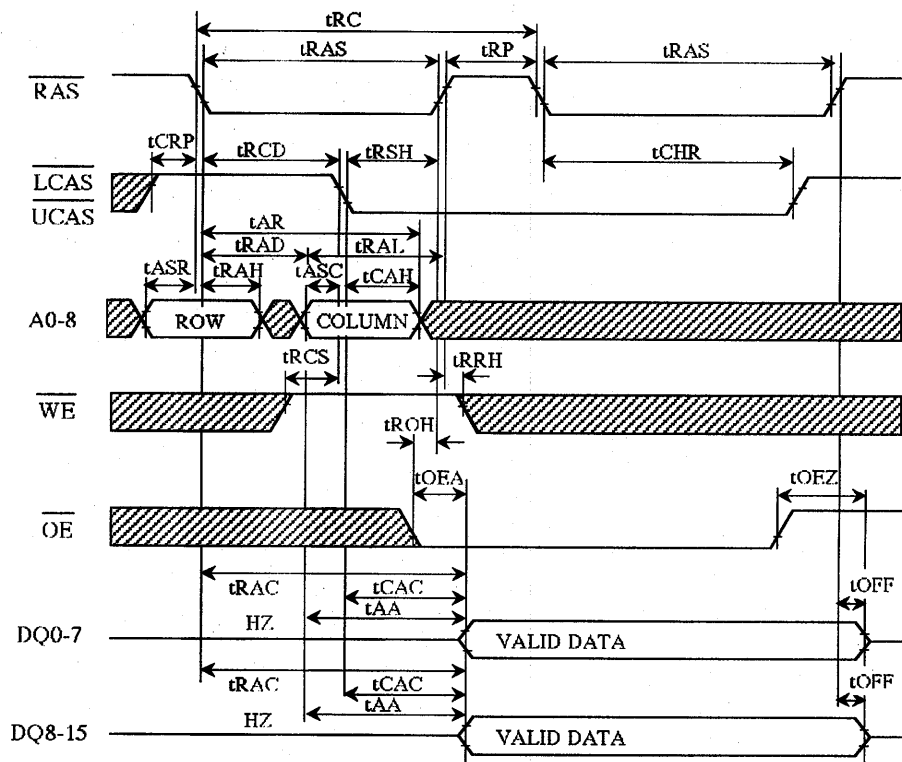


# CAS BEFORE RAS REFRESH CYCLE



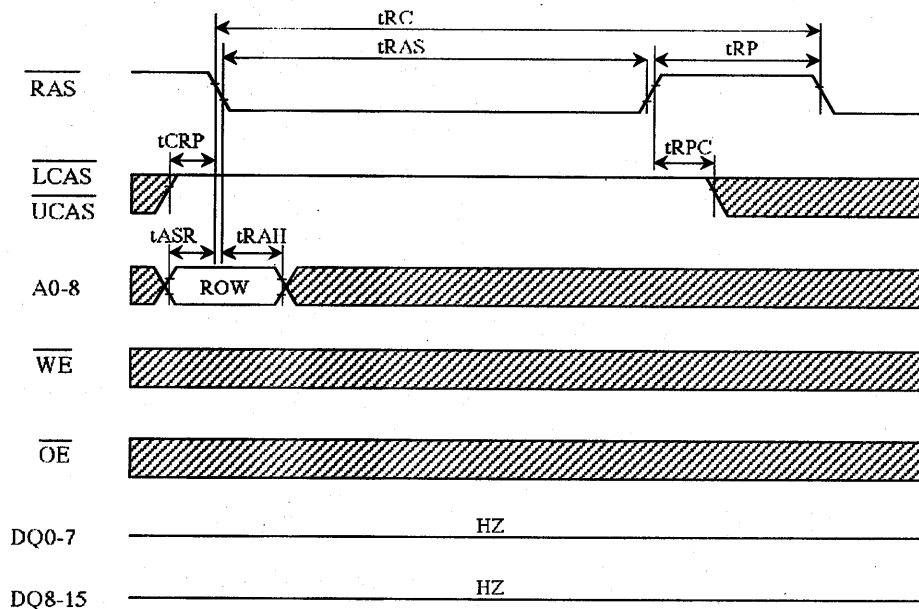
▨ : "H" or "L"

# HIDDEN REFRESH CYCLE



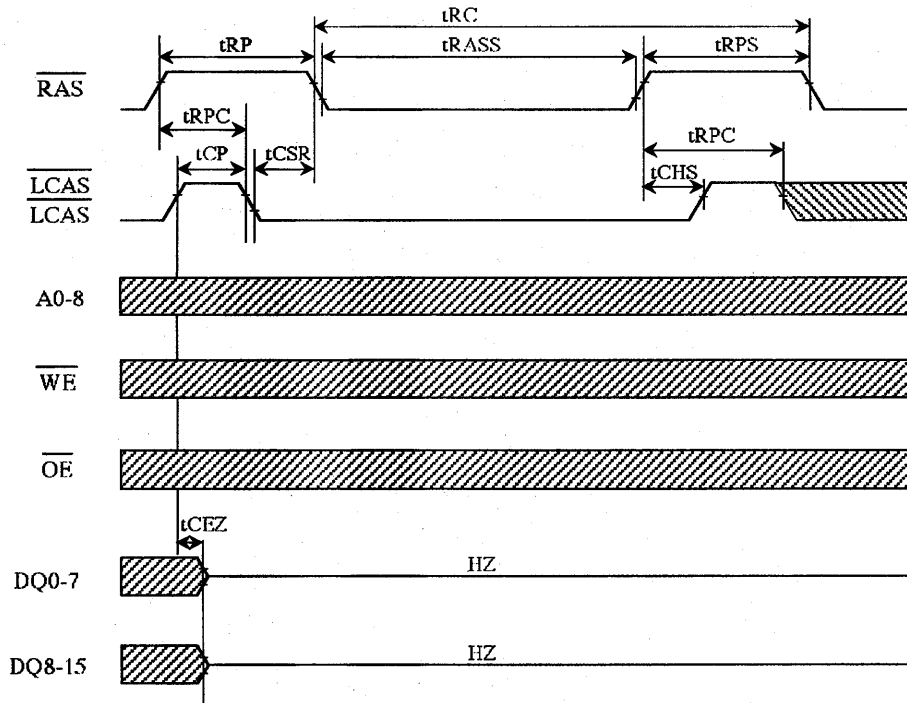
▨ : "H" or "L"

# RAS ONLY REFRESH CYCLE



▨ : "H" or "L"

# CAS BEFORE RAS SELFREFRESH CYCLE



▨ : "H" or "L"

NOTE : SL version.