16Mx36 DRAM SIMM with Fast Page Mode (FPM)

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
WPD16M36-60MSC	60ns	15ns	110ns	40ns
WPD16M36-70MSC	70ns	20ns	130ns	45ns

- Fast Page Mode operation called hyper page mode
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V ± 10% power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Gold or Tin edge connectors

GENERAL DESCRIPTION

The WPD16M36-XMSC is a 16Mbit x 36 Dynamic RAM (DRAM) high density memory module. The WPD16M36-XMSC consists of 8 CMOS 16M x 4 bit 3.3V DRAM components in 32-pin 400-mil SOJ packages, and four CMOS 16M x 1 bit 5.0V DRAM components in 24-pin 300-mil SOJ packages.

A 5.0V to 3.3V convertor supplies power to the 3.3V components, and bus switches convert the signals of the 3.3V components between 5.0V and 3.3V.

The WPD16M36-XMSC has gold edge connectors and the WPD16M36-XMSCT has tin edge connectors. The WPD16M36-60MSC and the WPD16M36-70MSC have a t_{RAC} of 60ns and 70ns respectively.

Pin Names

Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Address Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_5	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

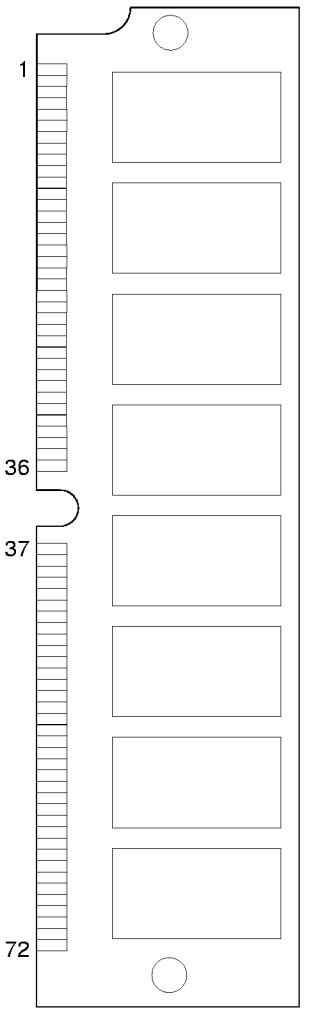
Presence Detect Pins*
(Optional)

Pin	60ns (t_{RAC}=60ns)	70ns (t_{RAC}=70ns)
PD_1	V_{SS}	V_{SS}
PD_2	V_{SS}	V_{SS}
PD_3	NC	V_{SS}
PD_4	NC	NC
PD_5	NC	NC

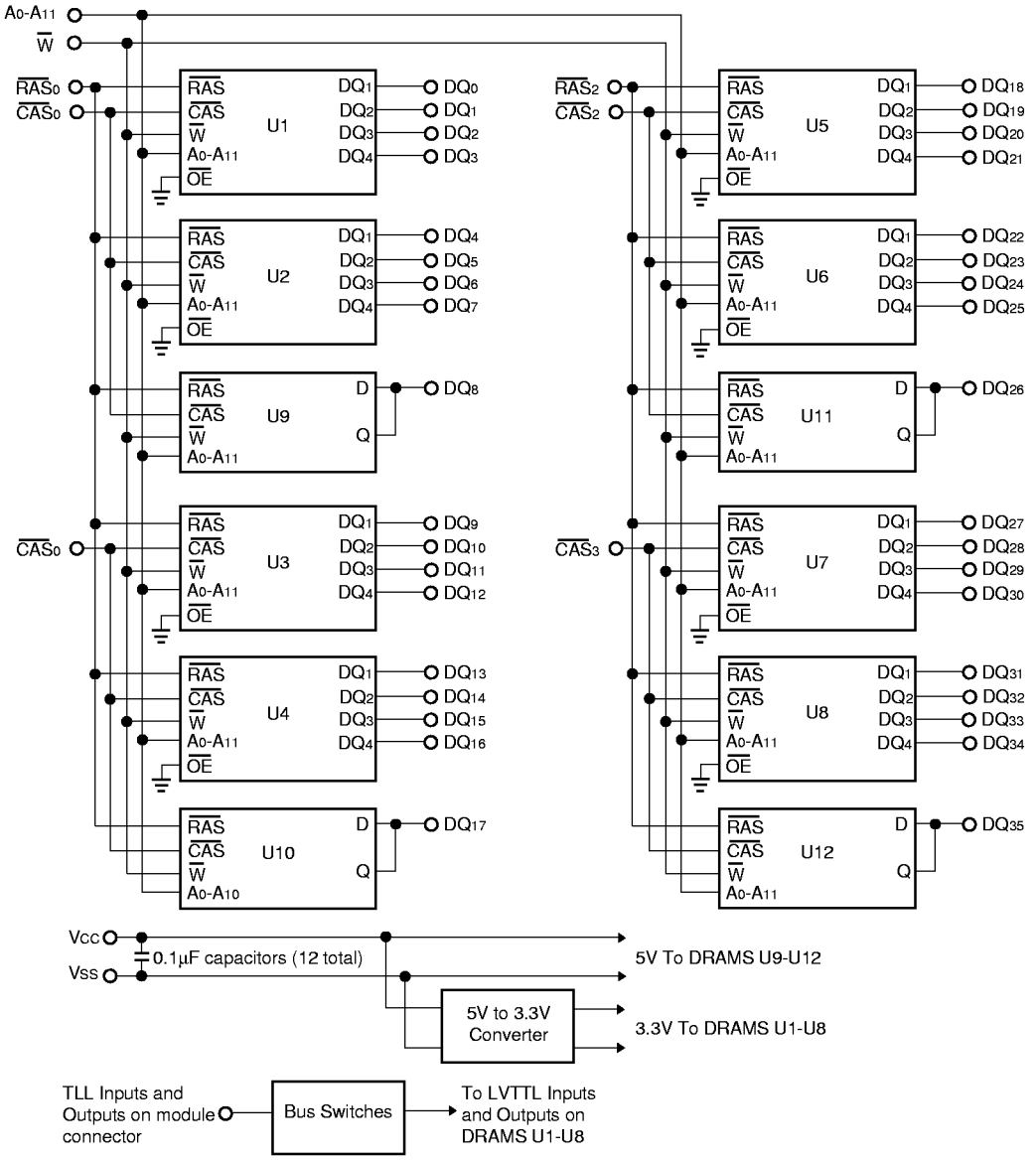
* Pin Connection Changing Available

PIN CONFIGURATION (Front View)

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	A_{11}	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	A_9	56	DQ_{30}
9	DQ_{21}	33	NC	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{31}
11	PD_5	35	DQ_{26}	59	V_{CC}
12	A_0	36	DQ_8	60	DQ_{32}
13	A_1	37	DQ_{17}	61	DQ_{14}
14	A_2	38	DQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{34}
17	A_5	41	$\overline{CAS}_2$	65	DQ_{16}
18	A_6	42	$\overline{CAS}_3$	66	NC
19	A_{10}	43	$\overline{CAS}_1$	67	PD_1
20	DQ_4	44	$\overline{RAS}_0$	68	PD_2
21	DQ_{22}	45	NC	69	PD_3
22	DQ_5	46	NC	70	PD_4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+1*	V
Input Low Voltage	V_{IL}	-1.0**	—	0.8	V

* V_{CC}+2.0V/20ns. Pulse width is measured at V_{CC}.

** -2.0V/20ns. Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	WPD16M36-60 WPD16M36-70	I_{CC1}	— —	1440 1320	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	—	24	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	WPD16M36-60 WPD16M36-70	I_{CC3}	— —	1440 1320	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	WPD16M36-60 WPD16M36-70	I_{CC4}	— —	540 460	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)		I_{CC5}	—	12	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	WPD16M36-60 WPD16M36-70	I_{CC6}	— —	1440 1320	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0V)		I_{IL}	-60	60	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})		I_{OL}	-10	10	µA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A=25 °C, V_{CC}=5.0, F=1MHZ)

Item	Symbol	Typ	Units
Input Capacitance (A_0-A_{10})	C_{IN1}	75	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	99	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{RAS}_2$)	C_{IN3}	57	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	36	pF
Input/Output Capacitance (DQ_0-DQ_{35})	C_{DQ1}	29	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	WPD16M36-60		WPD16M36-70		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		15		20	ns	3,4,5
Access time from column address	t_{AA}		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	ns	
$\overline{RAS}$ to CAS delay time	t_{RCD}	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	10
$\overline{RAS}$ to CAS precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		15		ns	6
Write command pulse width	t_{WP}	10		15		ns	

(continued on the next page)

AC CHARACTERISTICS (continued)

Parameter	Symbol	WPD16M36-60		WPD16M36-70		Unit	Notes
		Min	Max	Min	Max		
Data-in hold time	t_{DH}	10		15		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		ns	
$\overline{CAS}$ precharge time (fast page)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (fast page)	t_{RASP}	60	200,000	70	200,000	ns	
W to $\overline{RAS}$ precharge (C-B-R refresh)	t_{WRP}	10		10		ns	
W to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		ns	

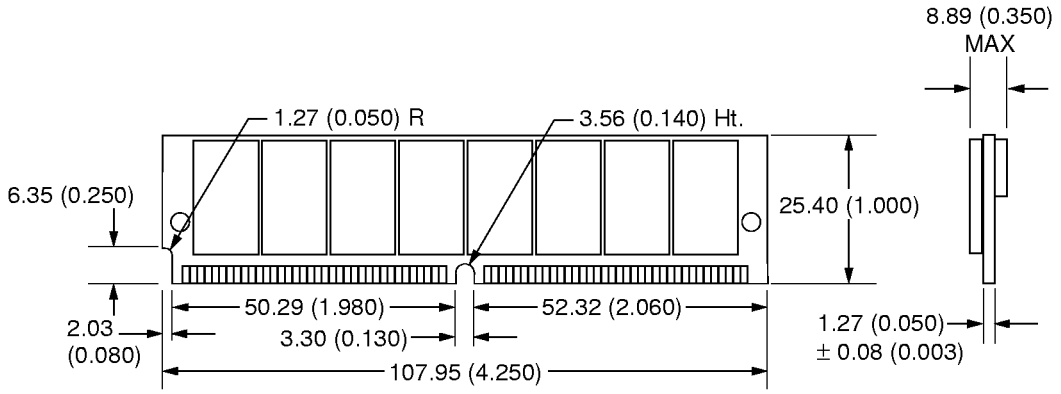
Notes

1. An initial pause of 200 ms is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 2ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes the $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

Timing Diagrams

Please refer to attached Timing Chart I.

PACKAGE DIMENSIONS



TOLERANCES: ±0.13 (0.005) UNLESS OTHERWISE SPECIFIED
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P D 16M36 - X MS C X

LEAD FINISH:
T = Tin Edge Connectors
Blank = Gold Edge Connectors

DEVICE GRADE:
C = Commercial 0 to + 70°C

PACKAGE TYPE:
MS = 72 pin SIMM

ACCESS TIME In ns

ORGANIZATION, 16M x 36

DRAM

Plastic Module

WHITE MICROELECTRONICS