

# MB81257-10/-12/-15

## MOS 262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

### 262,144-Bit Dynamic Random Access Memory

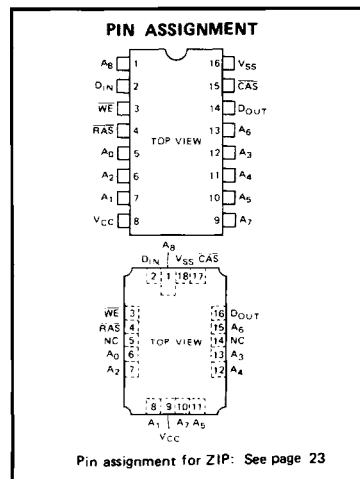
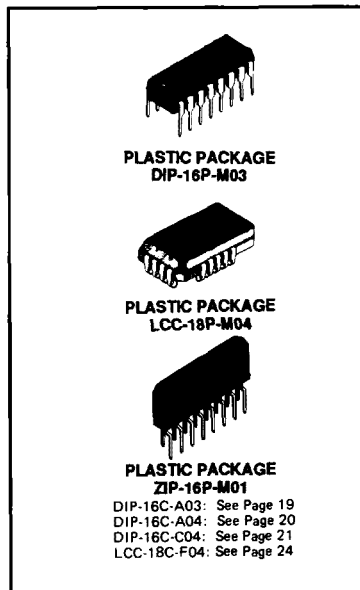
The Fujitsu MB81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and a compact layout are required.

Multiplexed row and column address inputs permit the MB81257 to be housed in standard 16-pin DIP and ZIP packages or an 18-pin PLCC package. Pinouts conform to the JEDEC-approved pinouts. Additionally, the MB81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. CAS-before-RAS refresh provides an on-chip refresh capability that is upwardly compatible with the MB8266A. The MB81257 also features nibble mode which allows high speed serial access of up to 4 bits of data.

The MB81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.

- 262,144 x 1 RAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time
  - 100 ns max. (MB 81257-10)
  - 120 ns max. (MB 81257-12)
  - 120 ns max. (MB 81257-15)
- Cycle Time
  - 200 ns min. (MB 81257-10)
  - 220 ns min. (MB 81257-12)
  - 260 ns min. (MB 81257-15)
- Nibble Cycle Time
  - 45 ns max. (MB 81257-10)
  - 50 ns max. (MB 81257-12)
  - 60 ns max. (MB 81257-15)
- Single +5 V Supply,  $\pm 10\%$  tolerance
- Low Power
  - 385 mW max. (MB 81257-10)
  - 358 mW max. (MB 81257-12)
  - 314 mW max. (MB 81257-15)
  - 25 mW max. (standby)
- 256 refresh cycles every 4 ms
- CAS-before-RAS, RAS-only, Hidden refresh capability
- High speed Read-Write cycle
- t<sub>AR</sub>, t<sub>WR</sub>, t<sub>CHR</sub>, t<sub>RWD</sub> are eliminated
- Output unlatched cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-Pin Plastic Packages:
  - DIP (MB81257-XXP)
  - ZIP (MB81257-XXPSZ)
- Standard 18-Pin Plastic Package:
  - PLCC(MB81257-XXPV)
- Standard 16-Pin Ceramic Packages:
  - DIP (MB81257-XXC) Seam Weld
  - DIP (MB81257-XXZ) Cerdip
- Standard 18-Pad Ceramic Package:
  - LCC (MB81257-XXTV)

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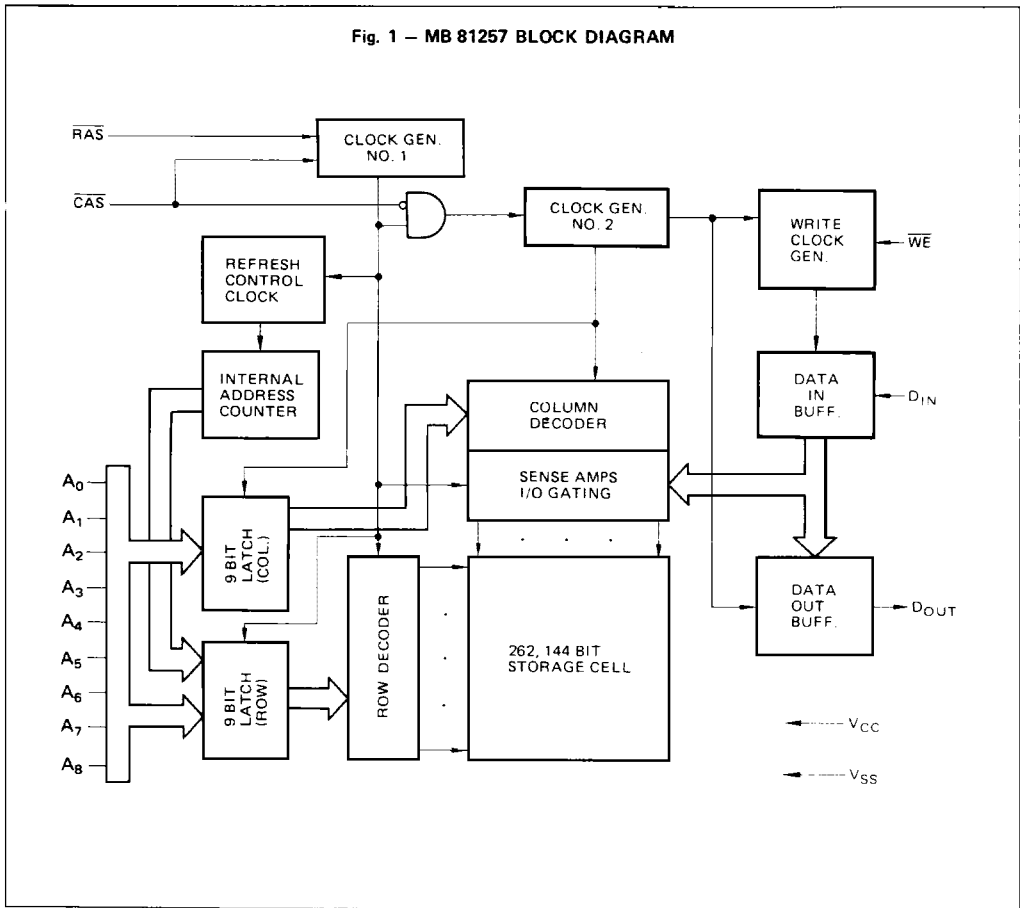
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7	V
Voltage of V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub>	-1 to +7	V
Storage Temperature	Ceramic	-55 to +150	°C
	Plastic		
Power Dissipation	P <sub>D</sub>	1.0	W
Short Circuit Output Current	—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ )

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0$ to $A_8$ , $D_{IN}$	$C_{IN1}$		7	pF
Input Capacitance $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	$C_{IN2}$		8	pF
Output Capacitance $D_{OUT}$	$C_{OUT}$		7	pF

## RECOMMENDED OPERATING CONDITIONS

(Referenced to  $V_{SS}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature 0°C to +70°C
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
	$V_{SS}$	0	0	0	V	
Input High Voltage, all inputs	$V_{IH}$	2.4		6.5	V	
Input Low Voltage, all inputs	$V_{IL}$	-2.0		0.8	V	

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ( $\overline{RAS}$ , $\overline{CAS}$ cycling; $t_{RC} = \text{Min.}$ )	$I_{CC1}$			70	mA
		MB 81257-10		65	
		MB 81257-12		57	
STANDBY CURRENT Standby Power Supply Current ( $\overline{RAS}$ , $\overline{CAS} = V_{IH}$ )	$I_{CC2}$			4.5	mA
		MB 81257-10			
		MB 81257-12			
REFRESH CURRENT 1* Average Power Supply Current ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ ; $t_{RC} = \text{Min.}$ )	$I_{CC3}$			60	mA
		MB 81257-10		55	
		MB 81257-15		50	
NIBBLE MODE CURRENT* Average Power Supply Current ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling; $t_{NC} = \text{Min.}$ )	$I_{CC4}$			22	mA
		MB 81257-10		20	
		MB 81257-15		18	
REFRESH CURRENT 2* Average Power Supply Current ( $\overline{CAS}$ before $\overline{RAS}$ ; $t_{RC} = \text{Min.}$ )	$I_{CC5}$			65	mA
		MB 81257-10		60	
		MB 81257-15		55	
INPUT LEAKAGE CURRENT any input ( $V_{IN} = 0V$ to $5.5V$ , $V_{CC} = 5.5V$ , $V_{SS} = 0V$ , all other pins not under test = $0V$ )	$I_{I(L)}$	-10		10	$\mu A$
OUTPUT LEAKAGE CURRENT (Data is disabled, $V_{OUT} = 0V$ to $5.5V$ )	$I_{O(L)}$	-10		10	$\mu A$
OUTPUT LEVEL Output Low Voltage ( $I_{OL} = 4.2 \text{ mA}$ )	$V_{OL}$			0.4	V
OUTPUT LEVEL Output high Voltage ( $I_{OH} = -5.0 \text{ mA}$ )	$V_{OH}$	2.4			V

NOTE \* :  $I_{CC}$  is depended on output loading and cycle rates. Specified values are obtained with the output open.

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) **NOTES 1,2,3**

Parameter	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
		Min	Max	Min	Max	Min	Max	
Time between Refresh	$t_{REF}$		4		4		4	ms
Random Read/Write Cycle time	$t_{RC}$	200		220		260		ns
Read-Write Cycle Time	$t_{RWC}$	200		220		260		ns
Access Time from $\overline{RAS}$	$t_{RAC}$		100		120		150	ns
Access Time from $\overline{CAS}$	$t_{CAC}$		50		60		75	ns
Output Buffer Turn off Delay	$t_{OFF}$	0	25	0	25	0	30	ns
Transition Time	$t_T$	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	$t_{RP}$	85		90		100		ns
$\overline{RAS}$ Pulse Width	$t_{RAS}$	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time	$t_{RSH}$	55		60		75		ns
$\overline{CAS}$ Pulse width	$t_{CAS}$	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time	$t_{CSH}$	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$t_{RCD}$	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	$t_{CRS}$	10		10		10		ns
Row Address Set Up Time	$t_{ASR}$	0		0		0		ns
Row Address Hold Time	$t_{RAH}$	10		12		15		ns
Column Address Set Up Time	$t_{ASC}$	0		0		0		ns
Column Address Hold Time	$t_{CAH}$	15		20		25		ns
Read Command Set Up Time	$t_{RCS}$	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	$t_{RCH}$	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	$t_{RRH}$	20		20		20		ns
Write Command Set Up Time	$t_{WCS}$	0		0		0		ns
Write Command Pulse Width	$t_{WP}$	15		20		25		ns
Write Command Hold Time	$t_{WCH}$	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time	$t_{RWL}$	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time	$t_{CWL}$	20		30		25		ns
Data In Set Up Time	$t_{DS}$	0		0		0		ns
Data In Hold Time	$t_{DH}$	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	$t_{CWD}$	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ( $\overline{CAS}$ -before- $\overline{RAS}$ cycle)	$t_{FCS}$	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ( $\overline{CAS}$ -before- $\overline{RAS}$ cycle)	$t_{FCH}$	20		25		30		ns

## AC CHARACTERISTICS

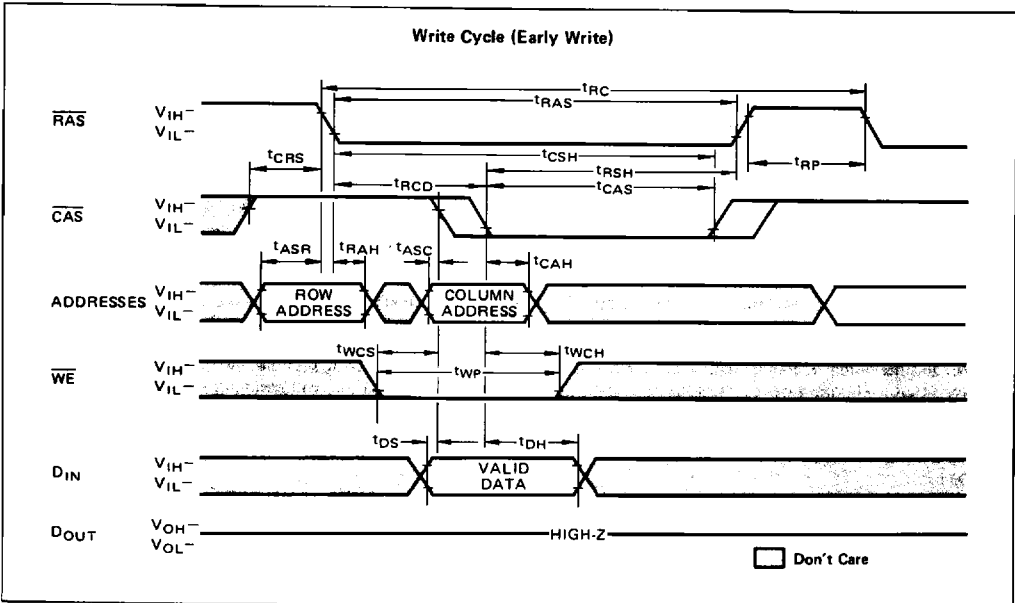
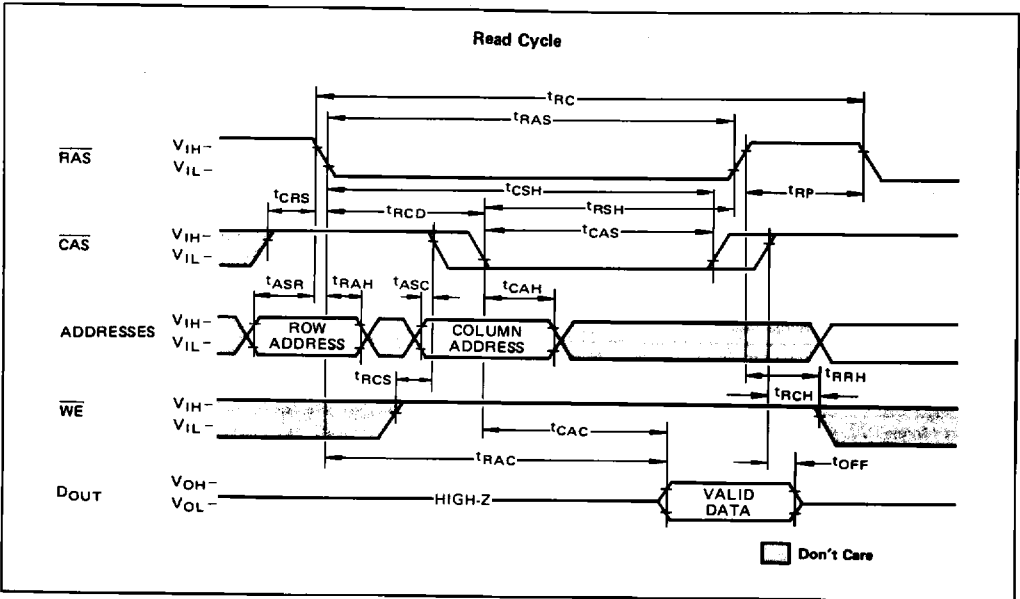
(Recommended operating conditions unless otherwise noted.)

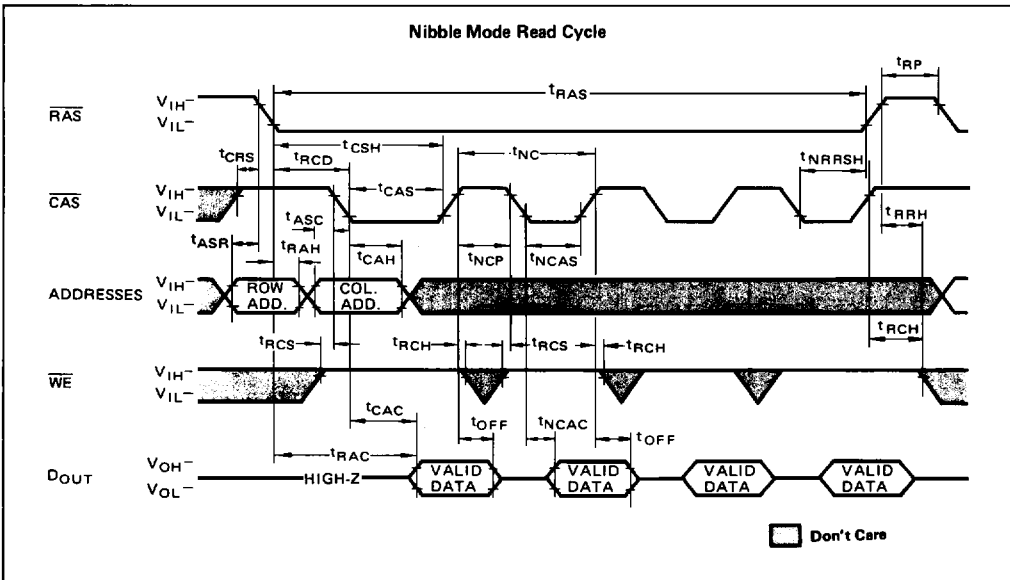
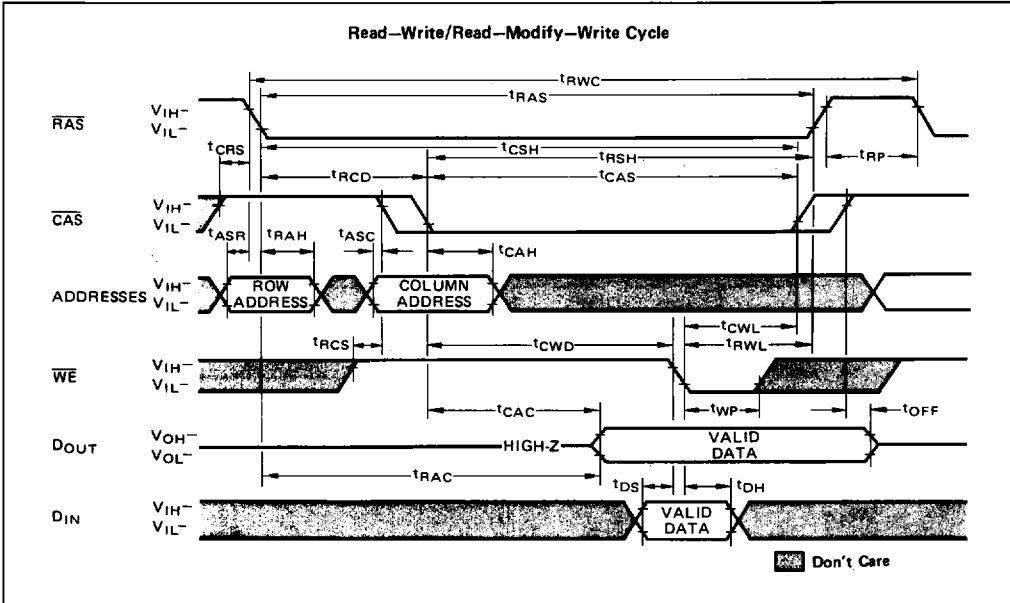
Parameter	NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
			Min	Max	Min	Max	Min	Max	
CAS Precharge Time (CAS-before-RAS cycle)		$t_{CPR}$	20		25		30		ns
RAS Precharge to CAS Active Time (Refresh cycles)		$t_{RPC}$	20		20		20		ns
Nibble Mode Read/Write Cycle Time		$t_{NC}$	45		50		60		ns
Nibble Mode Read-Write Cycle Time		$t_{NRWC}$	45		50		60		ns
Nibble Mode Access Time		$t_{NCAC}$		20		25		30	ns
Nibble Mode CAS Pulse Width		$t_{NCAS}$	20		25		30		ns
Nibble Mode CAS Precharge Time		$t_{NCP}$	15		15		20		ns
Nibble Mode Read RAS Hold Time		$t_{NRRSH}$	20		25		30		ns
Nibble Mode Write RAS Hold Time		$t_{NWRSH}$	35		40		45		
Nibble Mode CAS Hold Time Referenced to RAS		$t_{RNH}$	20		20		20		ns
Refresh Counter Test Cycle Time	11	$t_{RTC}$	330		375		430		ns
Refresh Counter Test RAS Pulse Width	11	$t_{TRAS}$	230	10000	265	10000	320	10000	ns
Refresh Counter Test CAS Precharge Time	11	$t_{CPT}$	50		60		70		ns

### Notes:

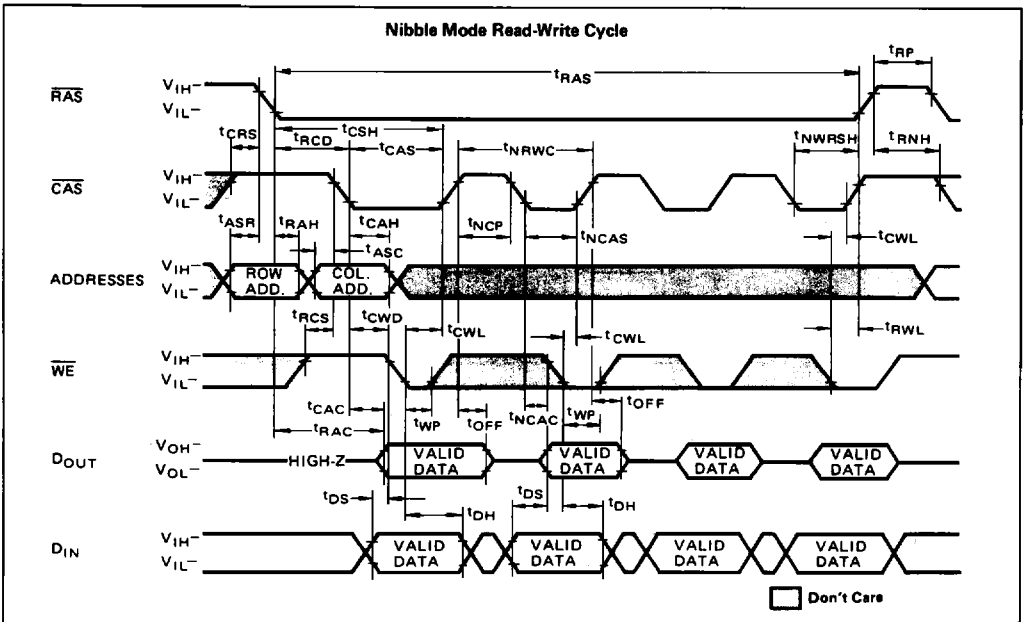
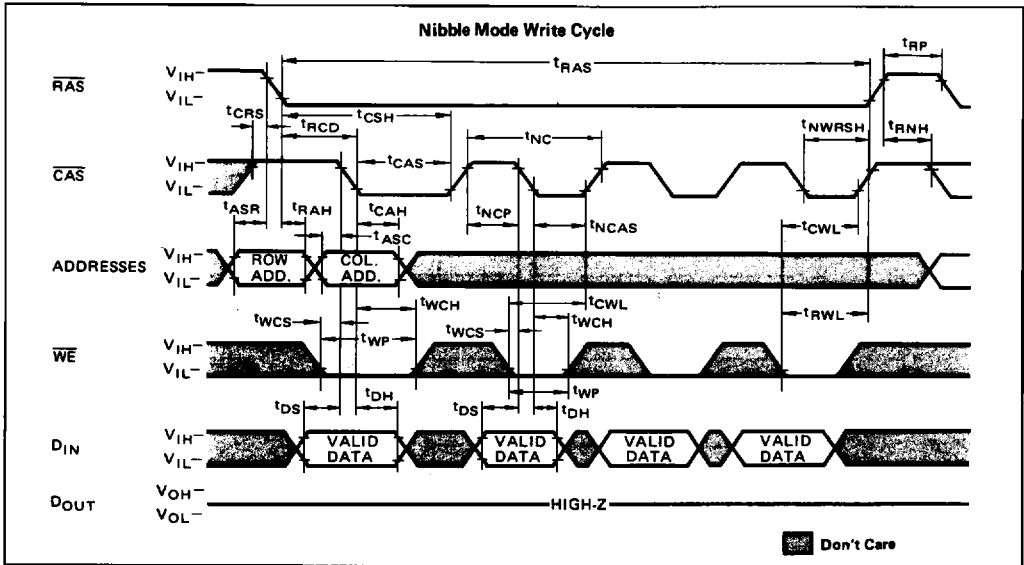
- 1 An initial pause of 200  $\mu$ s is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.  
If internal refresh counter is to be effective, a minimum of 8 CAS before RAS refresh cycles are required.
- 2 AC characteristics assume  $t_T = 5$  ns.
- 3  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
- 4 Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
- 5 Assumes that  $t_{RCD} \geq t_{RCD}(\max)$ .
- 6 Measured with a load equivalent to 2 TTL loads and 100 pF.
- 7 Operation within the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- 8  $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T (t_T = 5\text{ns}) + t_{ASC}(\min)$
- 9 Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- 10  $t_{WCS}$  and  $t_{CWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If  $t_{CWD} \geq t_{CWD}(\min)$ , the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
- 11 Test mode cycle only.

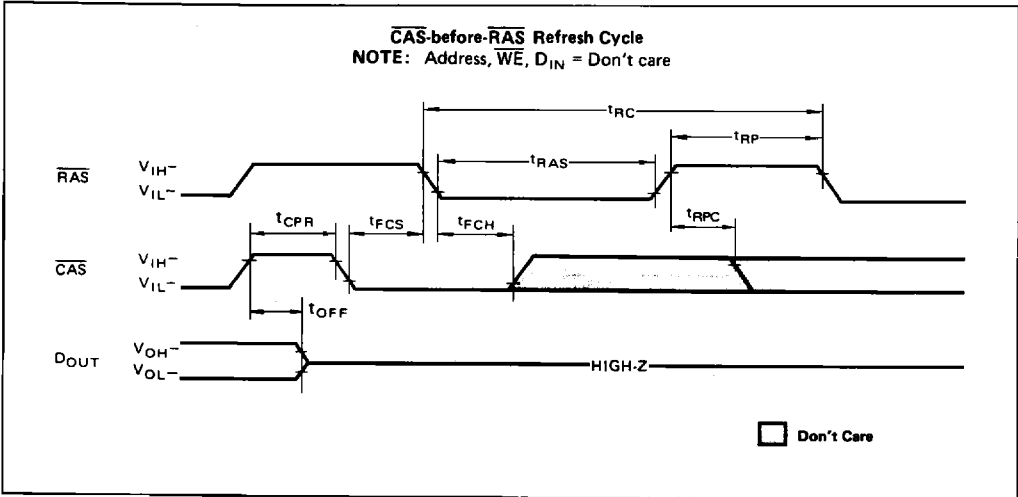
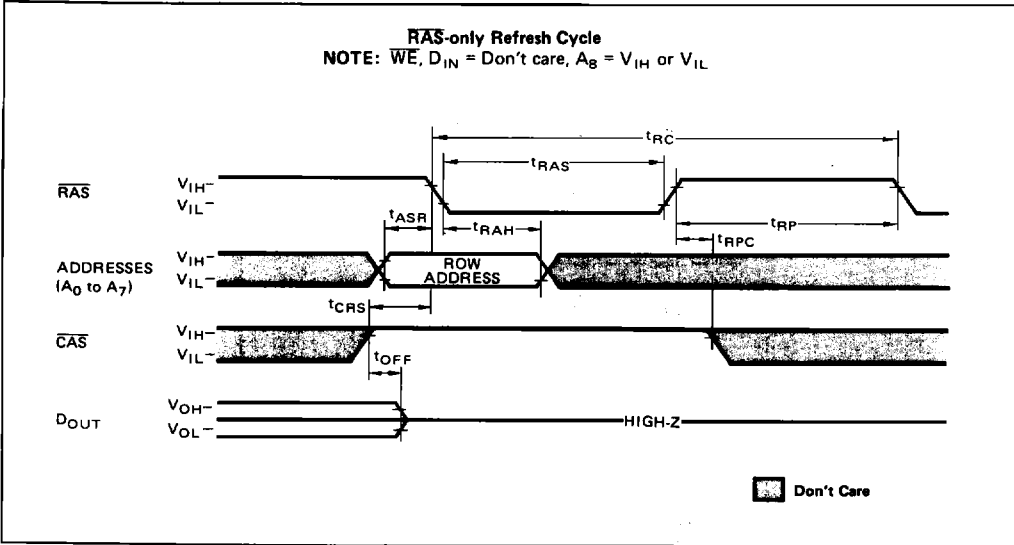
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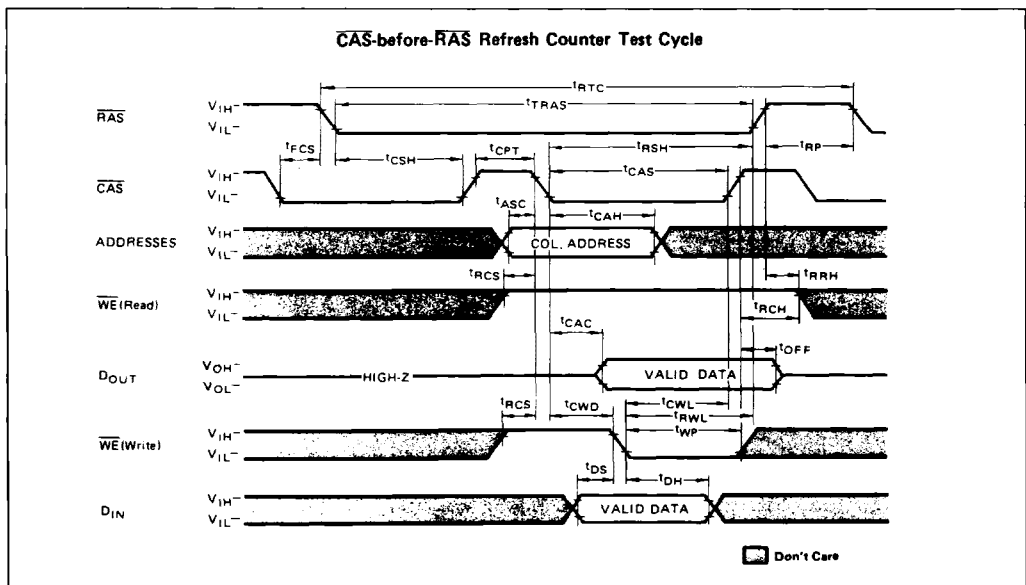
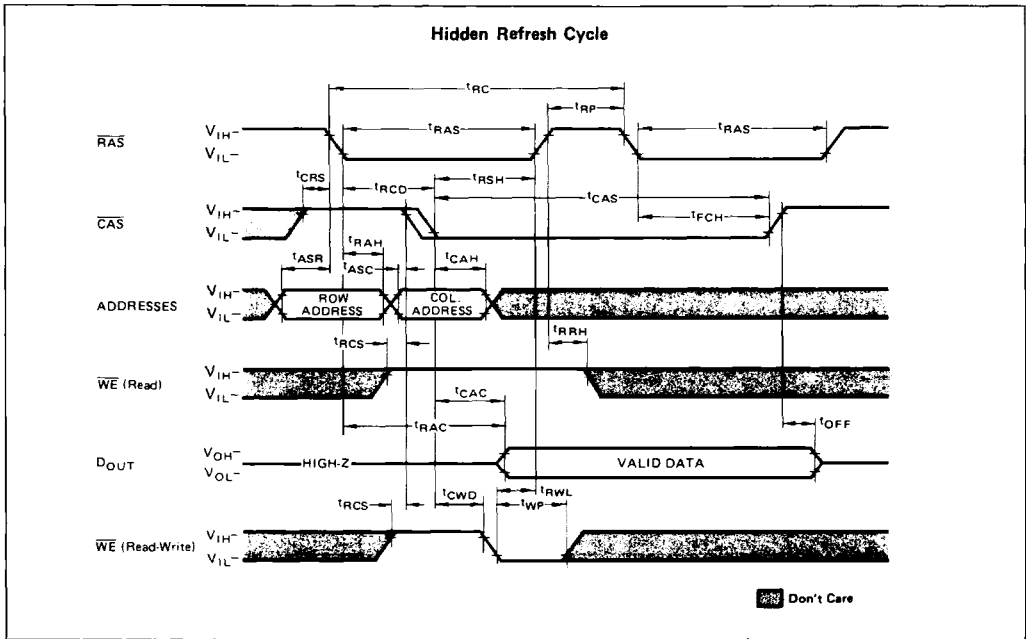


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## DESCRIPTION

### Simple Timing Requirement

The MB 81257 has improved circuitry that eases timing requirements for high speed access operations. The MB 81257 can operate under the condition of  $t_{RCD}(\max) = t_{CAC}$  thus providing optimal timing for address multiplexing. In addition, the MB 81257 has the minimal hold times of Address ( $t_{CAH}$ ),  $\overline{WE}$  ( $t_{WCH}$ ) and  $D_{IN}$  ( $t_{DH}$ ). The MB 81257 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to  $\overline{RAS}$  non-restrictive and deleted them from the data sheet. These include  $t_{AR}$ ,  $t_{WCR}$ ,  $t_{DHR}$  and  $t_{RWD}$ . As a result, the hold times of the Column Address,  $D_{IN}$  and  $\overline{WE}$  as well as  $t_{CWD}$  ( $\overline{CAS}$  to  $\overline{WE}$  Delay) are not restricted by  $t_{RCD}$ .

### Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81257. Nine row-address bits are established on the input pins ( $A_0$  to  $A_8$ ) and are latched with the Row Address Strobe ( $\overline{RAS}$ ). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ( $\overline{CAS}$ ). All row addresses must be stable on or before the falling edge of  $\overline{RAS}$ .  $\overline{CAS}$  is internally inhibited (or "gated") by  $\overline{RAS}$  to permit triggering of  $\overline{CAS}$  as soon as the Row Address Hold Time ( $t_{RAH}$ ) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

### Write Enable:

The read mode or write mode is selected with the  $\overline{WE}$  input. A high on  $\overline{WE}$  selects read mode, low selects write mode. The data input is disabled when read mode is selected.

### Data Input:

Data is written into the MB 81257 during a write or read-write cycle. The later falling edge of  $\overline{WE}$  or  $\overline{CAS}$  is a strobe for the Data In ( $D_{IN}$ ) register. In a write cycle, if  $\overline{WE}$  is brought low

before  $\overline{CAS}$ ,  $D_{IN}$  is strobed by  $\overline{CAS}$ , and the set-up and hold times are referenced to  $\overline{CAS}$ . In a read-write cycle,  $\overline{WE}$  can be delayed after  $\overline{CAS}$  has been low and  $\overline{CAS}$  to  $\overline{WE}$  Delay Time ( $t_{CWD}$ ) has been satisfied. Thus  $D_{IN}$  is strobed by  $\overline{WE}$ , and set-up and hold times are referenced to  $\overline{WE}$ .

### Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until  $\overline{CAS}$  is brought low. In a read cycle, or read-write cycle, the output is valid after  $t_{RAC}$  from transition of  $\overline{RAS}$  when  $t_{RCD}(\max)$  is satisfied, or after  $t_{CAC}$  from transition of  $\overline{CAS}$  when the transition occurs after  $t_{RCD}(\max.)$  Data remain valid until  $\overline{CAS}$  is returned to a high level. In a write cycle, the identical sequence occurs, but data is not valid.

### Fast Read-While-Write cycle

The MB 81257 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings, described in the previous section. The output buffer is controlled by the state of  $\overline{WE}$  when  $\overline{CAS}$  goes low. When  $\overline{WE}$  is low during  $\overline{CAS}$  transition to low, the MB 81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when  $\overline{WE}$  goes low after  $t_{CWD}$  following  $\overline{CAS}$  transition to low, the MB 81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from  $D_{IN}$  is written into the cell selected. Therefore, a very fast read write cycle ( $t_{RWC} = t_{RC}$ ) is possible with the MB 81257.

### Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses ( $CA_8$ ,  $RA_8$ ) are

used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling  $\overline{CAS}$  high then low while  $\overline{RAS}$  remains low. Toggling  $\overline{CAS}$  causes  $RA_8$  and  $CA_8$  to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the  $D_{OUT}$  pin is determined by the first normal access cycle.

The data output is controlled only by the  $\overline{WE}$  state referenced at the  $\overline{CAS}$  negative transition of the normal cycle (first nibble bit). That is, when  $t_{WCS} > t_{WCS}(\min)$  is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the  $\overline{WE}$  state. Whereas, when  $t_{CWD} > t_{CWD}(\min)$  is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the  $\overline{WE}$  state. The write operation is done during the period in which the  $\overline{WE}$  and  $\overline{CAS}$  clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of  $\overline{WE}$  ( $t_{WCS}$  and  $t_{CWD}$ ) during the normal cycle (first nibble bit). See Fig. 2.

### Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ( $A_0$  to  $A_7$ ) at least every 4 ms.

The MB 81257 offers the following 3 types of refresh.

### $\overline{RAS}$ -only Refresh;

The  $\overline{RAS}$  only refresh avoids any output during refresh because the output buffer is in the high impedance state unless  $\overline{CAS}$  is brought low. Strobing each

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of 256 row-addresses ( $A_0$  to  $A_7$ ) with  $\overline{RAS}$  will cause all bits in each row to be refreshed. Further  $\overline{RAS}$ -only refresh results in a substantial reduction in power dissipation. During  $\overline{RAS}$ -only refresh cycle, either  $V_{IH}$  or  $V_{IL}$  is permitted to  $A_8$ .

**$\overline{CAS}$ -before- $\overline{RAS}$  Refresh;**

$\overline{CAS}$ -before- $\overline{RAS}$  refreshing available on the MB 81257 offers an alternate refresh method. If  $\overline{CAS}$  is held low for the specified period ( $t_{FCS}$ ) before  $\overline{RAS}$  goes to low, on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{CAS}$ -before- $\overline{RAS}$  refresh operation.

**Hidden Refresh;**

A hidden refresh cycle may takes place while maintaining latest valid data at the output by extending the  $\overline{CAS}$  active time. For the MB 81257, a hidden refresh cycle is  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.

The internal refresh address counters provide the refresh addresses, as in a normal  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle.

**$\overline{CAS}$ -before- $\overline{RAS}$  Refresh Counter Test Cycle:**

A special timing sequence using  $\overline{CAS}$ -before- $\overline{RAS}$  counter test cycle provides a convenient method of verifying the functionality of  $\overline{CAS}$ -before- $\overline{RAS}$  refresh activated circuitry. After the  $\overline{CAS}$ -before- $\overline{RAS}$  refresh operation, if  $\overline{CAS}$  goes to high and goes to low again while  $\overline{RAS}$  is held low, the read and write operation are enabled. This is shown in the  $\overline{CAS}$ -before- $\overline{RAS}$  counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

\*A ROW ADDRESS – Bits  $A_0$  to  $A_7$  are defined by the refresh counter. The bit  $A_8$  is set high internally.

\*A COLUMN ADDRESS – All the bits  $A_0$  to  $A_8$  are defined by latching levels on  $A_0$  to  $A_8$  at the second falling edge of  $\overline{CAS}$ .

**Suggested  $\overline{CAS}$ -before- $\overline{RAS}$  Counter Test Procedure**

The timing, as shown in the  $\overline{CAS}$ -before- $\overline{RAS}$  Counter Test Cycle, is used for the following operations:

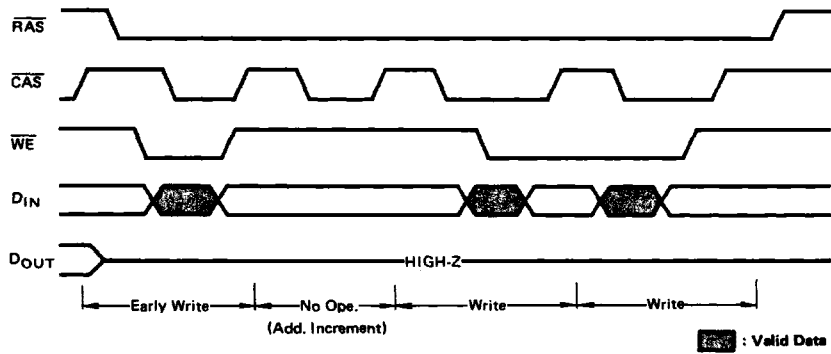
- 1) Initialize the internal refresh address counter by using eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles.
- 2) Throughout the test, use the same column address, and keep  $RA_8$  high.
- 3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
- 4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
- 5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
- 6) Complement the test pattern and repeat step 3), 4) and 5).

**Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE**

SEQUENCE	NIBBLE BIT	$RA_8$	ROW ADDRESS	$CA_8$	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Fig. 2 – Nibble Mode

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delayed write (Read-Write)

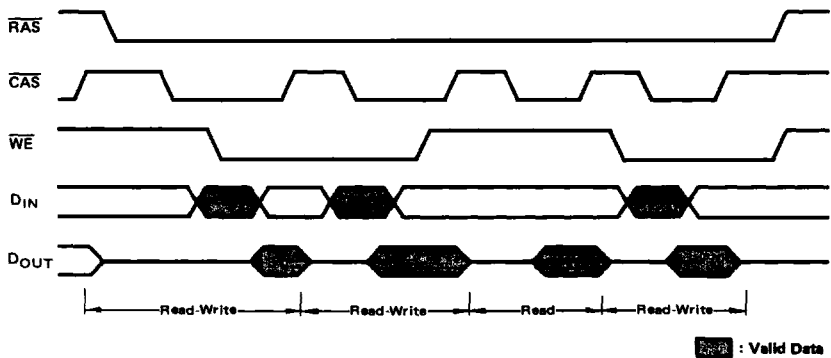
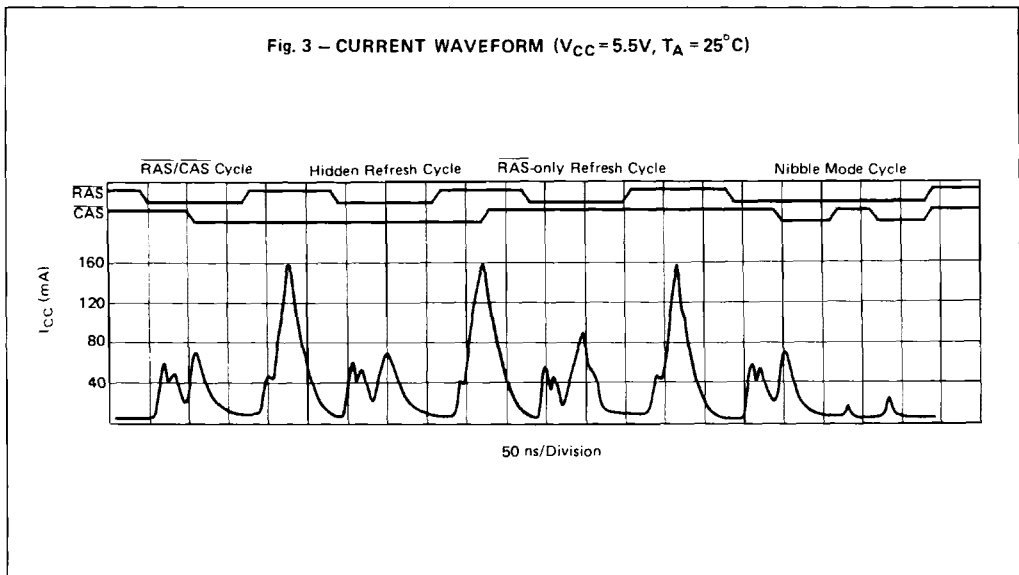


Table-2 FUNCTIONAL TRUTH TABLE

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	D <sub>IN</sub>	D <sub>OUT</sub>	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{\text{wcs}} \geq t_{\text{wcs}}(\text{min})$
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write ( $t_{\text{wcs}} \leq t_{\text{wcs}}(\text{min})$ or $t_{\text{cWD}} \geq t_{\text{cWD}}(\text{min})$ )
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{\text{RAS}}$ -only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{\text{CAS}}$ disturb.

Fig. 3 – CURRENT WAVEFORM ( $V_{\text{CC}} = 5.5\text{V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$ )



## TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

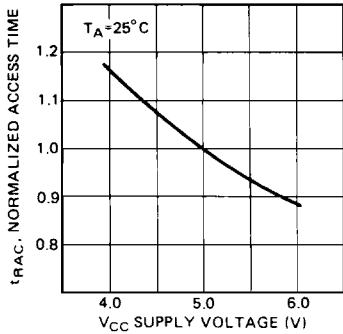


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

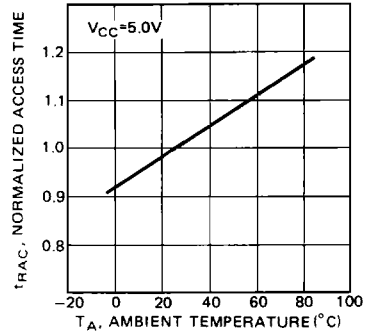


Fig. 6 – OPERATING CURRENT vs CYCLE RATE

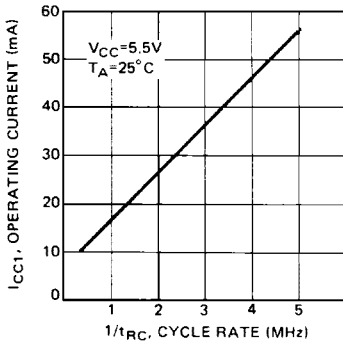


Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

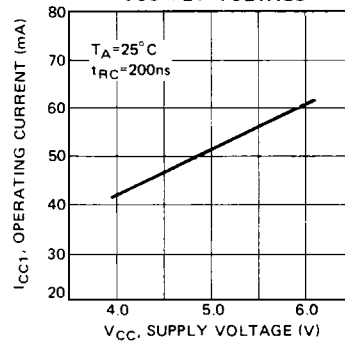


Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

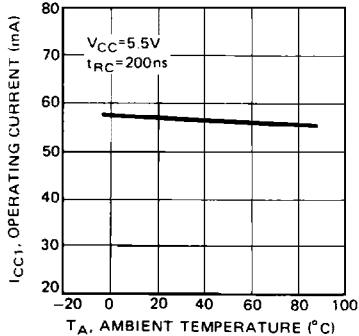
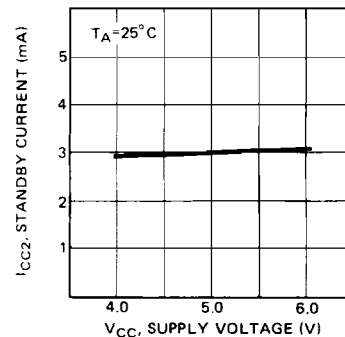


Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE



1

1

Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

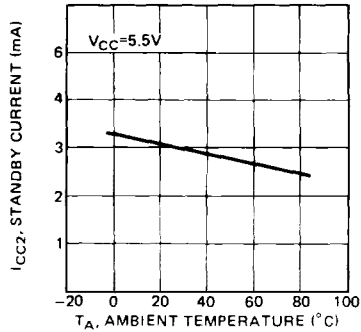


Fig. 11 – REFRESH CURRENT 1 vs CYCLE RATE

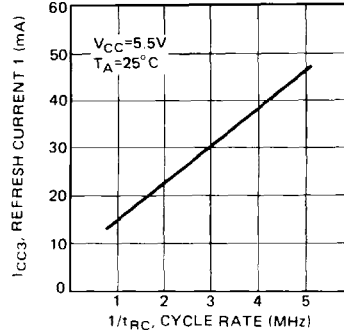


Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

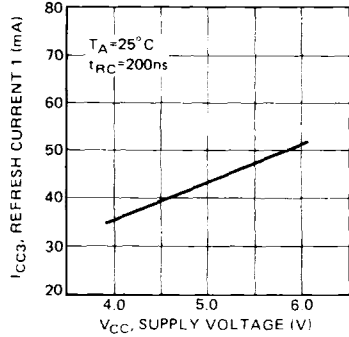


Fig. 13 – NIBBLE MODE CURRENT vs CYCLE RATE

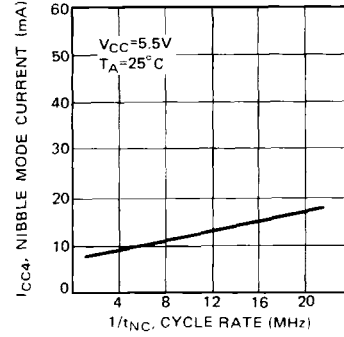


Fig. 14 – NIBBLE MODE CURRENT vs SUPPLY VOLTAGE

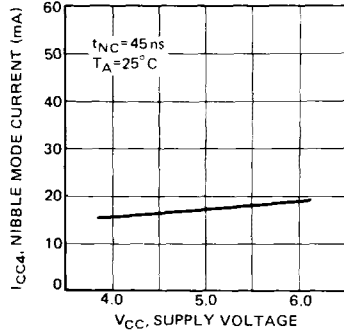


Fig. 15 – REFRESH CURRENT 2 vs CYCLE RATE

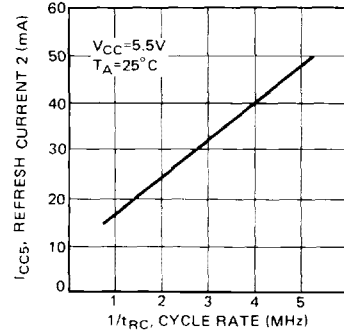


Fig. 16 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

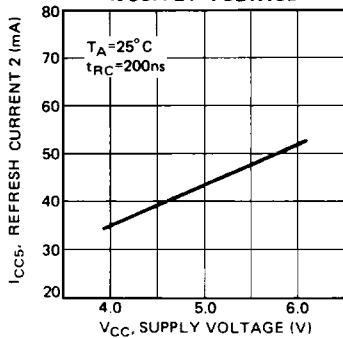


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

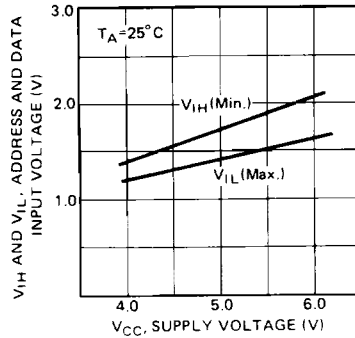


Fig. 18 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

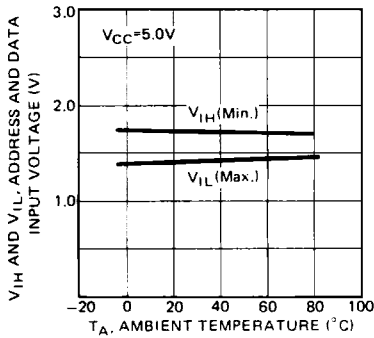


Fig. 19 –  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  AND  $\overline{\text{WE}}$  INPUT VOLTAGE vs SUPPLY VOLTAGE

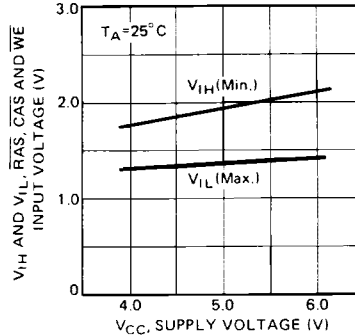


Fig. 20 –  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  AND  $\overline{\text{WE}}$  INPUT VOLTAGE vs AMBIENT TEMPERATURE

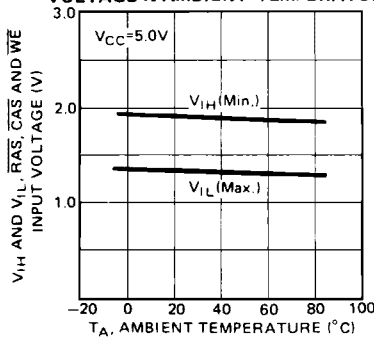
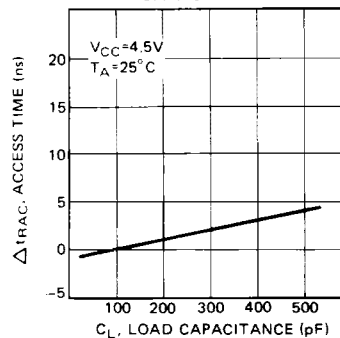


Fig. 21 – ACCESS TIME vs LOAD CAPACITANCE



1

1

Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

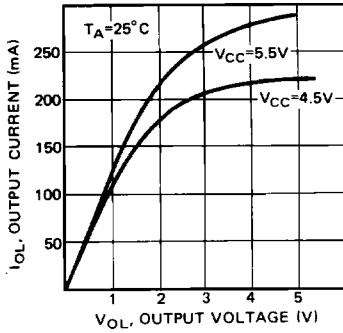


Fig. 23 – OUTPUT CURRENT vs OUTPUT VOLTAGE

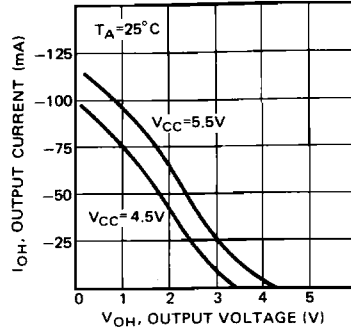


Fig. 24 – CURRENT WAVEFORM DURING POWER UP

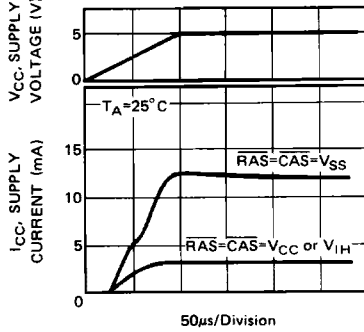
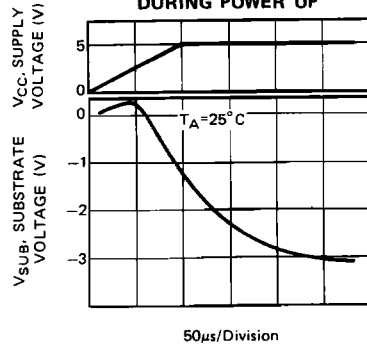


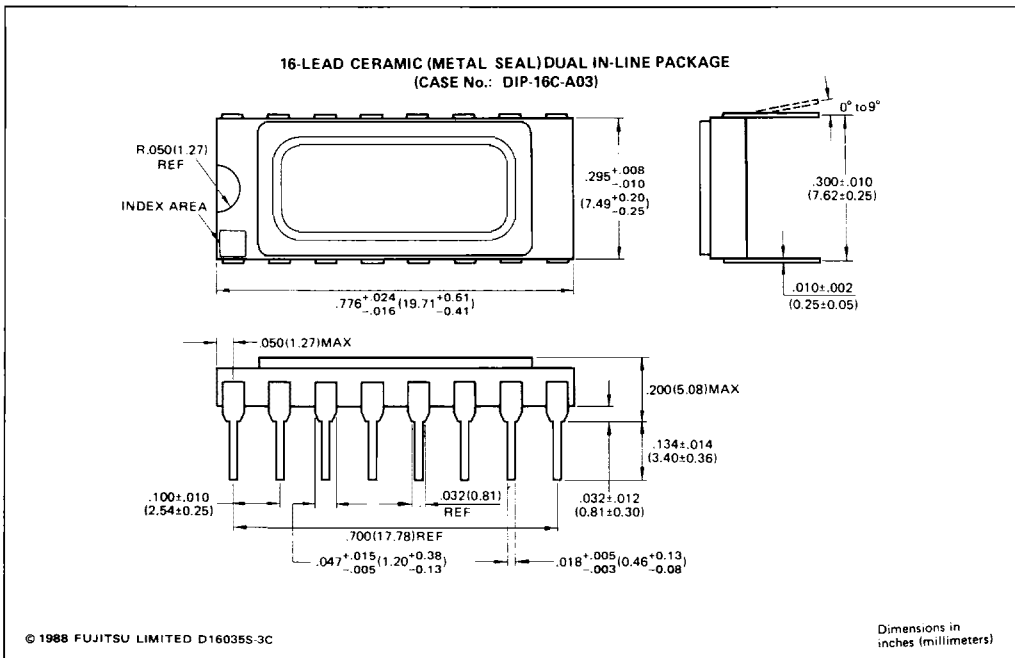
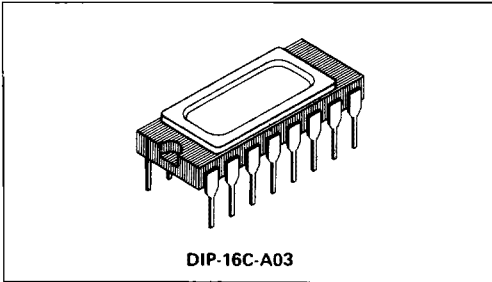
Fig. 25 – SUBSTRATE VOLTAGE DURING POWER UP



## PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)

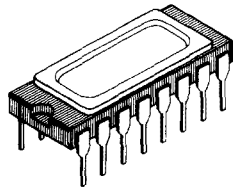
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MB81257-10  
 MB81257-12  
 MB81257-15

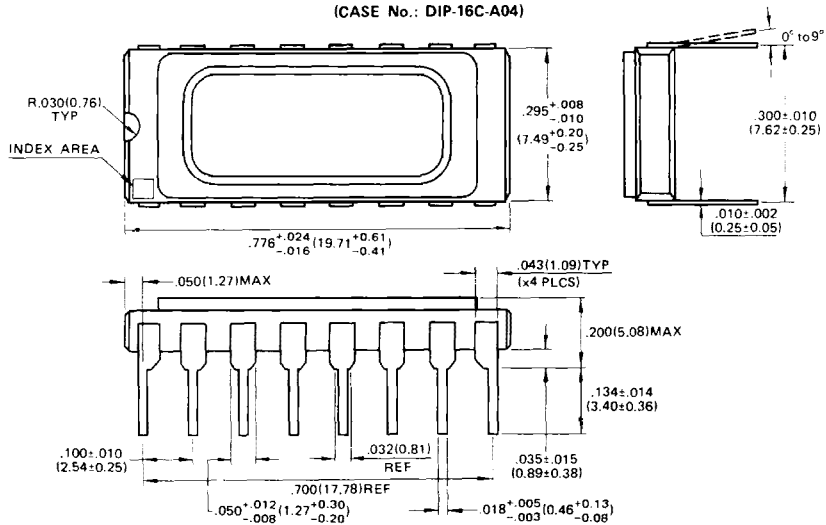
## PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A04

### 16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE (CASE No.: DIP-16C-A04)



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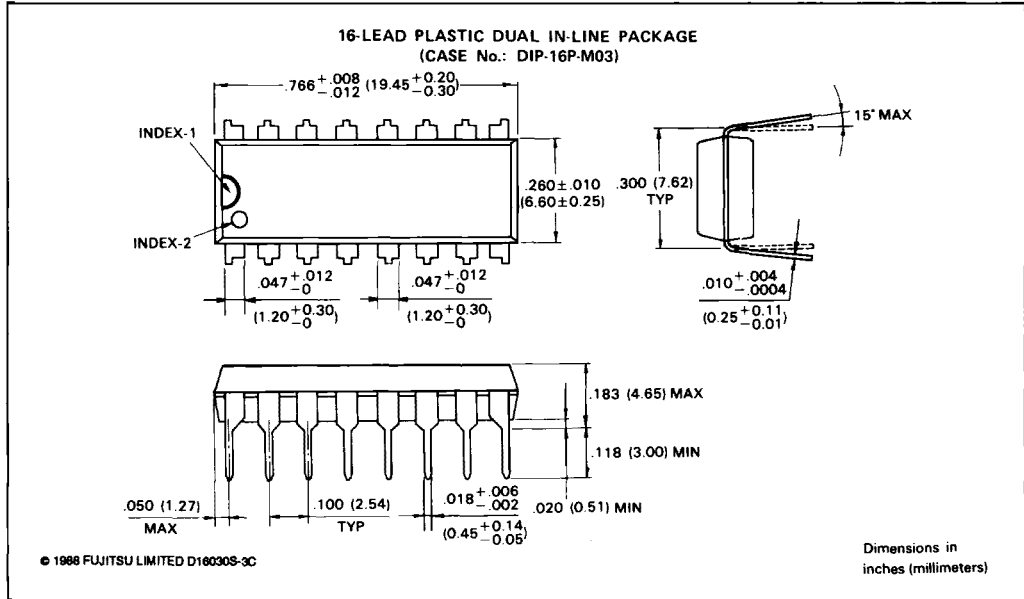
Dimensions in  
 inches (millimeters)



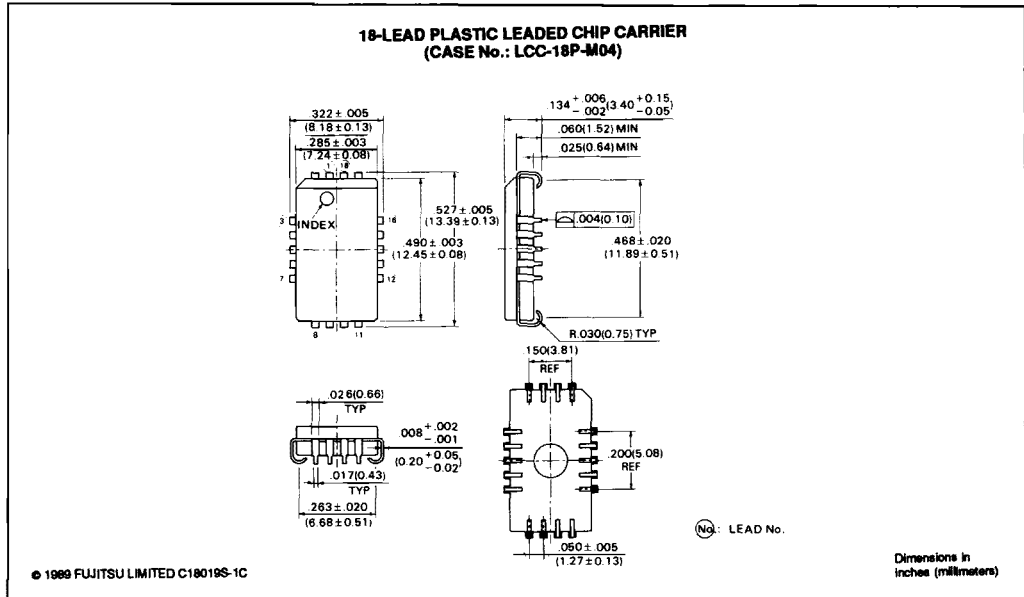
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## PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)

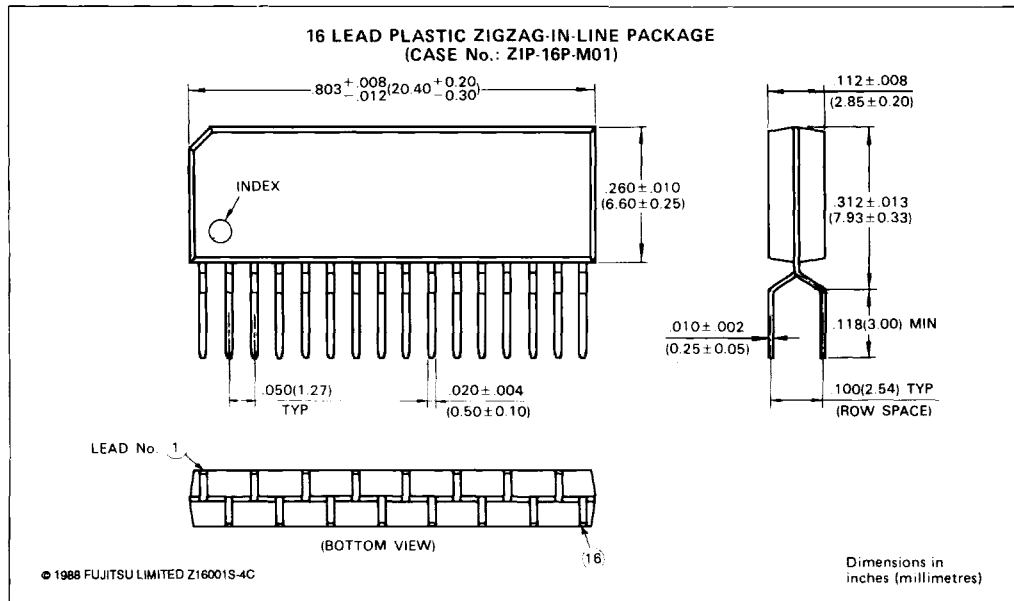
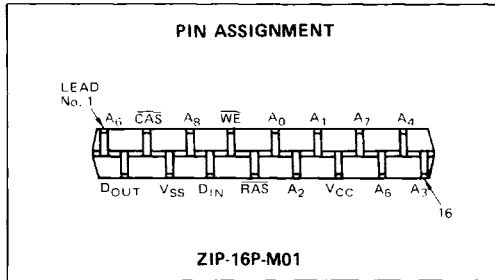


Standard 18-pin Plastic LCC (Suffix: -PD)



## PACKAGE DIMENSIONS

Standard 16-Pin Plastic ZIP (Suffix: -PSZ)



MB81257-10  
 MB81257-12  
 MB81257-15

## PACKAGE DIMENSIONS

Standard 18-pin Ceramic LCC (Suffix: -TV)

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