

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54LS385, SN74LS385 QUADRUPLE SERIAL ADDERS/SUBTRACTORS

D2412, NOVEMBER 1977 — REVISED MARCH 1988

- Four Synchronous Elements in a Single 20-Pin Package
- Buffered Clock and Direct Clear Inputs
- Independent Two's-Complement Addition/Subtraction

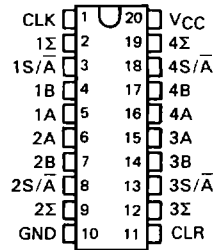
description

The 'LS385 is a general purpose adder/subtractor and is particularly useful as a companion part to the SN54LS384/SN74LS384 serial/parallel two's-complement multiplier. The 'LS385 contains four independent adder/subtractor elements with common clock and clear.

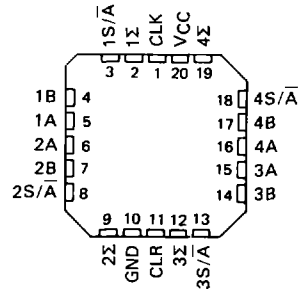
Each of the four independent sum (Σ) outputs reflects its respective A and B input as controlled by the S/ \bar{A} control. When S/ \bar{A} is high the Σ function is A minus B. When S/ \bar{A} is low the Σ function is A plus B.

When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops according to the function table.

SN54LS385 . . . J PACKAGE
SN74LS385 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS385 . . . FK PACKAGE
(TOP VIEW)



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FUNCTION TABLE

SELECTED FUNCTION	INPUTS					DATA IN CARRY FLIP-FLOP		Σ OUTPUT
	CLR	S/ \bar{A}	A	B	CLK	BEFORE \uparrow	AFTER \uparrow	AFTER \uparrow
Clear	L	L	X	X	X	L	L	L
	L	H	X	X	X	H	H	L
Add	H	L	L	L	\uparrow	L	L	L
	H	L	L	L	\uparrow	H	L	H
	H	L	L	H	\uparrow	L	L	H
	H	L	L	H	\uparrow	H	H	L
	H	L	H	L	\uparrow	L	L	H
	H	L	H	L	\uparrow	H	H	L
	H	L	H	H	\uparrow	L	L	H
Subtract	H	H	L	L	\uparrow	L	L	H
	H	H	L	L	\uparrow	H	H	L
	H	H	L	H	\uparrow	L	L	L
	H	H	L	H	\uparrow	H	L	H
	H	H	H	L	\uparrow	L	H	L
	H	H	H	L	\uparrow	H	H	H
	H	H	H	H	\uparrow	L	L	H

H = high level, L = low level, X = irrelevant,
 \uparrow = transition from low to high level at the clock input

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

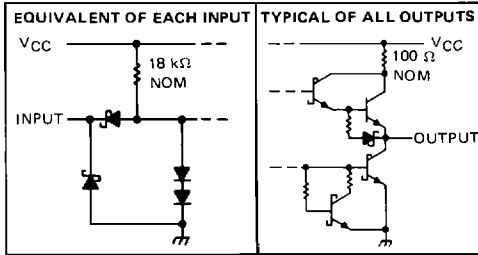
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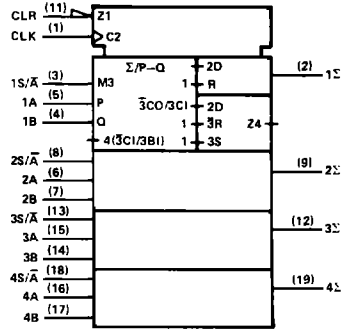
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SN54LS385, SN74LS385 QUADRUPLE SERIAL ADDERS/SUBTRACTORS

schematics of inputs and outputs



logic symbol†

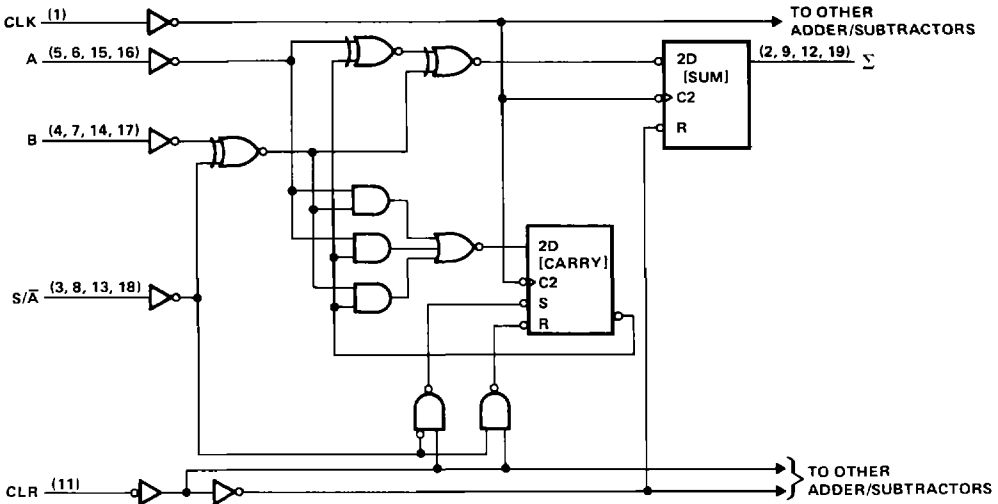


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12

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logic diagram (each adder/subtractor, positive logic)



Pin numbers shown are for DW, J, or N packages

SN54LS385, SN74LS385 QUADRUPLE SERIAL ADDERS/SUBTRACTORS

recommended operating conditions

	SN54LS385			SN74LS385			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	16			16			ns
Setup time, t_{su}	10			10			ns
Hold time, t_h	3			3			ns
Operating free-air temperature, T_A	-55	125		0	70		$^{\circ}$ C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS385			SN74LS385			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$			$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25 0.4	0.25 0.4	0.35 0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2		48	75		48	75	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

[§] Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				30	40		MHz
t_{PLH}	Clock	Σ	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 3		14	22	ns
t_{PHL}					18	27	
t_{PHL}	Clear	Σ			18	30	ns
t_{PHL}							

NOTE 3: Load circuits and voltage waveforms are shown in Section 1

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