

# **ID240D02**

Flash Memory Card  
2M

(Model No.: ID240D02)

Spec No.: EL104048

Issue Date: April 7, 1998

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- Machine tools
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● Please direct all queries regarding the products covered herein to a sales representative of the company.

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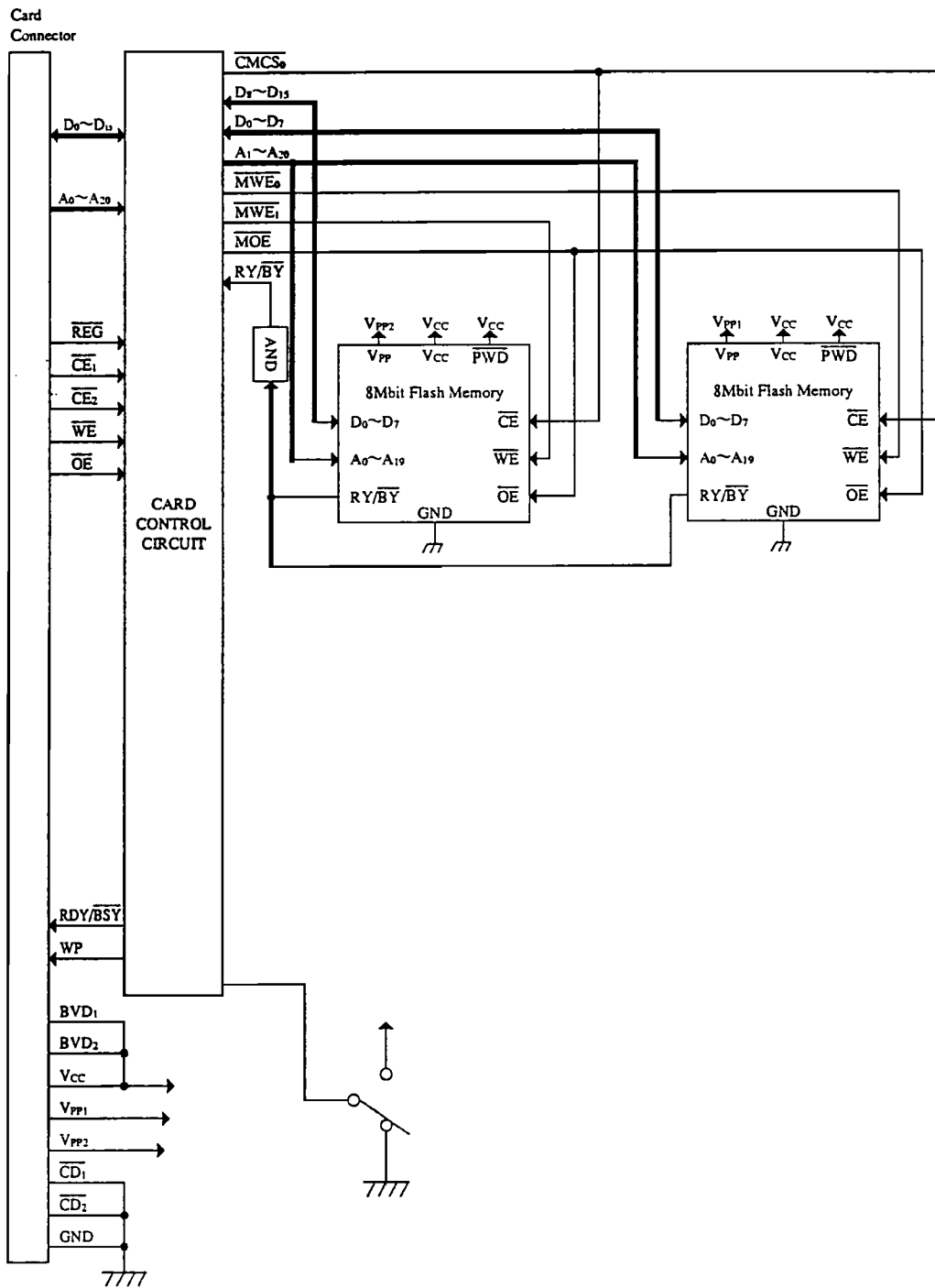
## 1. General Descriptions

The SHARP ID240D02, which panel design is SHARP standard, is a 2MB Flash Memory PC Card conforms to PCMCIA Release 2.0 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

## 2. Features

- |      |   |   |
|------|---|---|
| 2.1  | Type                                      | 2MB Flash Memory Card<br>(Conforms to PCMCIA Rel.2.0)   |
| 2.2  | Memory Capacity                           |   |
|      | Common Memory                             | 2M words×8 bits or 1M words×16 bits   |
|      | Attribute Memory                          | No EEPROM Model<br>(5 words×8 bits read only in card's control circuit)   |
|      | Note)                                     | We have another type of attribute memory as follows.<br>2k words×8 bits read/write. Sample card name: ID240D01.<br>Customers can choose one model from two. |
| 2.3  | Supply Voltage                            |   |
|      | Read Cycle                                | $V_{CC}=5\pm 0.5V$ , $V_{PP1}$ , $V_{PP2}=0\sim 1.5V$   |
|      | Read/Program/Erase Cycle                  | $V_{CC}=5\pm 0.5V$ , $V_{PP1}$ , $V_{PP2}=12.0V\pm 0.6V$  |
| 2.4  | Erase Unit                                | Block<br>(64k bytes/byte access, 128k bytes/word access)  |
| 2.5  | Program/Erase Cycles                      | 100,000 cycles  |
| 2.6  | Interface                                 | Parallel I/O Interface  |
| 2.7  | Function Table                            | See Function Table in page. 6   |
| 2.8  | External Dimensions                       | 54×85.6×3.3 mm  |
| 2.9  | Pin Connections                           | See Pin Connections in page. 4  |
| 2.10 | Type of Connector                         | Conforms to PCMCIA Re1.2.0 Card Use Connector<br>(Card connector: JC20-J68S-NB3 JAE, FCN-568J068-G/0 Fujitsu<br>or ICM-C68S-TS13-5035A JST)                 |
| 2.11 | Average Weight                            | 30g   |
| 2.12 | Operating Temp Range                      | 0 to 60°C   |
| 2.13 | Storage Temp Range                        | -20 to 65°C   |
| 2.14 | External Appearance                       | External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales.  |
| 2.15 | Manufacturer's Code                       | The manufacturer's code shall be printed on the memory card directly or on the seal which is then attached to the memory card.                              |
| 2.16 | Brand Name                                | The user's brand name will be used.   |
| 2.17 | Not designed or rated radiation hardened. |   |

## 3. Block Diagram



## 4. Pin Connections

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	18	V <sub>PP1</sub>	35	GND	52	V <sub>PP2</sub>
2	D <sub>3</sub>	19	A <sub>16</sub>	36	$\overline{CD}_1$	53	A <sub>22</sub> (NC)
3	D <sub>4</sub>	20	A <sub>15</sub>	37	D <sub>11</sub>	54	A <sub>23</sub> (NC)
4	D <sub>5</sub>	21	A <sub>12</sub>	38	D <sub>12</sub>	55	A <sub>24</sub> (NC)
5	D <sub>6</sub>	22	A <sub>7</sub>	39	D <sub>13</sub>	56	A <sub>25</sub> (NC)
6	D <sub>7</sub>	23	A <sub>6</sub>	40	D <sub>14</sub>	57	NC
7	$\overline{CE}_1$	24	A <sub>5</sub>	41	D <sub>15</sub>	58	NC
8	A <sub>10</sub>	25	A <sub>4</sub>	42	$\overline{CE}_2$	59	NC
9	$\overline{OE}$	26	A <sub>3</sub>	43	NC	60	NC
10	A <sub>11</sub>	27	A <sub>2</sub>	44	NC	61	REG
11	A <sub>9</sub>	28	A <sub>1</sub>	45	NC	62	BVD <sub>2</sub>
12	A <sub>8</sub>	29	A <sub>0</sub>	46	A <sub>17</sub>	63	BVD <sub>1</sub>
13	A <sub>13</sub>	30	D <sub>0</sub>	47	A <sub>18</sub>	64	D <sub>8</sub>
14	A <sub>14</sub>	31	D <sub>1</sub>	48	A <sub>19</sub>	65	D <sub>9</sub>
15	$\overline{WE}/\overline{PGM}$	32	D <sub>2</sub>	49	A <sub>20</sub>	66	D <sub>10</sub>
16	RDY/ $\overline{BSY}$	33	WP	50	A <sub>21</sub> (NC)	67	$\overline{CD}_2$
17	V <sub>CC</sub>	34	GND	51	V <sub>CC</sub>	68	GND

## Pin Descriptions :

D <sub>0</sub> ~D <sub>7</sub>	Data Bus (Input/Output)
D <sub>3</sub> ~D <sub>15</sub>	Data Bus (Input/Output)
A <sub>0</sub> ~A <sub>20</sub>	Address Bus (Input)
$\overline{CE}_1$ , $\overline{CE}_2$	Card Enable (Input)
$\overline{OE}$	Output Enable (Input)
$\overline{WE}/\overline{PGM}$	Write Enable/Program (Input)
$\overline{CD}_1$ , $\overline{CD}_2$	Card Detect (Output) (Card Inserted Detection Signal)
WP	Write Protect (Output) (in write protect mode, the WP output signal is "HIGH")
V <sub>PP1</sub>	Program/Erase Power Supply (Even Byte)
V <sub>PP2</sub>	Program/Erase Power Supply (Odd Byte)
REG	Register Select (Input)
BVD <sub>1</sub> , BVD <sub>2</sub>	Battery Voltage Detect (Always "HIGH")
RDY/ $\overline{BSY}$	Ready/Busy (Output)

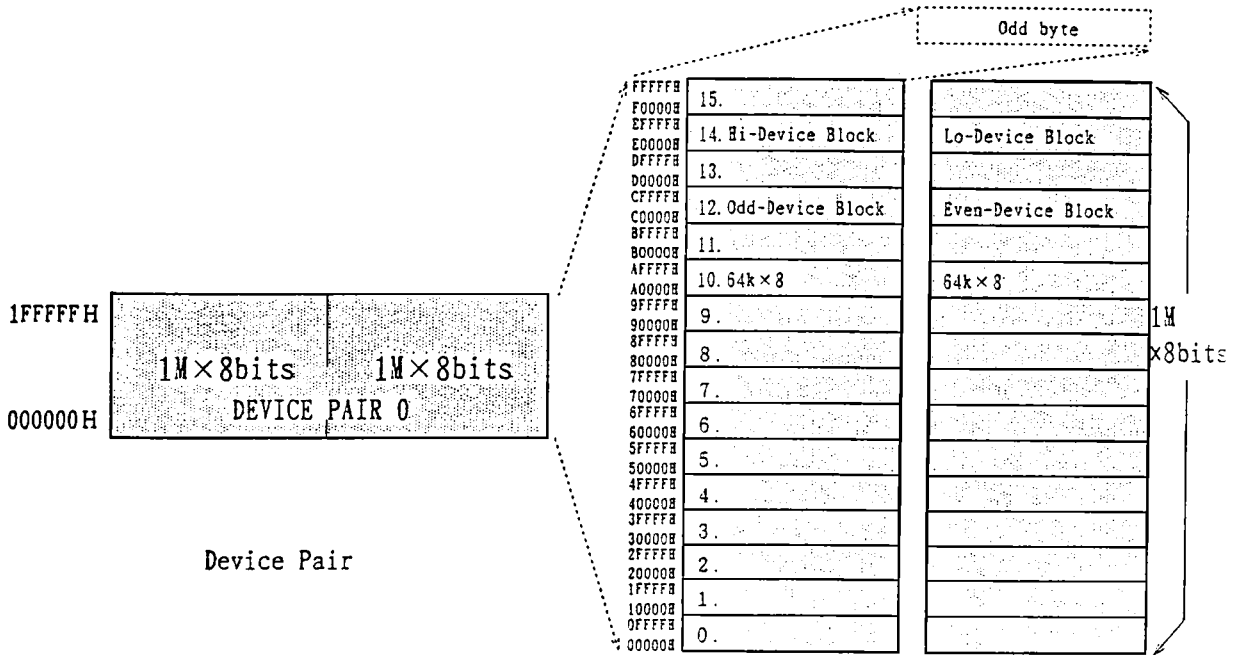
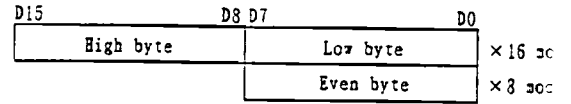
## 5. Function

### 5.1 Memory Block

5.1.1 Memory Configuration      8Mbits Flash Memory × 2 Devices.

5.1.2 Memory Erase Unit          Block Erase

Block:	Byte Mode	64k bytes
	Word Mode	128k bytes



Block Pair

## 5.2 Function Table

$\overline{CE}_1$	$\overline{CE}_2$	$A_0$	$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	$V_{PPI}$	$V_{PP2}$	$V_{CC}$	Operation	$D_0-D_7$	$D_8-D_{15}$	Status
H	H	×	×	×	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$		Hi-Z	Hi-Z	Standby
L	H	L	H	L	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$	Read (×8)	Do (Even)	Hi-Z	Byte
L	H	H	H	L	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$	Read (×8)	Do (Odd)	Hi-Z	Byte
L	L	×	H	L	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$	Read (×16)	Do (Even)	Do (Odd)	Word
H	L	×	H	L	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$	Read (×8)	Hi-Z	Do (Odd)	Byte
L	×	×	×	H	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$	Output Disable	Hi-Z	Hi-Z	Byte
H	L	×	×	H	H	$V_{PPL}$	$V_{PPL}$	$V_{CC}$	Output Disable	Hi-Z	Hi-Z	Byte
L	H	L	L	H	H	$V_{PPH}$	$V_{PPX}$	$V_{CC}$	Program (×8)	Di (Even)	Don't care	Byte
L	H	H	L	H	H	$V_{PPX}$	$V_{PPH}$	$V_{CC}$	Program (×8)	Di (Odd)	Don't care	Byte
L	L	×	L	H	H	$V_{PPH}$	$V_{PPH}$	$V_{CC}$	Program (×16)	Di (Even)	Di (Odd)	Word
H	L	×	L	H	H	$V_{PPX}$	$V_{PPH}$	$V_{CC}$	Program (×8)	Don't care	Di (Odd)	Byte
L	H	L	H	L	H	$V_{PPH}$	$V_{PPX}$	$V_{CC}$	Verify (×8)	Do (Even)	Hi-Z	Byte
L	H	H	H	L	H	$V_{PPX}$	$V_{PPH}$	$V_{CC}$	Verify (×8)	Do (Odd)	Hi-Z	Byte
L	L	×	H	L	H	$V_{PPH}$	$V_{PPH}$	$V_{CC}$	Verify (×16)	Do (Even)	Do (Odd)	Word
H	L	×	H	L	H	$V_{PPX}$	$V_{PPH}$	$V_{CC}$	Verify (×8)	Hi-Z	Do (Odd)	Byte
L	H	H	L	L	H	$V_{PPH}$	$V_{PPX}$	$V_{CC}$	*1 Prohibited	—	—	—
L	H	L	L	L	H	$V_{PPX}$	$V_{PPH}$	$V_{CC}$	*1 Prohibited	—	—	—
L	L	×	L	L	H	$V_{PPH}$	$V_{PPH}$	$V_{CC}$	*1 Prohibited	—	—	—
H	L	×	L	L	H	$V_{PPX}$	$V_{PPH}$	$V_{CC}$	*1 Prohibited	—	—	—

\*1. Do not use this mode as it will result in write errors.

H : High                      L : Low                      × : Don't Care  
 Di : Input Data              Do : Output Data          Hi-Z : High Impedance  
 $V_{CC}$  : 4.5 ~ 5.5V               $V_{PPL}$  : 0.0 ~ 1.5V           $V_{PPH}$  : 11.4 ~ 12.6V  
 $V_{PPX}$  :  $V_{PPL}$  or  $V_{PPH}$

Caution: When the write Protect switch is in protect-mode, the WP signal is "HIGH" and write operation are not allowed.

## 5.3 Software Command (8/16 Bits Operation ( ) : 16 Bits Operation)

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle			
		Operation	Address	Data	Operation	Address	Data Input	Data Output
Read Array/Reset	1	Write	RA	FFH/ (FFFFH)	—	—	—	—
Read Intelligent Identifier	3	Write	DA	90H/ (9090H)	Read	IA	—	IID
Read Status Register	2	Write	DA	70H/ (7070H)	Read	DA	—	SRD
Clear Status Register	1	Write	DA	50H/ (5050H)	—	—	—	—
Erase Setup/Erase Confirm	2	Write	BA	20H/ (2020H)	Write	BA	D0H/ (D0D0H)	—
Erase Suspend/Erase Resume	2	Write	BA	B0H/ (B0B0H)	Write	BA	D0H/ (D0D0H)	—
Byte Write Setup/Write	2	Write	WA	40H/ (4040H)	Write	WA	WD	—
Alternate Byte Write Setup/Write	2	Write	WA	10H/ (1010H)	Write	WA	WD	—

Note) 1. This Table shows the basic form of Erase, Verify and Program Verify.

Refer Programming Flowchart, Erase Algorithm in detail.

2. Bus operations are defined in function table in page.

3. IA : Device Identifier Address      IID : Device Identifier Data

	DA	IA			IID	
		8Bits (Even Device)	8Bits (Odd Device)	16Bits	Byte (8Bits)	Word (16Bits)
Manufacturer Code	000000H~1FFFFFFH	000000H	000001H	000000H	89H	8989H
Device Code	000000H~1FFFFFFH	000002H	000003H	000001H	A2H	A2A2H

RA : Read Address      WA : Write Address      WD : Write Data

DA : Device Address (Any Address in device is acceptable.)

BA : Erase Block Address (Erase Size is 64k Bytes.)

SRD : Status Register Data

4. Either 40H (4040H) or 10H (1010H) are recognized by the WSM as the Byte Write Setup Command.

a) Read Array/Reset Command(FFH/FFFFH):

By writing this command, device. Devices pair become read mode. The device remains enable for reads until the Command User Interface contents are altered.

b) Intelligent Identifier Command(90H/9090H):

After writing this command into the Command User Interface, a read cycle retrieves the manufacturer Code and device Code. To terminate the Operation, it is necessary to write another valid command into the register.

c) Read Status Register Command(70H/7070H):

By Writing this command, the Status Register may be read at any time to determine when a byte or block erase operation is complete, and whether that operation completed successfully.

Refer to Status Register definition in page. 9. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface.

d) Clear Status Register Command(50H/5050H):

Status bits which show error, the Erase Status (SR. 5), Byte Write Status (SR. 4) bits and the  $V_{PP}$  Status bit (SR. 3) can be reset by the Clear Status Machine Register Command.

e) Erase Setup/Erase Command(20H/2020H)/(D0H/D0D0H): Erase is executed one block (64kB for 1 device, 128kB for 2 devices) at a time.

This command is functional when  $V_{PP} = V_{PPI}$  and an Erase Setup Command is first written to the Command User Interface, followed by the Erase Confirm Command. After that, the device automatically outputs Status Register data when read.

The CPU can detect the completion of the erase event by analyzing the output of the  $RDY/\overline{BSY}$  pin, or the WSM Status bit of the Status Register. When erase is completed, the Erase Status bit should be checked. If erase error is detected, the Status Register should be cleared.

f) Erase Suspend/Erase Resume Command(B0H/B0B0H) / (D0H/D0D0H):

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. The device continues to output Status Register data when read, after the Erase Suspend Command is written. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended.  $RDY/\overline{BSY}$  pin will also transition to  $V_{OH}$ . At this point, a Read Array Command can be written to the Command User Interface to read data from blocks other than that which is suspended.  $V_{PP}$  must remain at  $V_{PPI}$  while device is in Erase Suspend.

Erase Resume Command, at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and  $RDY/\overline{BSY}$  pin will return to  $V_{OL}$ . After the Erase Resume is written, the device automatically output Status Register data when read.

g) Byte Write Setup/Write Command(40H/4040H) or (10H/1010H):

This command is functional when  $V_{PP} = V_{PPI}$  and an Byte Write Setup Command is first written to the Command User Interface, followed by a second write specifying the address and data to be written. The WSM then take over, controlling the byte write and write verify algorithms internally. After the two command byte sequence is written to it, the device automatically outputs Status Register data when read. The CPU can detect the completion of the byte write event by analyzing the output of the  $RDY/\overline{BSY}$  pin, or the WSM Status bits of the Status Register.

## 5.4 Status Register

The memory devices in this card have Status Register which shows state of the device.

### Byte Access × 8 Bits

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0
WSMS	ESS	ES	BWS	VPPS	RFU	RFU	RFU

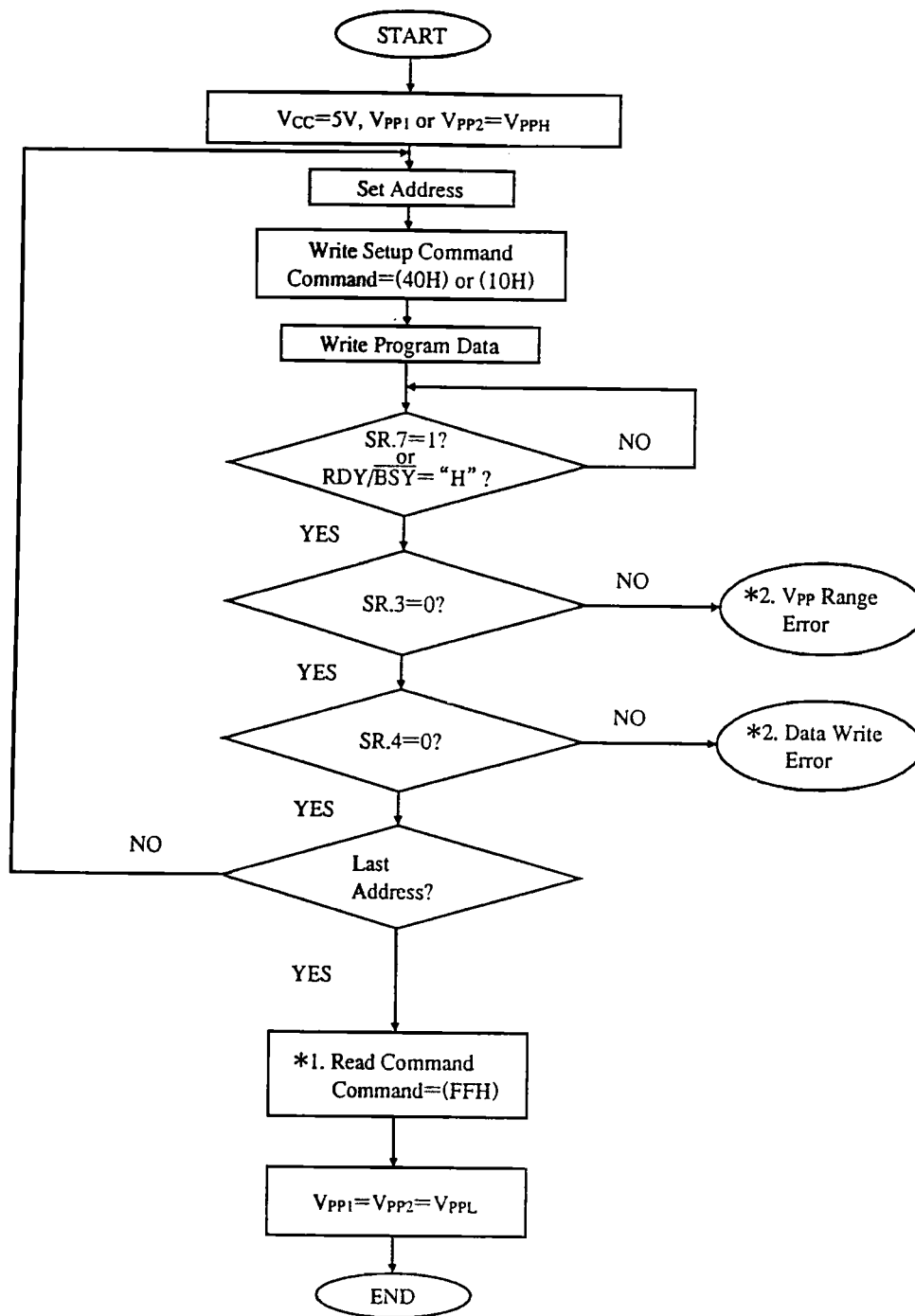
Register	Contents
SR.7=Write State Machine Status 1=Ready 0=Busy	When set "1" s, read, erase, data write is acceptable.
SR.6=Eraser Suspend Status 1=Eraser Suspend 0=Eraser In Progress/Completed	Check whether Eraser Suspend Command is executed or not.
SR.5=Eraser Status 1=Error In Block Erase 0=Successful Block Erase	Set "1" s when fail to Erase. Reset by the Clear Status Register Command.
SR.4=Byte Write Status 1=Error In Byte Write 0=Successful Byte Write	Set "1" s when fail to Byte Write. Reset by the Clear Status Register Command.
SR.3=V <sub>pp</sub> Status 1=V <sub>pp</sub> Low Detect ; Operation Abort 0=V <sub>pp</sub> OK	Set "1" s when V <sub>pp</sub> , which is needed in Byte Write or Erase operation, is below V <sub>ppH</sub> . Reset by the Clear Status Register Command.
SR.2~SR.0=Reserved for Future Use	

### Word Access × 16 bits

bit15								bit8	bit7								bit0
SR.15	SR.14	SR.13	SR.12	SR.11	SR.10	SR.9	SR.8	SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0		
Odd Byte device								Even Byte device									

## 5.5 Programming Flowchart

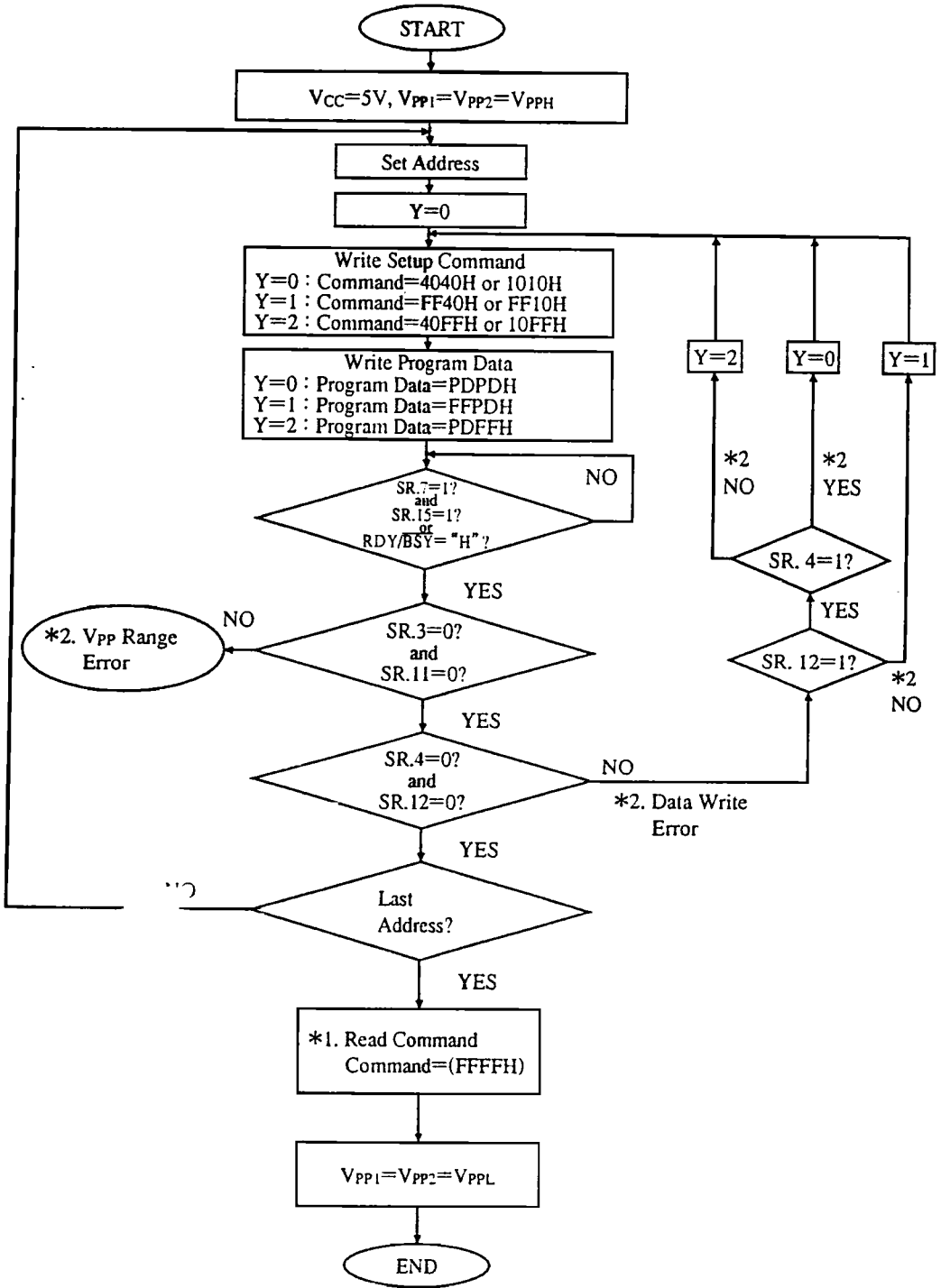
(Byte Mode)



Note) \* 1. Write FFH after the last block write operation to reset the device to Read Array Mode.

\* 2. If error is detected, clear the Status Register before attempting retry or other error recovery.

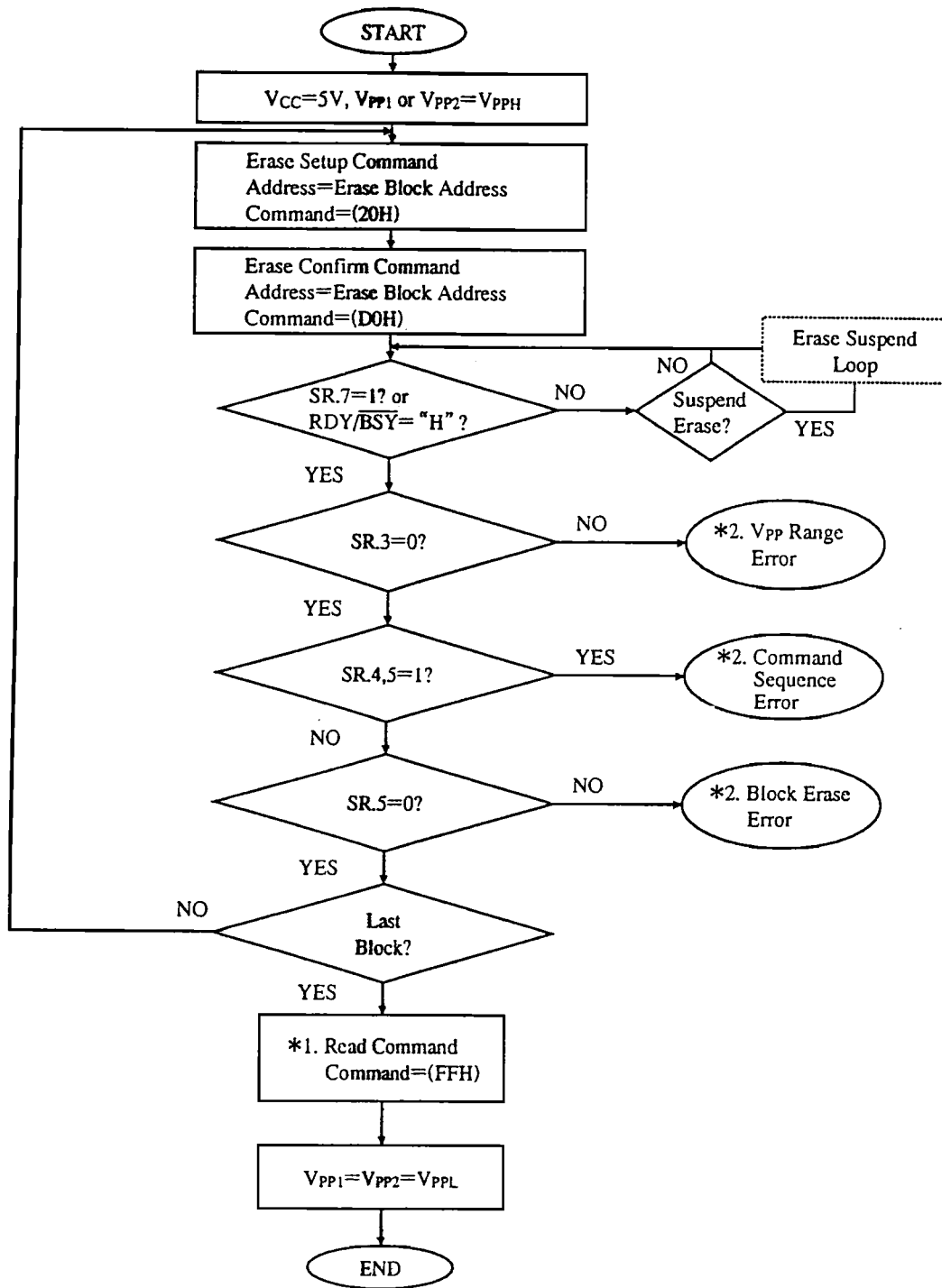
Programming Flowchart  
(Word Mode)



Note) \* 1. Write FFFFH after the last block write operation to reset the device to Read Array Mode.  
 \* 2. If error is detected, clear the Status Register before attempting retry or other error recovery.

## 5.6 Erase Algorithm

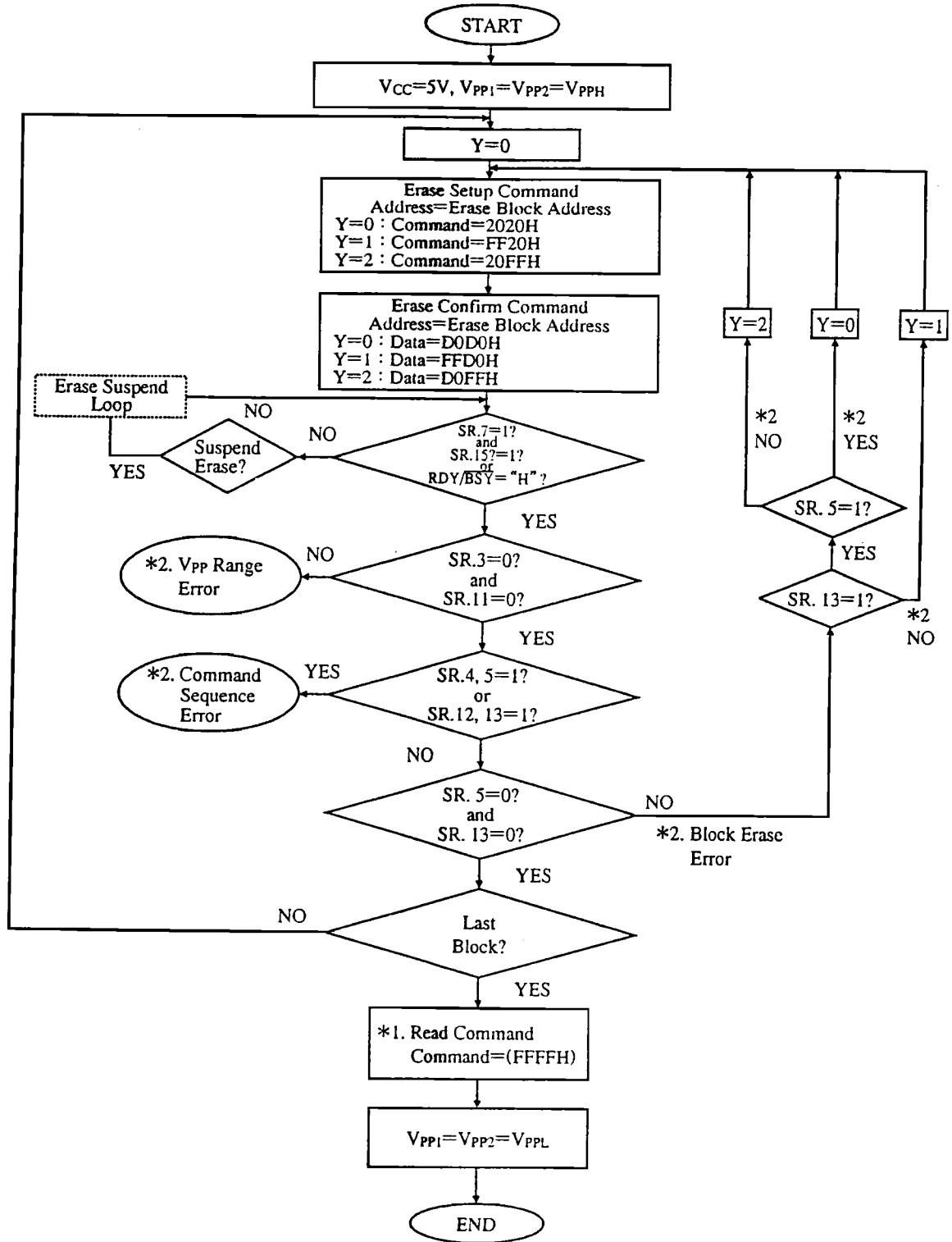
(Byte Mode)



Note) \* 1. Write FFH after the last block erase operation to reset the device to Read Array Mode.

\* 2. If error is detected, clear the Status Register before attempting retry or other error recovery.

Erase Algorithm  
(Word Mode)



Note) \* 1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.  
 \* 2. If error is detected, clear the Status Register before attempting retry or other error recovery.

## 6. Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	-0.3 to 7.0	V
Input Voltage	$V_{IN}$	-0.3 to $V_{CC} + 0.3$ (Max : 7.0)	V
Output Voltage	$V_{OUT}$	-0.3 to $V_{CC} + 0.3$ (Max : 7.0)	V
Operating Temperature	$T_{OPR}$	0 to +60	°C
Storage Temperature	$T_{STG}$	-20 to +65	°C

## 7. Recommended Operating Conditions

PARAMETER	SYMBOL	Min.	Max.	UNIT
Operating Temperature	$T_{OPR}$	0	+60	°C
Supply Voltage	$V_{CC}$	4.5	5.5	V
Input Voltage High	$V_{IH}$	3.5	$V_{CC} + 0.3$	V
Input Voltage Low	$V_{IL}$	-0.3	1.5	V

## 8. Capacitance

PARAMETER	SYMBOL	Min.	TYP	Max.	UNIT	CONDITION
Input Capacitance	$C_{IN}$	—	17	—	pF	$V_{CC} = 5V \pm 10\%$ $f = 1MHz, T_a = 25^\circ C$
Input/Output Capacitance	$C_{IO}$	—	17	—	pF	

## 9. Read Operation

### 9.1 DC Characteristics

( $V_{CC}=4.5\sim 5.5V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER		SYMBOL	Min.	TYP	Max.	UNIT	CONDITION
Operating Voltage	High Temperature	$V_{CC}$	4.5	—	5.5	V	
	Low Temperature						
Current Consumption * 1	Static Operatin Current	$I_{SB}$	—	—	2.0	mA	X16, Address : PingPong
	Dynamic Operating Current	$I_{CC}$	—	—	80		
Input Voltage	Input Voltage Level High	$V_{IH}$	3.5	—	$V_{CC}+0.3$	V	$V_{CC}=4.5\sim 5.5V$
	Input Voltage Level Low	$V_{IL}$	-0.3	—	1.5		
Input Current	$A_0\sim A_{20}$ , $D_0\sim D_{15}$	$I_{LI}$	-10	—	70	$\mu A$	$V_i = V_{CC}, 0V$
	$\overline{CE}_1$ , $\overline{CE}_2$ , $\overline{OE}$ , $\overline{WE}$ , $\overline{REG}$		-70	—	10		
Output Voltage	High	$V_{OH}$	$V_{CC}\sim 0.5$	—	—	V	$I_{OH} = -2mA (*^2)$
	Low	$V_{OL}$	—	—	0.4		$I_{OH} = -4\mu A (*^3)$
							$I_{OL} = 4mA$

PingPong : Scan the target address, with accessing the target and another address alternately.

- \* 1 (1) Static Operating Current : With the memory card's voltage at 5.5V and the  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{REG}$  signals "HIGH" ( $V_{IH} = V_{CC} - 0.2V$ ),  $A_0$  signal "LOW" ( $V_{IL} \leq 0.2V$ ) the current consumption is measured with the output open.
- (2) Dynamic Operating Current : With the memory card's  $V_{CC}$  at 5.5V and  $V_{PP1} = V_{PP2}$  at 12.6V, current consumption during access is measured with the output open.
- (Access time : 200ns) The current depends on addressing.

\* 2  $D_0\sim D_{15}$

\* 3  $BVD_1, BVD_2, RDY/\overline{BSY}, WP$

### 9.2 AC Characteristics ( $V_{CC}=4.5\sim 5.5V$ , $V_{PP}=0.0\sim 1.5V$ , $T_a=0\sim 60^\circ C$ )

Testing Conditions:

- Input Pulse Level : 0.8~3.5V
- Input Rise/Fall Time : 10ns
- Input/Output Timing Reference Level : 1.5V
- Output Load : 1TTL +  $C_L$  (100pF) (including scope and jig capacitance)

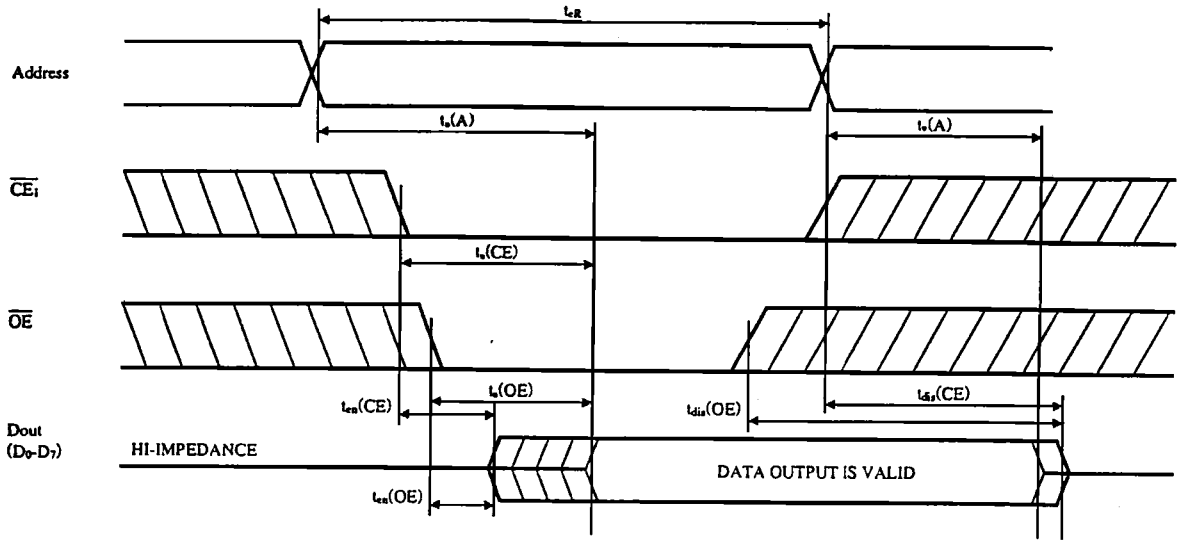
#### 9.2.1 Read Cycle

( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=0.0\sim 1.5V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER	SYMBOL	SYMBOL (PCMCIA)	Min.	Max.	UNIT
Read Cycle Time	$t_{AVAV}$	$t_{CR}$	200	—	ns
Address Access Time	$t_{AVQV}$	$t_a (A)$	—	200	
Card Enable Access Time	$t_{ELQV}$	$t_a (CE)$	—	200	
Output Enable Access Time	$t_{GLQV}$	$t_a (OE)$	—	100	
Output Disable Time from $\overline{CE}$ *	$t_{EHQV}$	$t_{dis} (CE)$	—	90	
Output Disable Time from $\overline{OE}$ *	$t_{GHQZ}$	$t_{dis} (OE)$	—	90	
Output Enable Time from $\overline{CE}$	$t_{ELQX}$	$t_{en} (CE)$	5	—	
Output Enable Time form $\overline{OE}$	$t_{GLQX}$	$t_{en} (OE)$	5	—	
Data Valid from Add Change		$t_v (A)$	0	—	

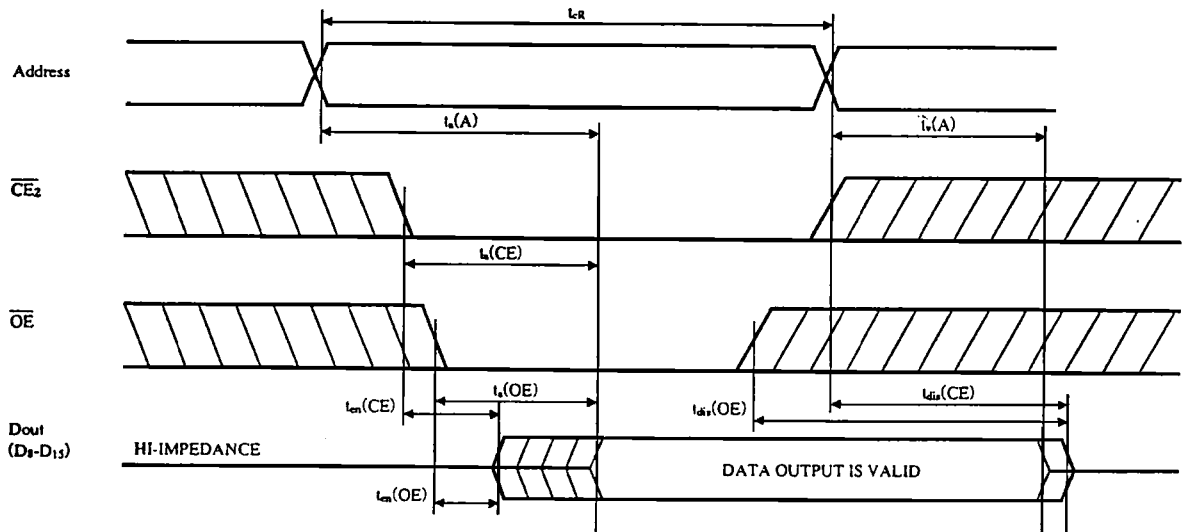
\* Time until output becomes floating. (The output voltage is not defined.)

○Read CYCLE (1) ( $\overline{CE}_2 = V_{IH}$  Fixed), 8bits Output



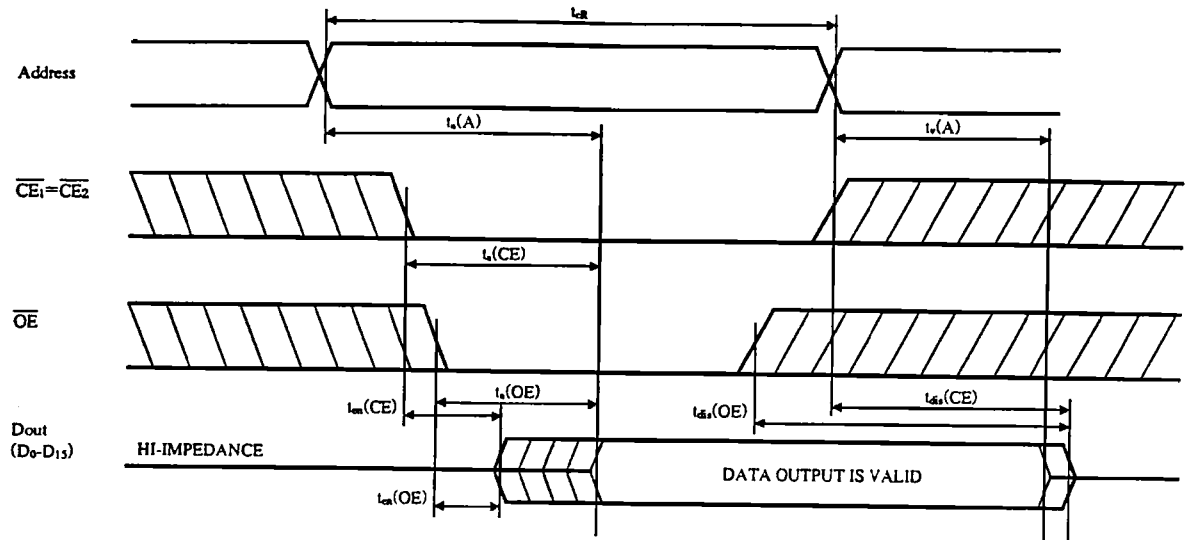
- Note) 1.  $\overline{WE} = \text{"HIGH"}$ , during a read cycle.  
 2. Either "HIGH" or "LOW" in diagonal areas.  
 3. The output data becomes valid when last interval,  $t_s(A)$ ,  $t_s(CE)$  or  $t_s(OE)$  have concluded.

○Read Cycle (2) ( $\overline{CE}_1 = V_{IH}$  Fixed), 8Bits Output



- Note) 1.  $\overline{WE} = \text{"HIGH"}$ , during a read cycle.  
 2. Either "HIGH" or "LOW" in diagonal areas.  
 3. The output data becomes valid when last interval,  $t_s(A)$ ,  $t_s(CE)$  or  $t_s(OE)$  have concluded.

○Read Cycle (3), 16Bits Output



- Note) 1.  $\overline{WE}$  = "HIGH", during a read cycle.  
 2. Either "HIGH" or "LOW" in diagonal areas.  
 3. Change  $\overline{CE}_1$  and  $\overline{CE}_2$  at the same time.  
 4. The output data becomes valid when last interval,  $t_s(A)$ ,  $t_s(CE)$  or  $t_s(OE)$  have concluded.

## 10. Programming Operation

### 10.1 DC Characteristics

( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=11.4\sim 12.6V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER	SYMBOL	Min.	Max.	UNIT	CONDITION
$V_{PP1}$ , $V_{PP2}$ operating Voltage	Read	$V_{PPL}$	0	V	
	Program	$V_{PPH}$	11.4		12.6
$V_{PP1}$ , $V_{PP2}$ operating Current ( $\times 16$ Mod)	Read	$I_{SB2}$	—	mA	Input open
	Program	$I_{PP}$	—		20
$V_{CC}$ operating Current	Standby	$I_{SB1}$	—	mA	Input open
	Program	$I_{CC}$	—		75
Input Voltage		$V_{IL}$	-0.3	V	
		$V_{IH}$	3.5		$V_{CC} + 0.3$
Output Voltage During Verify		$V_{OL}$	—	V	$I_{OL} = 4mA$
		$V_{OH}$	$V_{CC} - 0.5$		—

- Note) 1. Power on  $V_{CC}$  before power on  $V_{PP}$ , power off  $V_{CC}$  after power off  $V_{PP}$ .  
 2. Keep  $V_{PP}$  including its overshoot, below 13V.  
 3. Card insertion or removal while applying  $V_{PP}=12V$  may cause a loss of integrity.  
 4. Do not turn on or turn off during  $\overline{CE} = "LOW"$ .  
 5. If  $V_{IH}$  goes above  $V_{CC} + 0.3V$ , normal operation is not assured.

## 10.2 AC Characteristics ( $V_{CC}=4.5\sim 5.5V$ , $V_{PP}=11.4\sim 12.6V$ , $T_a=0\sim 60^\circ C$ )

Testing Conditions:

- 1) Input Pulse Level : 0.8~3.5V
- 2) Input Rise/Fall Time : 10ns
- 3) Input/Output Timing Reference Level : 1.5V
- 4) Output Load : 1TTL +  $C_L$  (100pF) (including scope and jig capacitance)

### 10.2.1 Program Cycle

$\overline{WE}$  Controlled

( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=11.4\sim 12.6V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER	SYMBOL	SYMBOL (PCMCIA)	Min.	Max.	UNIT
Write Cycle Time	$t_{AVAV}$	$t_{cw}$	200	—	ns
Address Setup Time	$t_{AVWL}$	$t_{su}(A)$	20	—	
Write Recovery Time	$t_{WHAX}$	$t_{rec}(WE)$	30	—	
Data Setup Time for $\overline{WE}$	$t_{DVWH}$	$t_{su}(D-WEH)$	60	—	
Data Hold Time	$t_{WHDX}$	$t_h(D)$	30	—	
Write Recovery Before Read	$t_{WHGL}$		10	—	
Card Enable Setup time for $\overline{WE}$	$t_{ELWH}$	$t_{su}(CE-WEH)$	140	—	
Address Setup for $\overline{WE}$	$t_{AVWH}$	$t_{su}(A-WEH)$	140	—	
Card Enable Hold Time	$t_{WHEH}$		15	—	
Write Pulse Width	$t_{WLWH}$	$t_w(WE)$	120	—	
Write Pulse Width High	$t_{WHWL}$	$t_w(WEH)$	30	—	
$\overline{WE}$ High to RDY/ $\overline{BSY}$ Going Low	$t_{WHRL}$		—	150	
Duration of write operation	$t_{WHQVI}$		4.8	—	$\mu s$
$V_{PP}$ Setup to $\overline{WE}$ Going High	$t_{VPWH}$		100	—	ns
$V_{PP}$ Hold from Valid SRD, RDY/ $\overline{BSY}$ High	$t_{QVVL}$		0	—	

$\overline{CE}$  Controlled

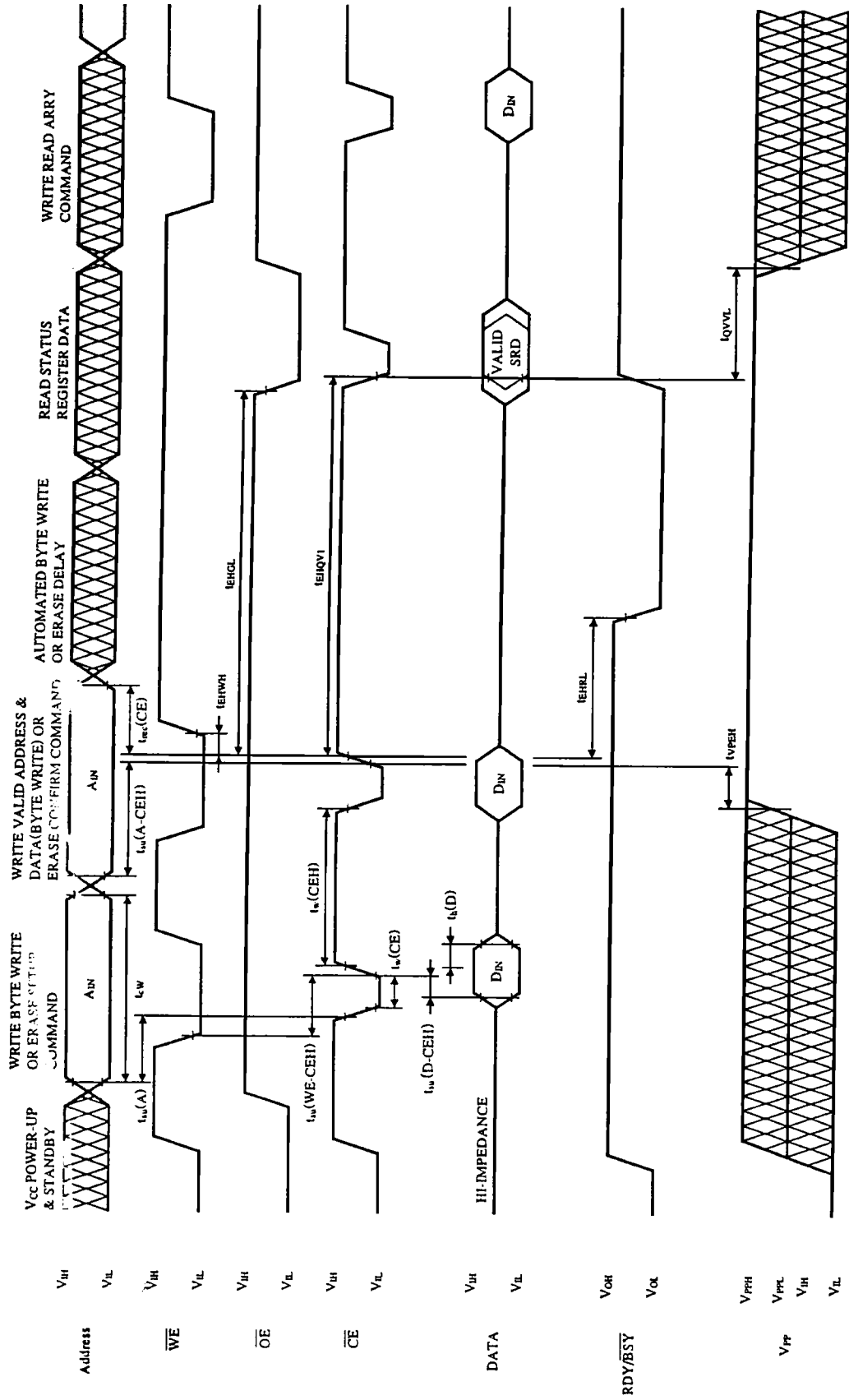
( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=11.4\sim 12.6V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER	SYMBOL	SYMBOL (PCMCIA)	Min.	Max.	UNIT
Write Cycle Time	$t_{AVAV}$	$t_{cw}$	200	—	ns
Address Setup Time	$t_{AVEL}$	$t_{su}(A)$	20	—	
Write Recovery Time	$t_{EHAX}$	$t_{rec}(CE)$	30	—	
Data Setup Time for $\overline{CE}$	$t_{DVEH}$	$t_{su}(D-CEH)$	60	—	
Data Hold Time	$t_{EHDX}$	$t_h(D)$	30	—	
Write Recovery Before Read	$t_{EHGL}$		10	—	
Write Enable Setup time for $\overline{CE}$	$t_{WLEH}$	$t_{su}(WE-CEH)$	140	—	
Address Setup for $\overline{CE}$	$t_{AVEH}$	$t_{su}(A-CEH)$	140	—	
Write Enable Hold Time	$t_{EHWL}$		0	—	
Write Pulse Width	$t_{ELEH}$	$t_w(CE)$	120	—	
Write Pulse Width High	$t_{EHEL}$	$t_w(CEH)$	30	—	
$\overline{WE}$ High to RDY/ $\overline{BSY}$ Going Low	$t_{EHRL}$		—	150	
Duration of write operation	$t_{EHQVI}$		4.8	—	$\mu s$
$V_{PP}$ Setup to $\overline{WE}$ Going High	$t_{VPEH}$		100	—	ns
$V_{PP}$ Hold from Valid SRD, RDY/ $\overline{BSY}$ High	$t_{QVVL}$		0	—	

1. Set  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{OE}$  and  $\overline{WE}$  "HIGH", when  $V_{PP}$  changes from  $V_{PPL}$  to  $V_{PPH}$  or vice versa.



## Program Cycle (CE Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

## 11. Erase Operation

### 11.1 DC Characteristics

( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=11.4\sim 12.6V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER	SYMBOL	Min.	Max.	UNIT	CONDITION
$V_{PP1}, V_{PP2}$ Operating Voltage	Read	$V_{PPL}$	0	1.5	V
	Program	$V_{PPHE}$	11.4	12.6	
$V_{PP1}, V_{PP2}$ Operating Current ( $\times 16$ Mode)	Standby	$I_{SB2}$	—	1.6	mA
	Erase	$I_{PP}$	—	20	
	Erase Suspend	$I_{PPS}$	—	1.6	
$V_{CC}$ Operating Current ( $\times 16$ Mode)	Standby	$I_{SB1}$	—	2.0	V
	Erase	$I_{CCE}$	—	75	
	Erase Suspend	$I_{CCES}$	-0.3	22	
Input Voltage	$V_{IL}$	3.5	1.5	V	I/O open
	$V_{IH}$	—	$V_{CC}+0.3$		
Output Voltage During Verify	$V_{OL}$	$V_{CC}-0.5$	0.4	V	$I_{OL}=4mA$
	$V_{OH}$	—	—		$I_{OH}=-2mA$

Note) Power on  $V_{CC}$  before power on  $V_{PP}$ , power off  $V_{CC}$  after power off  $V_{PP}$ . Keep  $V_{PP}$  including its overshoot, below 13V. Card insertion or removal while applying  $V_{PP}=12V$  may cause a loss of integrity. Do not turn on or turn off during  $\overline{CE} = "LOW"$ .

If  $V_{IH}$  goes above  $V_{CC}+0.3V$ , normal operation is not assured.

### 11.2 AC Characteristics ( $V_{CC}=4.5\sim 5.5V$ , $V_{PP}=11.4\sim 12.6V$ , $T_a=0\sim 60^\circ C$ )

Testing Conditions:

- 1) Input Pulse Level : 0.8~3.5V
- 2) Input Rise/Fall Time : 10ns
- 3) Input/Output Timing Reference Level : 1.5V
- 4) Output Load : 1TTL +  $C_L$  (100pF) (including scope and jig capacitance)

#### 11.2.1 Erase Cycle

$\overline{WE}$  Controlled

( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=11.4\sim 12.6V$ ,  $T_a=0\sim 60^\circ C$ )

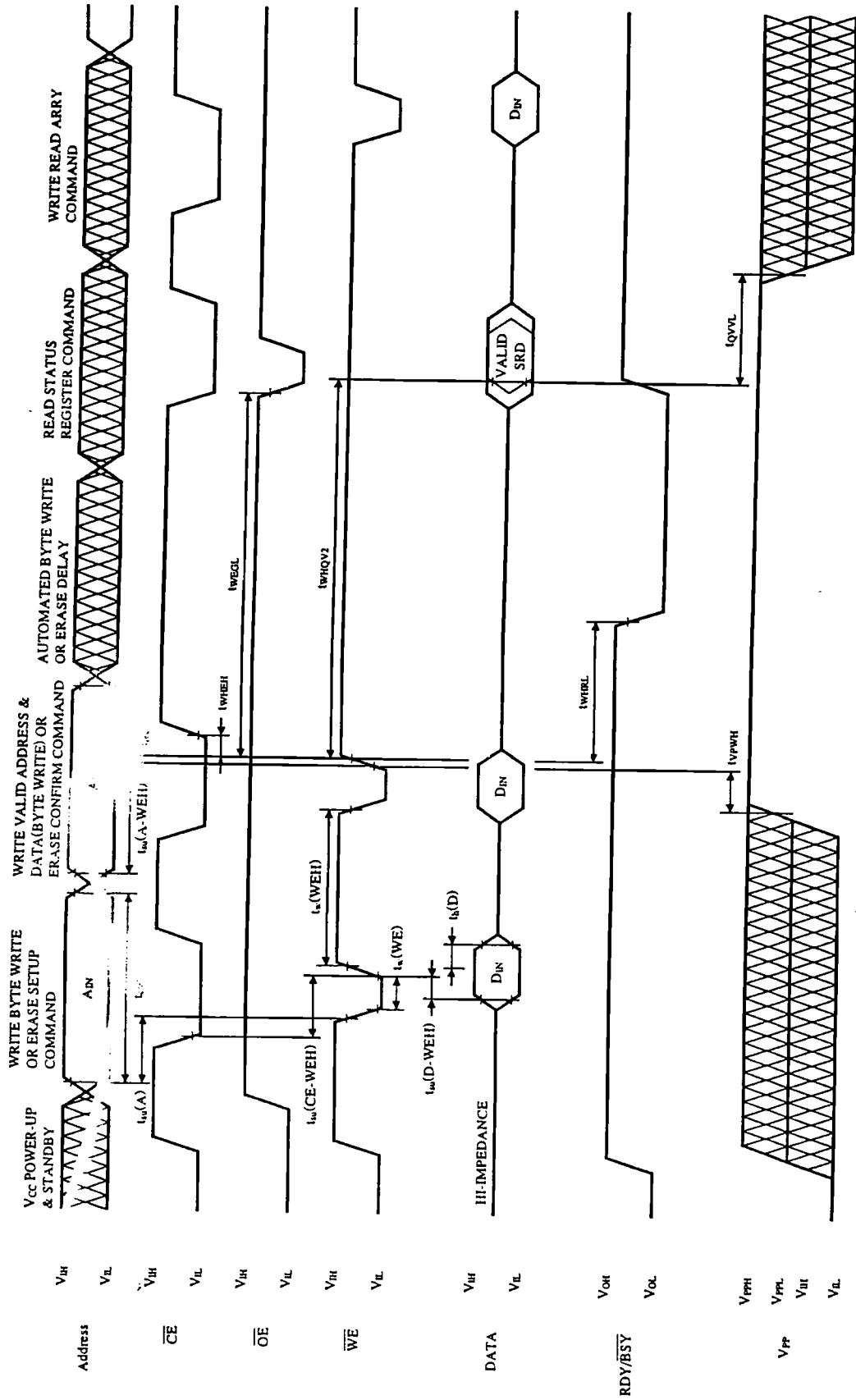
PARAMETER	SYMBOL	SYMBOL (PCMCIA)	Min.	Max.	UNIT	
Write Cycle Time	$t_{AVAV}$	$t_{cw}$	200	—	ns	
Address Setup Time	$t_{AVWL}$	$t_{su}(A)$	20	—		
Write Recovery Time	$t_{WHAX}$	$t_{rec}(WE)$	30	—		
Data Setup Time for $\overline{WE}$	$t_{DVWH}$	$t_{su}(D-WEH)$	60	—		
Data Hold Time	$t_{WHDX}$	$t_h(D)$	30	—		
Write Recovery Before Read	$t_{WHGL}$		10	—		
Card Enable Setup time for $\overline{WE}$	$t_{ELWH}$	$t_{su}(CE-WEH)$	140	—		
Address Setup for $\overline{WE}$	$t_{AVWH}$	$t_{su}(A-WEH)$	140	—		
Card Enable Hold Time	$t_{WHEH}$		15	—		
Write Pulse Width	$t_{WLWH}$	$t_w(WE)$	120	—		
Write Pulse Width High	$t_{WHWL}$	$t_w(WEH)$	30	—		
$\overline{WE}$ High to RDY/ $\overline{BSY}$ Going Low	$t_{WHRL}$		—	150		
Duration of Erase operation	$t_{WHQV2}$		0.3	—		s
$V_{PP}$ Setup to $\overline{WE}$ Going High	$t_{VPWH}$		100	—		ns
$V_{PP}$ Hold from Valid SRD, RDY/ $\overline{BSY}$ High	$t_{QVVL}$		0	—		

$\overline{CE}$  Contorlled $(V_{CC}=4.5\sim 5.5V, V_{PP}=11.4\sim 12.6V, T_a=0\sim 60^{\circ}C)$ 

PARAMETER	SYMBOL	SYMBOL (JEIDA)	Min.	Max.	UNIT
Write Cycle Time	$t_{AVAV}$	$t_{cw}$	200	—	ns
Address Setup Time	$t_{AVEL}$	$t_{su} (A)$	20	—	
Write Recovery Time	$t_{EIAx}$	$t_{rec} (CE)$	30	—	
Data Setup Time for $\overline{CE}$	$t_{DVEH}$	$t_{su} (D-CEH)$	60	—	
Data Hold Time	$t_{EHDX}$	$t_h (D)$	30	—	
Write Recovery Before Read	$t_{EIGL}$		10	—	
Write Enable Setup time for $\overline{CE}$	$t_{WLEH}$	$t_{su} (WE-CEH)$	140	—	
Address Setup for $\overline{CE}$	$t_{AVEH}$	$t_{su} (A-CEH)$	140	—	
Write Enable Hold Time	$t_{EHWL}$		0	—	
Write Pulse Width	$t_{ELEH}$	$t_w (CE)$	120	—	
Write Pulse Width High	$t_{EHEL}$	$t_w (CEH)$	30	—	
$\overline{WE}$ High to RDY/ $\overline{BSY}$ Going Low	$t_{EHRL}$		—	150	
Duration of Erase operation	$t_{EHQV2}$		0.3	—	
$V_{PP}$ Setup to $\overline{WE}$ Going High	$t_{VPEH}$		100	—	ns
$V_{PP}$ Hold from Valid SRD, RDY/ $\overline{BSY}$ High	$t_{QVVL}$		0	—	

1. Set  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{OE}$  and  $\overline{WE}$  "HIGH", when  $V_{PP}$  changes from  $V_{PPL}$  to  $V_{PPH}$  or vice versa.

## ○ERASE CYCLE (WE Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase signal.

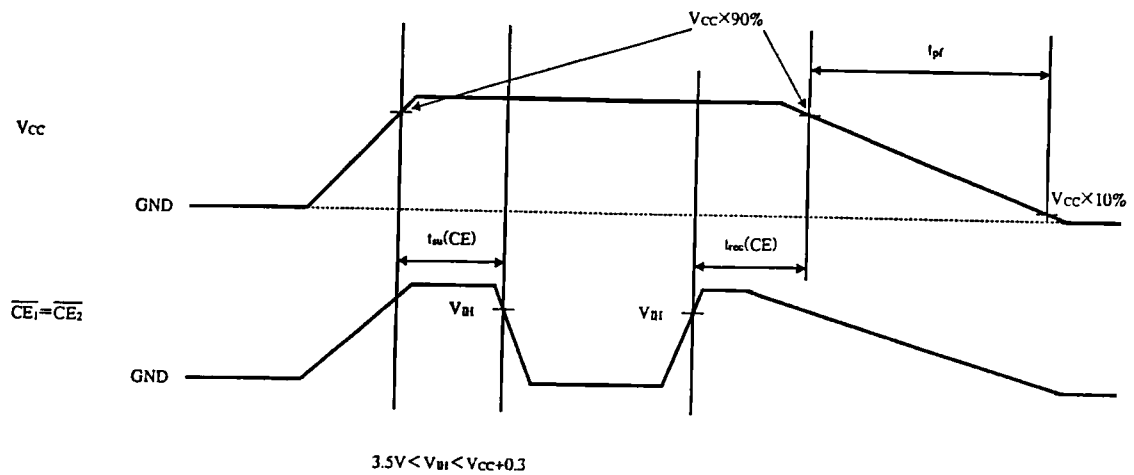


## 12. Block Erase and Data Write Characteristics

( $V_{CC}=4.5\sim 5.5V$ ,  $V_{PP}=11.4\sim 12.6V$ ,  $T_a=0\sim 60^\circ C$ )

PARAMETER	Min.	Typ.	Max.	UNIT
Block Pair Erase Time	—	1.0	10	s
Block Pair Write Time	—	0.4	2.1	

## 13. Voltage Timing ( $T_a=25^\circ C$ )



PARAMETER	SYMBOL	Min.	Max.	UNIT
$\overline{CE}$ Setup Time	$t_{su}(CE)$	4.0	—	ms
$\overline{CE}$ Recovery Time	$t_{rec}(CE)$	1.0	—	$\mu s$
$V_{CC}$ Falling Time	$t_{pf}$	3.0	300	ms

Note) 1. When  $V_{CC}$  (4.5 ~ 5.5V) is applied to the memory card and you are inserting or removing the card,  $\overline{CE}_1$ ,  $\overline{CE}_2$  should both be high-impedance. At such a time, other signal line should also be high-impedance. After inserting the memory card, do not access it during the  $\overline{CE}$  setup time (minimum of 4ms).  
(During this time, neither  $\overline{CE}_1$  nor  $\overline{CE}_2 = "LOW"$ .)

2. When  $V_{CC}$  is turn on, if the condition (for example,  $V_{CC}$  rising time. etc) is not sufficient as specified, it is possible that device's Status Register is not cleared or device not becomes to Read Array Mode. To prevent these, it is recommended that using software command, reset the Status Register or set the device to Read Array Mode.

ex.

Reset the Status Register    50H (5050H)  
Set to Read Array Mode    FFH (FFFFH)

## 14. Attribute Memory

The attribute memory holds the attribute information of the card such as the type of card, bit configuration, speed and so on.

No EEPROM Model:

Five bytes card informations in even address 0 to 8, read only in card's control circuit, with the same access timing as common memory read.

### Device Informations

Address	Tuple Code	Description
0H	01	Common Memory device information
2H	FF	There is no next tuple link
4H	52	Device Type : FLASH Memory WPS : 0 means WP switch controls the device writable or not Device Speed : 200ns
6H	06	Card Capacity : 2MB
8H	FF	The end of this tuple

Note) We have another type of attribute memory as follows,

EEPROM Model. (Model no. ID240D01): Card has 2k bytes of EEPROM attribute memory with access time 300ns maximum.

To read the attribute memory, set  $\overline{REG}$  = "LOW" and perform a read with the same access timing as common memory read.

Since only the even-numbered bytes are used, reading odd-numbered bytes will result in invalid data.

### 14.1 Attribute Memory Read/Write Function Chart

$\overline{CE}_1$	$\overline{CE}_2$	$A_0$	$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	MODE	$D_0 \sim D_7$	$D_8 \sim D_{15}$	STAATUS
H	H	X	X	X	X		High-Z	High-Z	Standby
L	H	L	H	L	L	Read ( $\times 8$ )	$D_0$ (even byte)	High-Z	Byte Access
L	H	H	H	L	L		High-Z	High-Z	Standby
L	L	X	H	L	L	Read ( $\times 8$ )	$D_0$ (even byte)	High-Z	Byte Access
H	L	X	H	L	L		High-Z	High-Z	Standby

H : High

L : Low

X : High/Low not applicable

$D_i$  : Input Data

$D_o$  : Output Data

Hi-Z : High Impedance

## 15. Specification Changes

Specifications may be changed upon discussion and agreement between both parties.

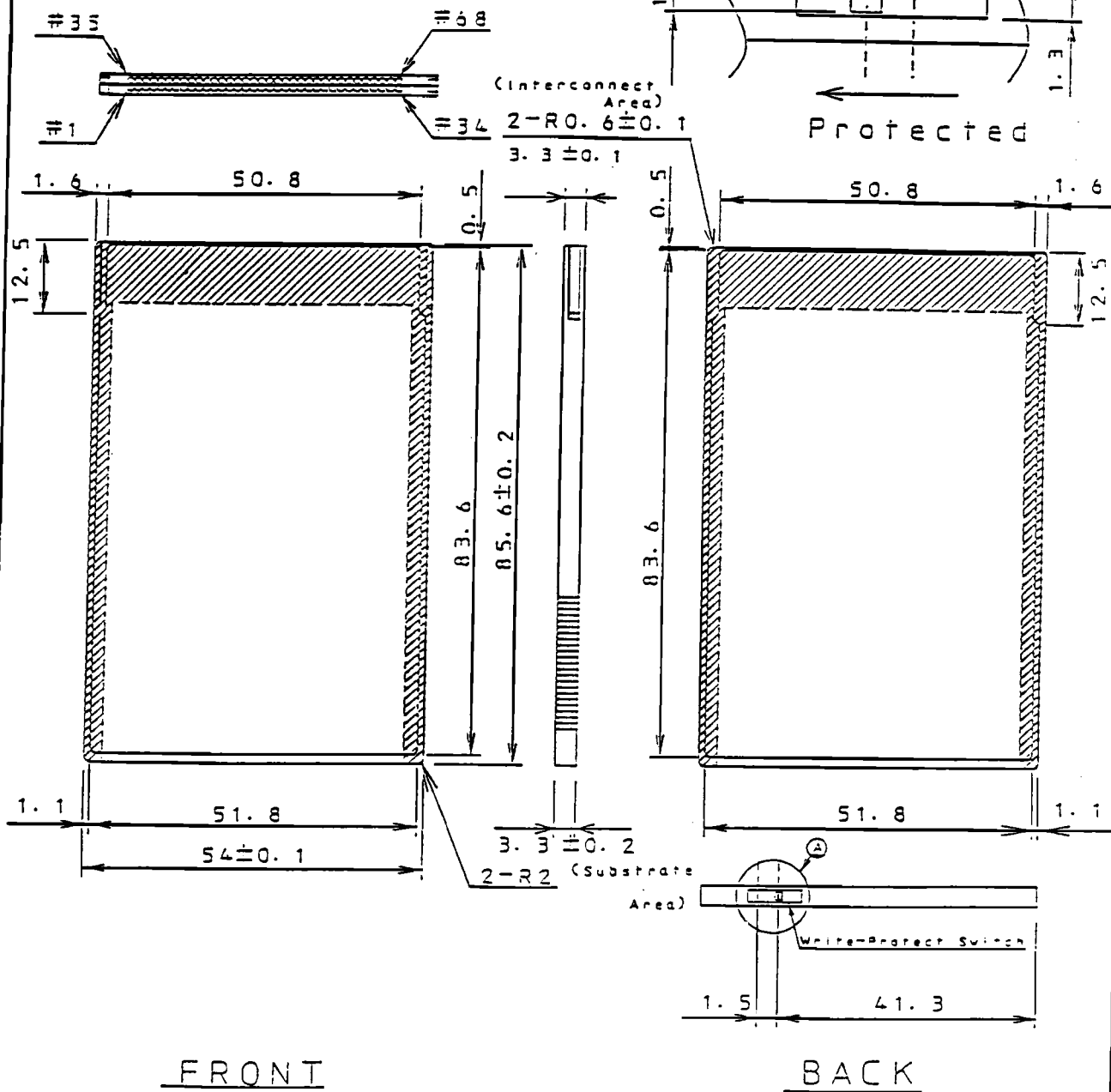
## 16. Othes Precautions

- Permanent damage occurs if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

**SHARP**

(A) ENLARGEMENT OF THE  
WRITE-PROTECT SWITCH

17. External Diagrams



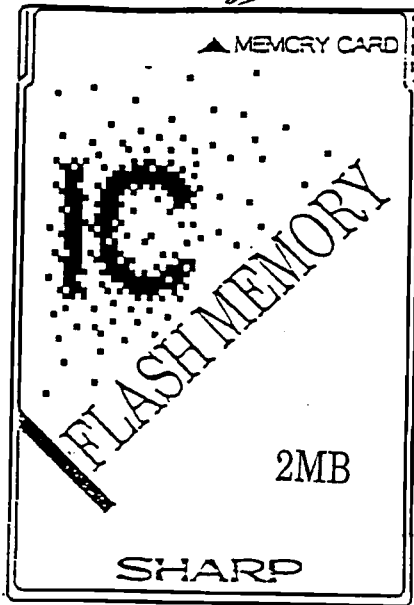
APPLICABLE		SCALE	UNIT	<input checked="" type="checkbox"/>	
MODEL		1/1	<input checked="" type="checkbox"/>	CH. DATE	REVISE
THICKNESS		MATERIAL	FINISH	NAME	
				MEMORY CARD	
DATE	1994.11.13			EXTERNAL DIAGRAM	
DESIGNER	DRW	TRACE	CHECK	APPROVE	PCMCIA Rev. 2.0 TYPE
TENRI IC GROUP					
SHARP CORPORATION					DRAWING NO. IMC001-A102



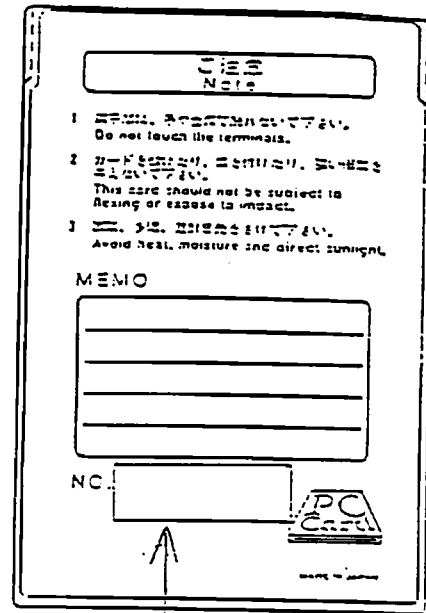
**SHARP**

19. EXTERNAL APPEARANCES

CONNECTOR SIDE

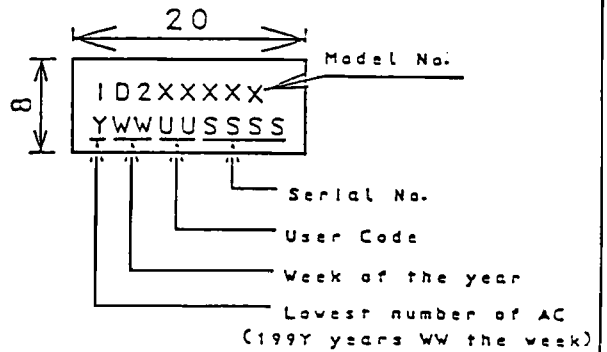


FRONT PANEL



LABELING POSITION  
BACK PANEL

LABEL SIZE AND DENOTATIONS



APPLICABLE MODEL		SCALE	UNIT	mm	CH. DATE	REVISE	CHARGE
THICKNESS	DEFERENCE	MATERIAL	FINISH		NAME		
DATE	1995. 10. 10	MEMORY CARD BUSINESS PROJECT TEAM					
<i>A. Hashimoto</i>		<i>S. Sakaki</i>		<i>S. Saito</i>		INTEGRATED CIRCUITS GROUP	
SHARP CORPORATION				DRAWING NO.			

Flash, PCMCIA Cards, Series 2, Non-Volatile, 2 MByte, ID240D02