T1 Receive Buffer

GENERAL INFORMATION

The XR-T5691 is designed to synchronize receive loop-timed T-carrier data streams to systems side timing. It is very flexible and allows interfacing of incoming data to parallel or serial TDM backplanes. It is implemented using low power CMOS technology and is available in a "skinny" 24 lead plastic DIP & 24 pin PLCC packages. This device operates in conjunction with the XR-T5690 Framer and is capable of extracting, buffering and integrating ABCD Signaling.

FEATURES

Synchronizes T1 Data Streams to System Clocks
Two Frame Buffer Depth
Frame Slip Output at Frame Boundaries
Buffer Recentering Capability
Ideal for T1 (1.544MHz) to cept (2.048MHz) rate conversion
Interfaces to Parallel and Serial Backplanes
Robbed-bit Signaling Updates During Alarm or Slip Conditions
Integration Feature "Debounces" Signaling
Pin to Pin and Functionally Compatible to DS2176

APPLICATIONS

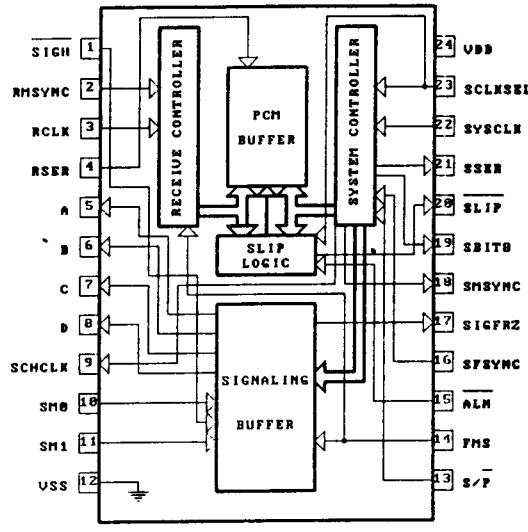
Digital Trunks
Drop and Insert Equipment
Transcoders
Digital Cross Connects
Private Network Equipment
PABX's
DMI's
CPI's

ABSOLUTE MAXIMUM RATINGS

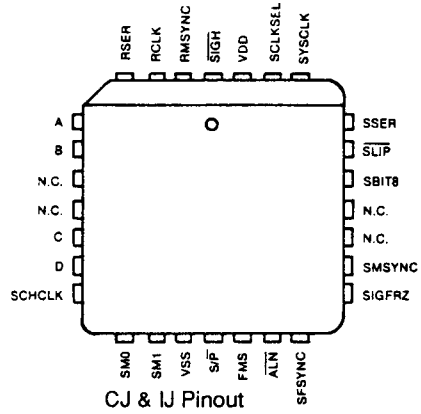
Input Voltage	-1.0V to 7.0V
Storage Temperature	-65°C to +150°C
Soldering Temperature	260°C for 10sec

NOTE: Stresses exceeding those specified above may cause permanent damage to the device or reduce normal operating life.

PIN ASSIGNMENT



CP & 1P Pinout



CJ & IJ Pinout

ORDERING INFORMATION

Part Number	Package	Operating Temp.
T5691 IP	Plastic	-40°C to +85°C
T5691 IJ	PLCC	-40°C to +85°C
XR-T5691CP	Plastic	0°C to 70°C
XR-T5691CJ	PLCC	0°C to 70°C

PIN DESCRIPTION

Pin #	Symbol	Description
1	SIGH	**SIGNALING INHIBIT.** When low it disables ABCD signaling updates for a period determined by SM0 and SM1 or until returned to high.
2	RMSYNC	**RECEIVE MULTIFRAMES SYNC.** When high during multiframe boundaries it establishes frame and multiframe alignment.
3	RCLK	**RECEIVE CLOCK.** Extracted 1.544 MHz clock.
4	RSER	**RECEIVE SERIAL DATA.** Sampled during the falling edge of RCLK.
5-8	A/B/C/D	**ROBBED-BIT SIGNALING OUTPUT A-D.**
9	SCHCLK	**SYSTEM CHANNEL CLOCK.** Needed for serial to parallel conversion of channel data. Transitions occur during channel boundaries.
10/11	SM0/SM1	**SIGNALING MODES** 0 AND 1. Select signaling logic.
12	VSS	**SIGNAL GROUND.**
13	S/P	**SERIAL TO PARALLEL SELECT.** Parallel (tie to VSS). Serial (tie to VDD).
14	FMS	**FRAME MODE SELECT.** For 193S Framing (tie to VSS) for 193E Framing (tie to VDD).
15	$\overline{\text{ALN}}$	**ALIGN.** When forced low, it recenters the buffer on the next system side frame boundary.
16	SFSYNC	**SYSTEM FRAME SYNC.** Rising edge establishes the start of the frame.
17	SIGFRZ	**SIGNALING FREEZE.** Indicates signaling updates when high. These can be caused internally via a slip or externally by forcing SIGH low.
18	SMSYNC	**SYSTEM MULTIFRAME SYNC.** Slip-compensated multiframe output; indicates when signaling updates are made.
19	SBIT8	**SYSTEM BIT 8.** Intended to reinsert the extracted signaling into the outgoing data stream. It is high during the LSB time of each channel.
20	$\overline{\text{SLIP}}$	**FRAME SLIP.** (Active low). Indicates a slip and held low for 64 SYSCLK cycles. Open collector output.
21	SSER	**SYSTEM SERIAL OUT.** Output data updated on the rising edge of SYSCLK.
22	SYSCLK	**SYSTEM CLOCK.** 1.544 MHz or 2.046 MHz clock.
23	SCLKSEL	**SYSTEM CLOCK SELECT. 1.544 MHz** (tie to VSS); 2.048 MHz (tie to VDD).
24	VCC	**POSITIVE SUPPLY VOLTAGE.** 5.0V +/- 10%.

SYSTEM DESCRIPTION

The XR-T5691 is designed to synchronize the received T1 PCM data (loop timed) to the host backplane, and also to supervise the robbed-bit signaling information embedded in the data stream. This device is intended to operate in conjunction with the XR-T5690 "T1 Framer" and the XR-T56L22 "T1 Line Receiver" to offer a complete system solution.

Synchronization

The XR-T5691 buffers the incoming PCM data from RSER into a 2-frame buffer (386 bits long). This data is sampled on the falling edge of RCLK and appears back at SSER where it is updated on the rising edge of SYSCLK. The frame and multiframe alignment on the receive side is established with the rising edge of RMSYNC. On the system side, a rising edge of SFSYNC establishes frame alignment. Buffer depth monitoring is done by an on board contention logic which signals a "slip" whenever the buffer is completely emptied or filled. After the occurence of a "slip", the SLIP output (open collector) is held low for 64 clock cycles and the buffer recenters automatically to a one-frame boundary. This configuration is adequate for most T-carrier applications which need to synchronize under short term jitter conditions. The XR-T5691 offers a good compromise between total delay and slip correction capability.

Buffer depth monitoring is achieved by sensing the distance between the rising edge of RMSYNC and SMSYNC real time. The output pulse SMSYNC which indicates the system side multiframe boundaries, is held high for 65 SYSCLK cycles.

This device is compatible with the two most common backplane frequencies (1.544 and 2.048MHz) which can be selected by strapping SCLKSEL to VCC for 2.048MHz and to VSS for 1.544MHz operation. In 1.544MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. For 2.048MHz applications the F-bit is dropped, and the MSB of channel 1 appears at SSER after a one bit period delay following the rising edge of SFSYNC. For the excess channels (greater than 24), the SSER pin is forced high. Also the slip criteria for 2.048MHz applications is different because of the faster system side read frequency.

The XR-T5691 is capable of interfacing to serial and/or parallel backplanes. For serial applications (S/P = 1), the data from channel 1 appears at SSER after a rising edge at SFSYNC as illustrated in Figure 8. For parallel applications a look-ahead mechanism is used whereby data is made available 8 clock cycles prior to SCHCLK in order to convert parallel data externally.

Signaling

Robbed-bit signaling data is inserted into the LSB portion of each channel during signaling frames. Depending on the type of frame format used (193S or 193E), the signaling information is first extracted from the incoming frames and then presented at the corresponding outputs (A, B, C or D). In 193S framing (FMS=0), the "A" signaling bits is inserted into frame 6 and the "B" signaling data into frame 12. In 193E framing (FMS=1), four signaling bits are available, in which case the two additional bits "C and D" are inserted into frames 18 and 24 correspondingly. The outputs A, B, C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframes. In 193S applications, the two extra outputs "C and D" contain the previous "A and B" data. Signaling updates occur once per multiframe at the rising edge of SMSYNC unless otherwise prohibited by the freeze function.

This "freeze function", which occurs during a slip condition or by forcing SIGH low, inhibits any signaling updates during alarm or slip conditions. The duration of the freeze is dependent on SM0 and SM1. During this period "old" data is recirculated in the output registers, and SIGFRZ is held high until the next signaling update. The input to output delay of the signaling data is equal to 1 multiframe plus the current depth of the PCM buffer (1 multiframe + 1 frame +/-1 frame).

Integration is another feature of the XR-T5691 which minimizes the impact of random noise and possible robbed-bit signaling corruption. This requires that the per channel signaling data be in the same state for 2 or more multiframes before appearing at A, B, C or D. As to what degree of integration is required can be selected by toggling SM0 and SM1. In order to minimize update delay, integration is limited to 1 multiframe during slip or alarm conditions. This is shown in Table 1.

Concerning ISDN applications and per channel capability, in order to assure integrity of data, the XR-T5691 will not merge processed signaling information back into the outgoing PCM frame. SBIT8 indicates the LSB position of each channel which can be combined with off chip logic to selectively reinsert robbed-bit signaling data into the outgoing data stream.

TABLE 1. SIGNALING SUPERVISION MODES

SM0	SM1	FMS	SELECTED MODE
0	0	0	193S framing, no integration, 1 multiframe freeze
0	0	1	193E framing, no integration, 1 multiframe freeze
0	1	0	193S framing, 2 multiframes integration & freeze
0	1	1	193E framing, 2 multiframes integration & freeze
1	0	0	193S framing, 5 multiframes integration & 2 multiframes freeze. (1)
1	0	1	193E framing, 3 multiframes integration & 2 multiframes freeze. (1)
1	1	0	Test mode.
1	1	1	Test mode.

Notes: 1) During a slip or alarm condition, integration is limited to 2 multiframes to minimize signaling delay.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V+/-10%, Ta = -40°C to +85°C unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Logic 1	2.0		V_{DD}+0.3	V	
V_{IL}	Logic 0	-0.3		+0.8	V	
V_{CC}	Positive Supply	4.5		5.5	V	
I_{CC}	Current Input		6	10	mA	Note 1, 2
I_{IL}	Leakage In Current	-1.0		+1.0	µA	
I_{OH}	Current Output High	-1.0			mA	Note 3
I_{OL}	Current Output Low	+4.0			mA	Note 4
I_{LO}	Leakage Output	-1.0		+1.0	µA	Note 5
C_{IN}	Input Capacitance			5	pF	
C_{OUT}	Output Capacitance			7	pF	

Notes: 1) TCLK = RCLK = 1.544 MHz
2) Outputs open
3) Measured @ 2.4V; all outputs except SLIP which is collector
4) All outputs
5) Applies to SLIP when tri-stated.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V+/-10%, Ta = -40°C to +85°C unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t RCLK	RCLK Period	250	648		ns	Figure 1
tR, tF	RCLK, SYSCLK Rise/Fall Time			20	ns	Figure 1
tRWH tRWL	RCLK Pulse Width	125	324		ns	Figure 1
tSWH tSWL	SYSCLK Pulse Width	100	244		ns	Figure 2
tSYSCLK	SYSCLK Period	200	488		ns	Figure 2
tSC	RMSYNC Setup to RCLK Rising	-tRWH/2		+tRWL/2	ns	Figure 1
tSC	SFSYNC Setup to SYSCLK Rising	-tSWL/2		-tSWL/2	ns	Figure 1 & 2
tPW	SFSYNC, SFSYNC $\overline{\text{SIGH}}$, $\overline{\text{ALN}}$ Pulse Width	100			ns	Figure 1 & 2
tHD	-RSER Hold from RCLK Falling	50			ns	Figure 1
tSD	RSER Setup to RCLK Falling	50			ns	
tPVD	Propagation delay SYSCLK to SSER A,B,C,D			100	ns	Figure2
tPSS	Propagation delay SYSCLK to SMSYNC High			75	ns	Figure 2
tPS	Propagation delay SYSCLK or RCLK to SLIP low			100	ns	Figure 1 & 2
tPSF	Propagation delay SYSCLK to SIGFRZ			75	ns	Figure 2
tSR	ALN, SIGH Setup to SFSYNC Rising	500			ns	Figure 2

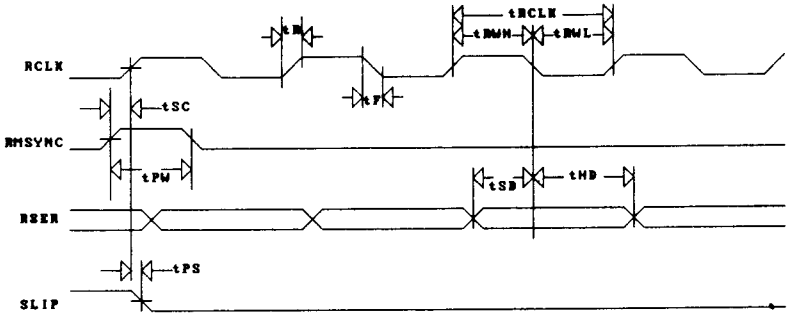


Figure 1. Receive A.C. Diagram

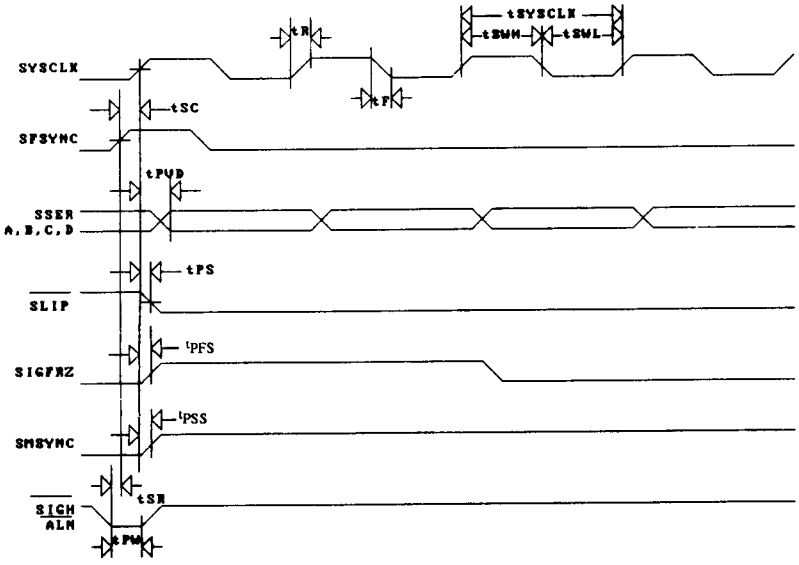


Figure 2. System AC Timing Diagram

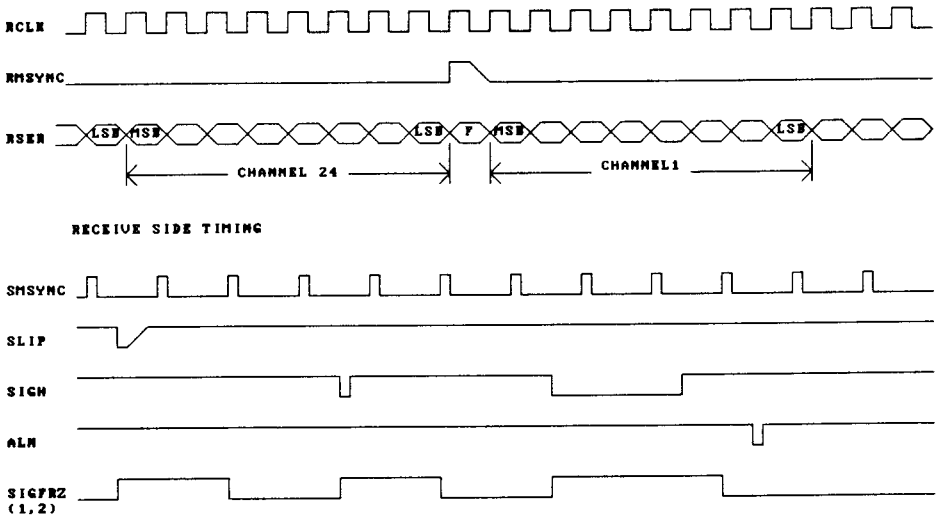


Figure 3. Slip and Signaling Supervision Logic Timing

Notes: 1) Integration feature disabled (SM0=SM1=0) in timing set shown.
2) Depending on present buffer depth, forcing ALN low may or may not cause a slip condition

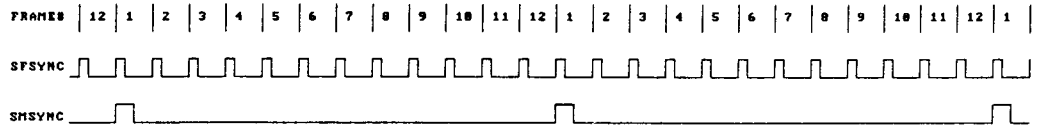


Figure 4. 193S System Multiframe Timing

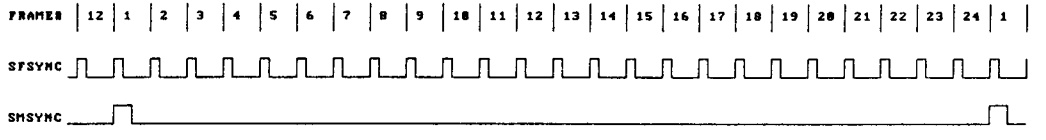


Figure 5. 193E System Multiframe Timing

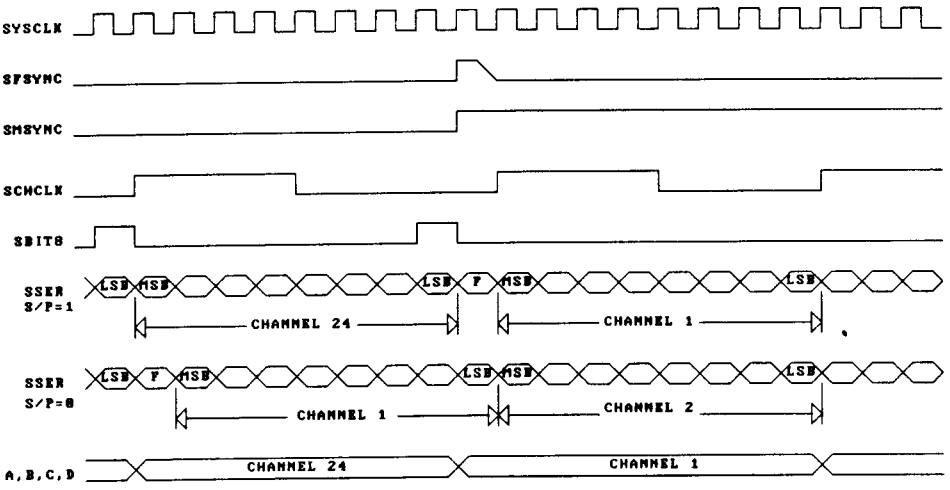


Figure 6. System Multiframe Boundry Timing (SYSCLM = 1.54 MHz)

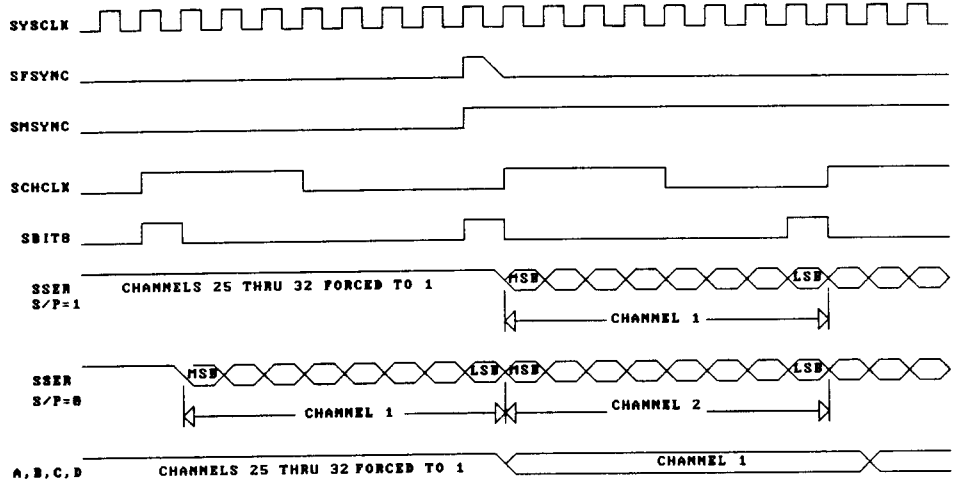


Figure 7. System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)

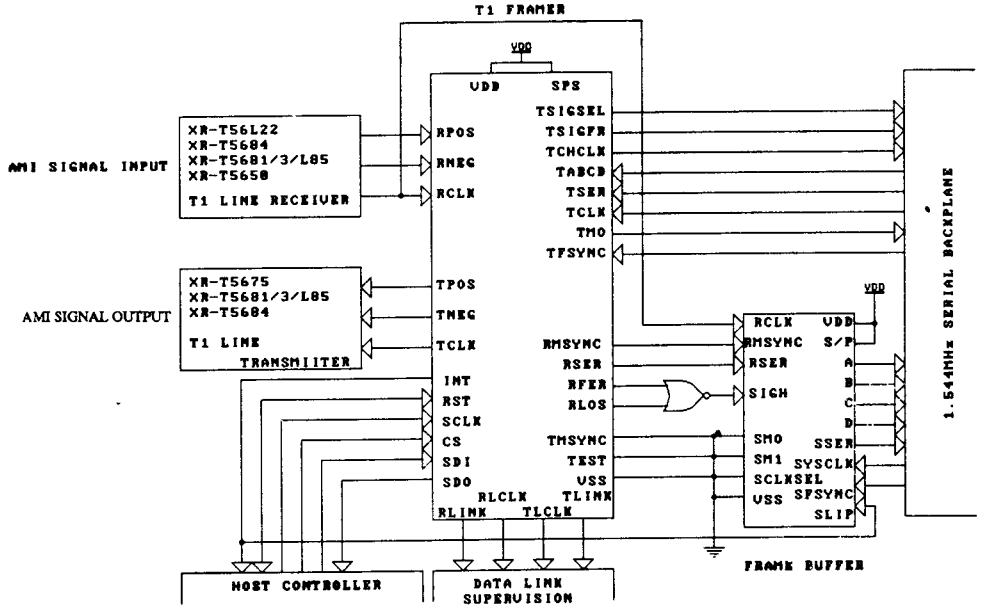


Figure 8. Typical Application using the XR-T5690 Framer and XR-T5691 Frame Buffer