T-46-23-05

GD4720B/GD4720BX

256-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION – The 4720B/4720BX is a 256-Bit Random Access Memory with 3-State Outputs. It has a Data Input (D), eight Address Inputs (A_0-A_7), an active HIGH Write Enable Input (WE), an active LOW Chip Select Input ($\overline{CS}$), an active HIGH 3-State Output (Q) and an active LOW 3-State Output ($\overline{Q}$). Information on the Data Input (D) is written into the memory location selected by the Address Inputs (A_0-A_7) when the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input (WE) is HIGH. Under these conditions, the device is transparent, i.e., the data input is reflected at the True and Complementary Outputs (Q, $\overline{Q}$). Information is read from the memory location selected by the Address Inputs (A_0-A_7) while the Chip Select ($\overline{CS}$) and the Write Enable (WE) Inputs are LOW. The Q Output is the information written into the memory, $\overline{Q}$ is its complement. When the Chip Select Input ($\overline{CS}$) is HIGH, both outputs (Q, $\overline{Q}$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The 4720B/4720BX offers fully static operation.

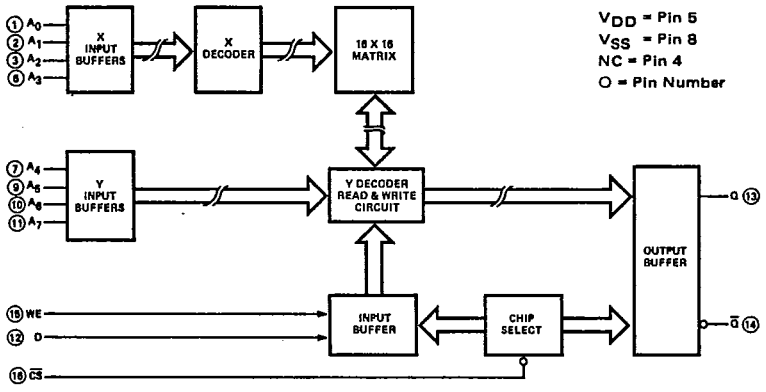
The 4720B is specified to operate over a power supply voltage range of 4.5 to 12.5 V. The 4720BX is specified to operate over a power supply voltage range of 3 to 15 V.

- 3-STATE OUTPUTS
- ORGANIZATION – 256 WORDS X 1-BIT
- ON-CHIP DECODING
- TRUE AND COMPLEMENT OUTPUTS AVAILABLE
- FULLY STATIC
- LOW POWER DISSIPATION
- HIGH SPEED
- TYPICAL HOLDING VOLTAGE OF 1.5 V

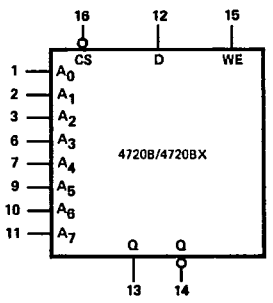
MODE SELECTION

$\overline{CS}$	WE	Q	$\overline{Q}$	MODE
L	H	Data Written Into Memory	Complement of Data Written Into Memory	Write
L	L	Data Written Into Memory	Complement of Data Written Into Memory	Read
H	X	High Impedance	High Impedance	Inhibit

BLOCK DIAGRAM

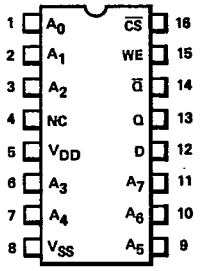


LOGIC SYMBOL



V_{DD} = Pin 5
V_{SS} = Pin 8
NC = Pin 4

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
WE	Write Enable Input
D	Data Input
A_0-A_7	Address Inputs
Q	3-State Output (Active HIGH)
$\overline{Q}$	3-State Output (Active LOW)

NOTE:
The SO Package has the same pin-outs (Connection Diagram) as the Dual In-line Package.

GS CMOS · GD4720B/GD4720BX

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current, HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
											12		MAX	
		XM									0.4	μA	MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current, LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
											-12		MAX	
		XM									-0.4	μA	MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

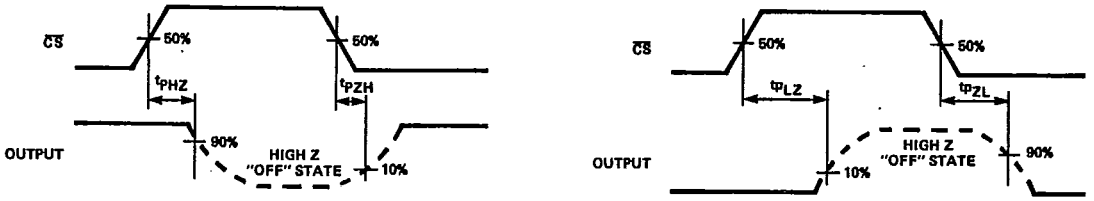
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
	READ MODE											
t_{PLH}	Propagation Delay,		250	500		95	190		68	136	ns	
t_{PHL}	Address to Output		250	500		95	190		68	136		
t_{PZH}	Enable Time, $\overline{CS}$ to Output		30	60		15	30		11	22	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			35	70		17	34		12	24		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Disable Time, $\overline{CS}$ to Output		25	50		15	30		11	22	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			27	54		16	32		12	24		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		75	150		35	70		25	50	ns	
t_{THL}			75	150		35	70		25	50		
	WRITE MODE											
t_{PLH}	Propagation Delay,		250	500		100	200		65	130	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}	WE to Output		250	500		100	200		65	130		
	WRITE MODE											
t_wWE	Minimum WE Pulse Width	240	120		110	55		80	40		ns	
t_s	Set-Up Time, D to WE	80	40		38	19		28	14		ns	
t_h	Hold Time, D to WE	40	20		22	11		18	9			
t_s	Set-Up Time, Address to WE	260	130		130	65		90	45		ns	
t_h	Hold Time, Address to WE	160	80		80	40		40	20			
t_s	Set-Up Time, $\overline{CS}$ to WE	60	30		30	15		20	10		ns	
t_h	Hold Time, $\overline{CS}$ to WE	60	30		30	15		20	10			

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. All set-up (t_s) and hold (t_h) times are measured with minimum write enable pulse width (t_wWE).

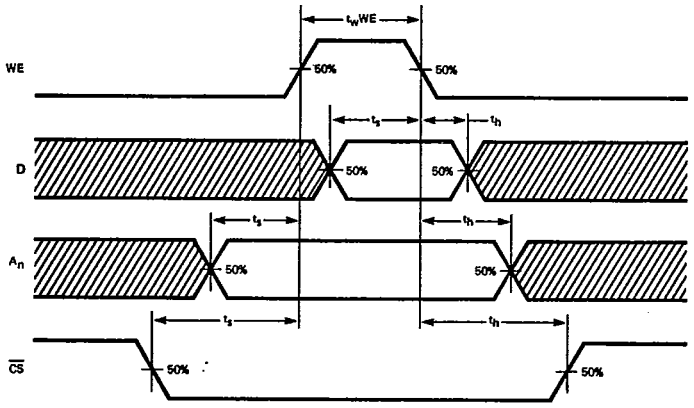
SWITCHING WAVEFORMS

READ MODE



$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



MINIMUM PULSE WIDTH FOR WE AND SET-UP AND HOLD TIMES, D TO WE, A_n TO WE, AND $\overline{CS}$ TO WE

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.