IBM PowerPRS™ Switch Core Interface Chip (SCIC), Version 2.1

Datasheet

Preliminary

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IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351

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Contents

List of Figures

List of Tables

1. General Information

1.1 Features

- Companion to the IBM PowerPRS™ 64G Packet Routing Switch and C192 Common Switch Interface chips
- PowerPRS C192-compatible high-speed serializer/deserializer (HSS) interface to PowerPRS 64G-compatible data-aligned synchronous link (DASL) serial interface conversion
- HSS interface: serial data communication of up to 2.5 Gbps, compatible with InfiniBand™ physical layer standards and protected by Fibre Channel Standard 8b/10b data encoding
- DASL interface: serial data communication of up to 500 Mbps, compliant with Electronic Industries Association/JEDEC Standard No. 8-6 regarding high-speed transceiver logic
- Synchronous clocks on the HSS and DASL serial interfaces
- 16-Gbps duplex throughput
- Configurable packet length of 64, 68, 72, 76, or 80 bytes
- 16- to 20-byte logical unit packet processing with PowerPRS 64G four-way port paralleling
- No queuing (pass-through device)
- Send grant and memory grant flow control serialization
- PowerPRS 64G-compatible packet header parity calculation and verification
- DASL cyclic redundancy check calculation and verification
- Detection of link liveness messages in service packets
- Eight-bit parallel processor interface or serial processor interface (serial host interface) to access all registers for control and error reporting
- Internal loopback support for both the PowerPRS 64G and C192
- Internal logic built-in self-test (BIST) and memory BIST
- IEEE® Standard 1149.1 boundary scan to facilitate circuit-board testing
- CMOS 7SF (SA-27E) technology (L_{drawn} = 0.18 µm, L_{eff} = 0.11 µm):
  - 2.5-V LVCMOS-compatible (3.3-V tolerant) I/Os for microprocessor interfaces
  - 1.8-V LVCMOS-compatible test I/Os
- 1.8-V DASL differential I/Os
- 27-mm, 399-ball IBM HyperBGA™ package

1.2 Description

The IBM PowerPRS Switch Core Interface Chip (SCIC) is a companion device to the IBM PowerPRS 64G Packet Routing Switch. It connects the switch's 32 data-aligned synchronous links (DASLs), which operate between 425 and 500 Mbps, to the PowerPRS C192's eight high-speed serializers/deserializers (HSSs, formerly Unilinks), which operate between 2.125 and 2.5 Gbps. The PowerPRS C192 functions as the switch core access layer between the protocol engine and the HSSs. Both the PowerPRS SCIC and the C192 use Fibre Channel Standard 8b/10b data encoding.

The PowerPRS SCIC receives data from incoming PowerPRS C192 packets, which are formatted in logical units (LUs) of 16 to 20 bytes for compatibility with the PowerPRS 64G. The PowerPRS SCIC alternately decodes the corresponding bytes of the two LUs carried on each HSS to feed the four DASL ports, which then carry the corresponding nibbles. The PowerPRS SCIC realigns the HSS and DASL ports to maintain the correct timing offset between the physical ports.

The PowerPRS SCIC resolves all input and output clock phase differences when both the receive and transmit clocks have the same frequency. The PowerPRS SCIC also transmits the DASL synchronization pattern controlled by the local processor.

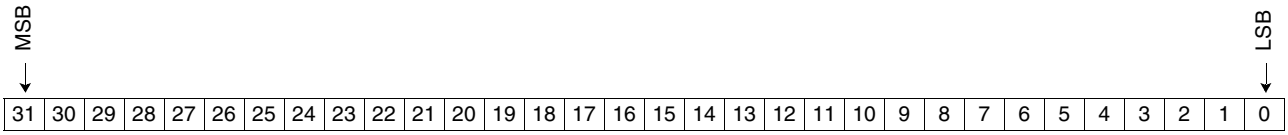
The PowerPRS SCIC implements the same eight-bit parallel processor interface as the PowerPRS C192 and the same serial processor interface as the PowerPRS 64G (that is, the serial host interface [SHI]). The parallel processor and the SHI can access the PowerPRS SCIC internal registers; download DASL picocode; and perform diagnostic functions, such as online error detection and reporting, and built-in self-test (BIST).

1.3 Ordering Information

Part Number	Description	Throughput
IBM3247P5177	IBM PowerPRS	16 Gbps

1.4 Notation and Conventions

Throughout this document, bit notation is non-IBM, meaning that bits and bytes are numbered in descending order from left to right. For a four-byte word, bit 31 is the most significant bit (MSB) and bit 0 is the least significant bit (LSB).



Notation for bit encoding is as follows:

- Hexadecimal values are preceded by an *x* and enclosed in single quotation marks. For example: x‘0A00’.
- Binary values in sentences appear in single quotation marks. For example: ‘1010’.

Differential pairs are designated by an *_P* for the positive signal and an *_N* for the negative signal at the end of the signal name. For example: DaslData[0]In[0]_P and DaslData[0]In[0]_N.

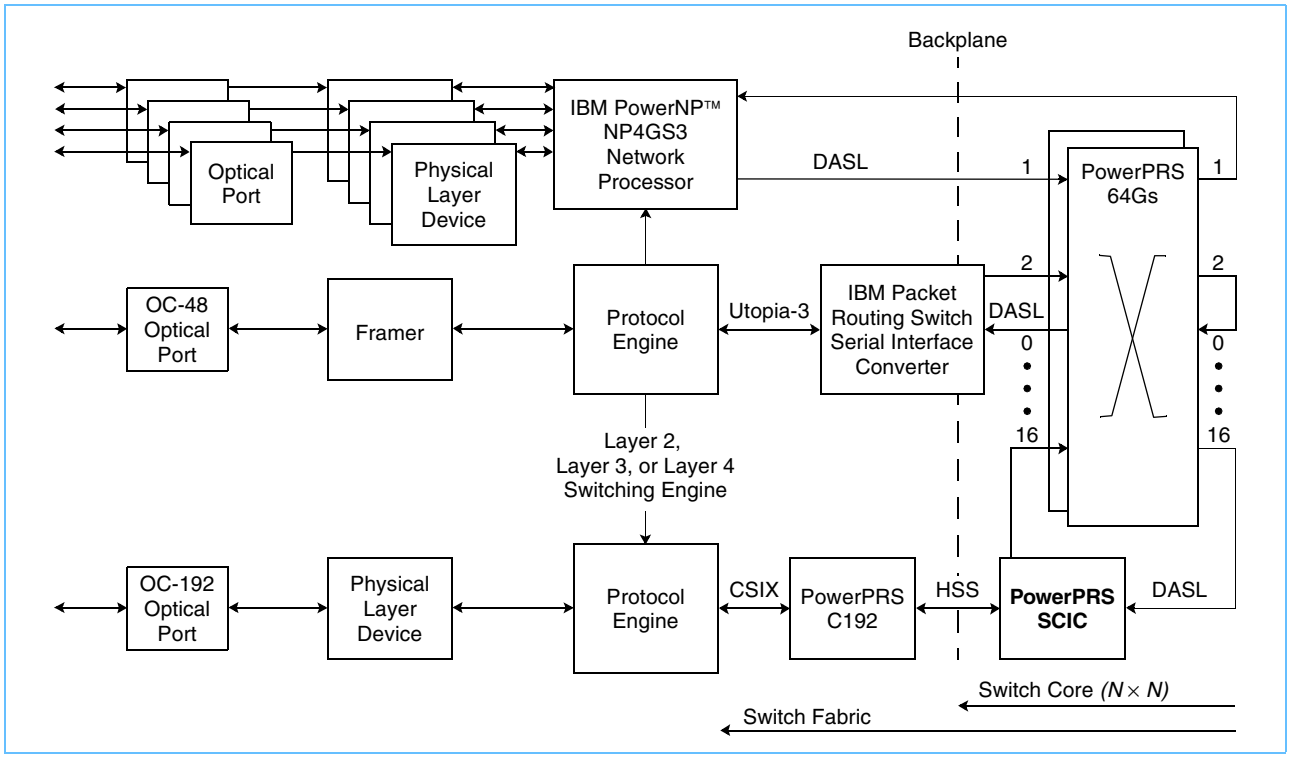
Nondifferential signals that are active low are designated by a *#* symbol at the end of the signal name. For example: InterruptOut#.

2. Architecture

2.1 System Application

In the system architecture illustrated in *Figure 2-1,* the PowerPRS SCIC is connected to eight PowerPRS C192 high-speed serializers/deserializers (HSSs), on the left side, and to four PowerPRS 64G data-aligned synchronous link (DASL) ports configured for port paralleling, on the right side. In a PowerPRS 64G-based switch core application, the PowerPRS C192 is attached between the switch fabric and the CSIX-compliant protocol engine to produce an OC-192 port.

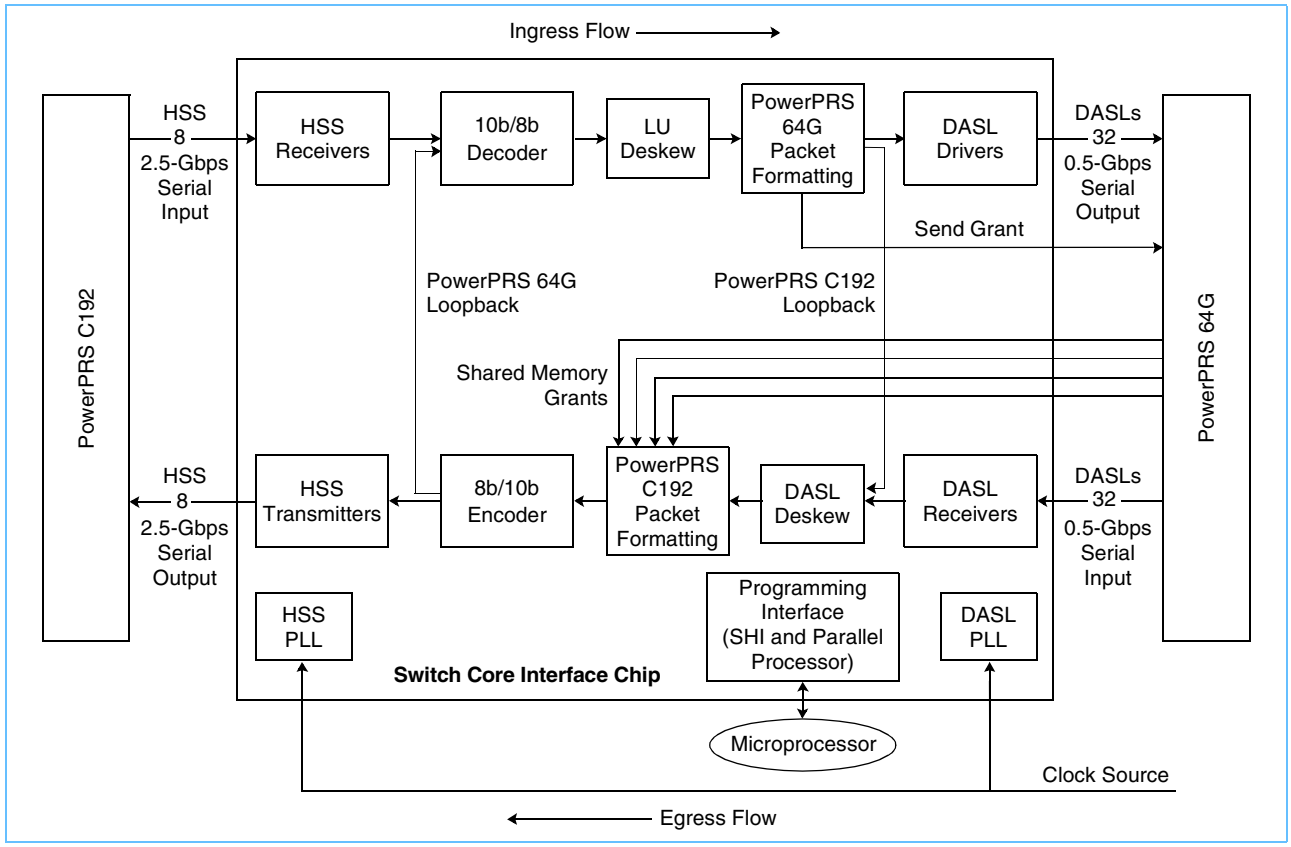
Figure 2-1. System View of the PowerPRS SCIC with the Network Processor and Packet Routing Switches



2.2 Internal Structure

Figure 2-2 on page 14 presents the internal structure of the PowerPRS SCIC. The PowerPRS SCIC is comprised of two nearly symmetrical data flows: the ingress data flow (to the switch) and the egress data flow (from the switch). To control the traffic flow, send grant and shared memory grant bits are exchanged between the PowerPRS 64G and the PowerPRS C192. The PowerPRS C192 codes up to four send-grant bits (one per priority) in the ingress packet headers before forwarding the packets to the PowerPRS SCIC. The PowerPRS SCIC decodes these bits and sends the data to the PowerPRS 64G via the send grant signal. The PowerPRS 64G sends up to four shared memory grant signals (one per priority) to the PowerPRS SCIC in the same way. The PowerPRS SCIC codes the memory grant bits into the egress packet headers before forwarding the packets to the PowerPRS C192. The PowerPRS C192 then decodes the memory grant bits.

Figure 2-2. PowerPRS SCIC Block Diagram



The PowerPRS SCIC is also comprised of a programming interface that provides access to all the internal registers and two phase-locked loops (PLLs), one for HSS clocks and the other for DASL and internal clocks. The two PLLs are fed by the same clock source so that the HSSs, DASLs, and all internal logic (except the programming interface) are synchronous. For this reason, there is no packet buffer. On the DASL interface, the throughput is 16 Gbps; on the HSS interface, it is 20 Gbps. However, the 8b/10b-coded HSSs produce a payload throughput of only 16-Gbps.

2.2.1 HSS Receivers

Eight HSS receivers deserialize the 2.5-Gbps serial data and transform it into 10-bit parallel bus data. The receivers also resynchronize the ingress packets according to the PowerPRS SCIC internal clock.

2.2.2 8b/10b Encoder/Decoder

In this block, data is either 8b/10b encoded (egress side) or decoded (ingress side) to improve data transmission and synchronization. Code violations are detected by the decoder.

2.2.3 LU Deskew

The logical unit (LU) deskew block rearranges the LU sequence to resolve the various link delays that accumulate on the eight HSS paths (for example, during clock resynchronization). The LU deskew process is performed during synchronization when traffic is comprised of idle packets only.

2.2.4 PowerPRS 64G Packet Formatting

The PowerPRS 64G packet formatting block analyzes each ingress packet qualifier byte (H0) to characterize the packet type, and extracts the send grant bits. It verifies the header parity, and calculates the cyclic redundancy check (CRC) value and inserts it into idle packets. The PowerPRS 64G packet formatting block modifies idle packet and synchronization packet format for DASL compatibility.

2.2.5 DASL Drivers and Receivers

DASL drivers and receivers serialize or deserialize the data packets on the four DASL switch ports.

2.2.6 DASL Deskew

The DASL deskew block rearranges the switch port sequence to resolve the various link delays that accumulate on the four DASL paths. The DASL deskew process is performed during synchronization when traffic is comprised of synchronization packets only.

2.2.7 PowerPRS C192 Packet Formatting

The PowerPRS C192 packet formatting block analyzes each egress packet qualifier byte (H0) to characterize the packet type. It verifies the header parity and the DASL CRC in idle packets, inserts the shared memory grant bits, and recalculates the header parity. The PowerPRS C192 packet formatting block modifies idle packet format for HSS compatibility.

2.2.8 HSS Transmitters

Eight HSS transmitters resynchronize egress data packets according to the HSS clocks, and serialize the internal 10-bit bus data into 2.5-Gbps serial data.

2.2.9 HSS and DASL PLLs

The HSS and DASL phase-locked loops (PLLs) generate all the clocks for the HSSs, DASLs, and internal logic (except the programming interface, which has a separate clock).

2.2.10 Programming Interface

The programming interface allows access to all PowerPRS SCIC internal registers.

3. Functional Description

This section describes basic PowerPRS SCIC functionality, including information about:

- Packet type
- Packet format according to packet type
- Ingress and egress data flow
- Internal loopbacks
- Synchronization
- Clocking

3.1 Packet Type

There are five types of packets:

- Data packets
- Idle packets
- Service packets
- Synchronization packets
- Control packets

3.1.1 Data Packets

Data packets contain user data (payload) to be transferred from one device to another. They have a priority of 0, 1, 2, or 3, with 0 being the highest priority. Data packet headers carry routing information (destination bitmap), filtering information used for switchover support (color coding), and a “best-effort discard” flag. Egress data packets (and egress idle packets) carry the output queue grants that control ingress traffic flow to the PowerPRS 64G (see *Section 3.2.5 Egress Data Packet Format* on page 26).

3.1.2 Idle Packets

When there is no data available to transfer, the PowerPRS 64G on the egress side and the PowerPRS C192 on the ingress side transmit idle packets. Idle packets are used to maintain and verify valid synchronization on the high-speed SerDes (HSS) links. They also contain a side communication channel (SCC) byte in the sixth byte position. The SCC byte is not part of the packet header; the PowerPRS SCIC considers it data and leaves it intact.

3.1.3 Service Packets

The PowerPRS SCIC transfers service packets (also called yellow packets) between the PowerPRS 64G and the C192. There are three types of service packets:

- *Event-1 service packets* (or yellow type-1 service packets) are used to test link liveness.
- *Event-2 service packets* (or yellow type-2 service packets) are used to communicate events, such as write acknowledgement.
- *Command service packets* (or yellow type-3 service packets) are used to request actions, such as read and write access.

Each time the PowerPRS SCIC detects a service packet on the ingress or egress path, it sets the corresponding bit in the *Yellow Packet Register* (page 64).

The PowerPRS SCIC regards egress service packets as data packets and leaves the data intact. On the ingress side, the PowerPRS SCIC may calculate a cyclic redundancy check (CRC) value and insert the corresponding bits into the trailer byte of a service packet, depending on the Service Packet CRC Insert bit setting in the *General Configuration Register* (page 62).

3.1.4 Synchronization Packets

Synchronization packets are used to transition bits and delineate packets for synchronizing the data-aligned synchronous links (DASLs). Synchronization packets exist only on the PowerPRS SCIC DASL interface. As stated in *Section 3.1.2,* idle packets are used to synchronize the HSS links.

3.1.5 Control Packets

Control packets carry the communications between the local processor and the protocol engine. The PowerPRS SCIC regards them as data packets.

3.2 Packet Format According to Packet Type

3.2.1 General Packet Format Information

The PowerPRS SCIC supports five packet lengths: 64, 68, 72, 76, and 80 bytes. Packets are transferred in four logical units (LUs) of 16 to 20 bytes each, depending on the packet length. The LU Length field (bits 5:1) must be set in the *General Configuration Register* (page 62) after reset but before starting any traffic. Once traffic begins, the LU length cannot be changed.

The PowerPRS SCIC's four-way port paralleling feature causes the timing relationship illustrated in *Figure 3-1* between the four packets processed in parallel. The PowerPRS SCIC preserves this relationship across the HSS and DASL interfaces to the PowerPRS 64G on the ingress path and across the DASL and HSS interfaces to the PowerPRS C192 on the egress path.

Figure 3-1. PowerPRS SCIC Four-Way Port Paralleling Packet Timing

		C0				C4				C8				C12				C0
Port 0	DASL-0 Master[0:3]	H0-0	OQG0	OQG1	OQG2	OQG3	D	D	D	D	D	D	D	D	D	D	D	H0-0
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	DASL-0 Slave[0:3]	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Port 1	DASL-1 Master[0:3]	D	D	D	D	H0-1	OQG0	OQG1	OQG2	OQG3	D	D	D	D	D	D	D	D
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	DASL-1 Slave[0:3]	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Port 2	DASL-2 Master[0:3]	D	D	D	D	D	D	D	D	H0-2	OQG0	OQG1	OQG2	OQG3	D	D	D	D
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	DASL-2 Slave[0:3]	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Port 3	DASL-3 Master[0:3]	D	D	D	D	D	D	D	D	D	D	D	D	H0-3	OQG0	OQG1	OQG2	OQG3
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	DASL-3 Slave[0:3]	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

3.2.1.1 Packet Header

The PowerPRS SCIC supports three packet header lengths: 2, 3, and 5 bytes. Like the packet length, the Header Length field (bits 7:6) must be set in the *General Configuration Register* (page 62) after reset but before starting any traffic. Once traffic begins, the header length cannot be changed.

On the ingress path, packet headers are comprised of the following bytes:

- Two-byte header: packet qualifier byte (H0) and one bitmap byte (BM0)
- Three-byte header: H0 and two bitmap bytes (BM0 and BM1)
- Five-byte header: H0 and four bitmap bytes (BM0 through BM3)

On the egress path, packet headers are comprised of the following bytes:

- Two-byte header: H0 and one output queue grant byte (OQG0)
- Three-byte header: H0 and two output queue grant bytes (OQG0 and OQG1)
- Five-byte header: H0 and four output queue grant bytes (OQG0 through OQG3)

The PowerPRS SCIC does not use the bitmap and output queue grant header bytes but leaves them intact.

The packet header is protected on the ingress (PowerPRS C192 to PowerPRS SCIC) and egress (PowerPRS 64G to PowerPRS SCIC) paths by an even parity bit in the packet qualifier byte. The PowerPRS SCIC calculates and verifies the packet header parity according to the header length. If the PowerPRS SCIC detects a parity error in a data, service, or *ingress* idle packet header, then it transmits the packet with an incorrect header parity. If it detects a parity error in an *egress* idle packet header, the PowerPRS SCIC corrects the header parity before transmitting the packet. After modifying a packet header, the PowerPRS SCIC recalculates the header parity before transmitting the packet. All parity errors are reported in the *Packet Error Register* (page 66).

3.2.1.2 DASL Interface CRC Protection

All packets on the DASL interface ingress and egress paths are protected by cyclic redundancy check (CRC) bits coded in the trailer byte of each *idle* packet LU. CRC values are calculated on every byte of each LU between two idle packet trailer bytes. On the ingress path, the PowerPRS SCIC calculates the CRC value and the PowerPRS 64G verifies it. On the egress path, the PowerPRS 64G calculates the CRC value and the PowerPRS SCIC verifies it. When the PowerPRS SCIC detects a CRC error, it reports it in the *Packet Error Register*.

3.2.2 Ingress Data Packet Format

The data packet format for ingress packets on the PowerPRS SCIC HSS interface is presented in *Figure 3-2* on page 20. The packet header format (bytes H0 through H4) is presented and described in *Tables 3-1* through *3-3* on page 20.

Figure 3-2. PowerPRS C192 to PowerPRS SCIC Data Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
LU 0	H0	H1	H2/D	H3/D	H4/D	D	D	D	…	D	D	D	D	D	D
LU 1	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
LU 2	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
LU 3	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D

Notes:

1. Each of the four parallel packets is distributed over two HSS pairs (for example, packet 0 is carried on HSS-0 and HSS-1, packet 1 is carried on HSS-2 and HSS-3, and so forth).
2. LU 0 and LU 2 are carried on the high channel and LU 1 and LU 3 are carried on the low channel.
3. H0 through H4 are packet header bytes.
4. D is user data.

Table 3-1. PowerPRS C192 to PowerPRS SCIC Data Packet, Byte H0

Byte	Information Carried					
	Bit 0	Bit 1	Bits 2:3	Bit 4	Bit 5	Bits 6:7
H0 (high channel)	Extended bitmap	Parity	Protection	Best effort	Send grant	Packet priority

Table 3-2. PowerPRS C192 to PowerPRS SCIC Data Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Extended Bitmap	Designates the range of output ports addressed by the destination bitmap in the data packet header: 0 Ports 0 to 7 or ports 0 to 15, depending on the switch fabric port configuration 1 Ports 8 to 15 or ports 16 to 31, depending on the switch fabric port configuration
1	Parity	Header parity (see *Section 3.2.1.1* on page 19).
2:3	Protection	Specifies the traffic type (red data packet or blue data packet): 01 Red (backup) 10 Red (active) 11 Blue (unfiltered)
4	Best Effort	Flags packet as best-effort bandwidth traffic when the PowerPRS 64G best-effort discard function is enabled: 1 Packet flagged as best-effort bandwidth traffic (optional discard). 0 Packet flagged as guaranteed bandwidth traffic (no discard).
5	Send Grant	Reports the status of the send grant for the priority specified by the PowerPRS SCIC port number (for example, port 0 carries the send grant for priority 0 [SG0], port 1 carries the send grant for priority 1 [SG1], and so forth).
6:7	Packet Priority	Specifies the packet priority (data packets only): 00 Priority 0 (highest priority) 01 Priority 1 10 Priority 2 11 Priority 3 (lowest priority)

Table 3-3. PowerPRS C192 to PowerPRS SCIC Data Packet, Bytes H1 through H4

Header Byte	Packet Destination Bitmap							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
H1 (high channel)	Output port 0	Output port 1	Output port 2	Output port 3	Output port 4	Output port 5	Output port 6	Output port 7
H2 (high channel)	Output port 8	Output port 9	Output port 10	Output port 11	Output port 12	Output port 13	Output port 14	Output port 15
H3 (high channel)	Output port 16	Output port 17	Output port 18	Output port 19	Output port 20	Output port 21	Output port 22	Output port 23
H4 (high channel)	Output port 24	Output port 25	Output port 26	Output port 27	Output port 28	Output port 29	Output port 30	Output port 31

In NP4GS3 network processor applications (see *Figure 2-1* on page 13), the ingress data packet (or frame) format is the same as the format presented in *Figure 3-2* on page 20 except for the packet qualifier byte. *Tables 3-4* and *3-5* present and describe the packet qualifier byte format in NP4GS3 applications.

Table 3-4. PowerPRS C192 to PowerPRS SCIC Data Packet in NP4GS3 Applications, Byte H0

Byte	Information Carried					
	Bit 0	Bit 1	Bits 2:3	Bit 4	Bit 5	Bits 6:7
H0 (high channel)	Reserved	Parity	Protection	Send grant	Reserved	Packet priority

Table 3-5. PowerPRS C192 to PowerPRS SCIC Data Packet in NP4GS3 Applications, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Reserved	Set to '1'.
1	Parity	See *Table 3-2* on page 20.
2:3	Protection	See *Table 3-2*.
4	Send Grant	See *Table 3-2*, bit 5.
5	Reserved	1 Indicates packet format. 0 Indicates frame format.
6:7	Packet Priority	See *Table 3-2*.

The data packet format for ingress packets on the PowerPRS SCIC DASL interface is presented in *Figure 3-3* on page 22. The packet header format is identical to the format presented and described in *Tables 3-1* through *3-3* on page 20 except for bit 5 in the packet qualifier byte. *Table 3-6* on page 22 indicates that bit 5 is reserved for future use.

Figure 3-3. PowerPRS SCIC to PowerPRS 64G Data Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
Master LU	H0	H1	H2/D	H3/D	H4/D	D	D	D	…	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D

Notes:

1. Each of the four parallel packets is distributed over eight DASL pairs.
2. The master LU and one slave LU are carried on the master port and the remaining two slave LUs are carried on the slave port.
3. H0 through H4 are packet header bytes.
4. D is user data.

Table 3-6. PowerPRS SCIC to PowerPRS 64G Data Packet, Byte H0

Byte	Information Carried					
	Bit 0	Bit 1	Bits 2:3	Bit 4	Bit 5	Bits 6:7
H0	Extended bitmap	Parity	Protection	Best effort	Reserved	Packet priority

3.2.3 Ingress Idle Packet Format

The idle packet format for ingress packets on the PowerPRS SCIC HSS interface is presented in *Figure 3-4.* The packet header format (byte H0) is presented and described in *Tables 3-7* and *3-8* on page 23.

Figure 3-4. PowerPRS C192 to PowerPRS SCIC Idle Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
LU 0	H0	D	D	D	D	SCC	SG	K28.1	…	D	D	D	D	D	D
LU 1	D	D	D	D	D	D	D	K28.5	…	D	D	D	D	D	D
LU 2	D	D	D	D	D	D	D	K28.1	…	D	D	D	D	D	D
LU 3	D	D	D	D	D	D	D	K28.5	…	D	D	D	D	D	D

Notes:

1. Each of the four parallel packets is distributed over two HSS pairs (for example, packet 0 is carried on HSS-0 and HSS-1, packet 1 is carried on HSS-2 and HSS-3, and so forth).
2. LU 0 and LU 2 are carried on the high channel and LU 1 and LU 3 are carried on the low channel.
3. H0 is the packet qualifier byte.
4. D is the 8b/10b-coded D21.5 character (alternating ‘01’).
5. SCC is the side communication channel.
6. SG is the send grant byte.
7. K28.1 and K28.5 are 8b/10b-coded K characters.

Table 3-7. PowerPRS C192 to PowerPRS SCIC Idle Packet, Byte H0

Byte	Information Carried				
	Bit 0	Bit 1	Bits 2:3	Bits 4:5	Bits 6:7
H0 (high channel)	Reserved	Parity	Protection	Color	Reserved

Table 3-8. PowerPRS C192 to PowerPRS SCIC Idle Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Reserved	Reserved.
1	Parity	Header parity.
2:3	Protection	Specifies the traffic type: 00 Idle packet
4:5	Color	Specifies the idle packet color: 00 Blue 01 Red
6:7	Reserved	Reserved.

Tables 3-9 and *3-10* present the format for the side communication channel and send grant bytes, respectively. The side communication channel byte exists only in ingress and egress idle packets.

Table 3-9. PowerPRS C192 to PowerPRS SCIC Side Communication Channel, SCC Byte

Byte	Information Carried							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
H0 (high channel)	SCC0	SCC1	SCC2	SCC3	SCC0	SCC1	SCC2	SCC3

Table 3-10. PowerPRS C192 to PowerPRS SCIC Send Grant, SG Byte

Byte	Information Carried							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
H0 (high channel)	SG0	SG1	SG2	SG3	SG0	SG1	SG2	SG3

The idle, service, and synchronization packet format for ingress packets on the PowerPRS SCIC DASL interface is presented in *Figure 3-5* on page 24. The packet header format (byte H0) is presented and described in *Tables 3-11* and *3-12* (page 24).

Figure 3-5. PowerPRS SCIC to PowerPRS 64G Idle, Service, or Synchronization Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
Master LU	H0	D	D	D	D	SCC	D	D	…	D	T/D	T/D	T/D	T/D	T
Slave LU	D	D	D	D	D	D	D	D	…	D	T/D	T/D	T/D	T/D	T
Slave LU	D	D	D	D	D	D	D	D	…	D	T/D	T/D	T/D	T/D	T
Slave LU	D	D	D	D	D	D	D	D	…	D	T/D	T/D	T/D	T/D	T

Notes:

1. Each of the four parallel packets is distributed over eight DASL pairs.
2. The master LU and one slave LU are carried on the master port and the remaining two slave LUs are carried on the slave port.
3. H0 is the packet qualifier byte.
4. D is x‘CC’ (alternating ‘01’).
5. SCC is the side communication channel (idle packets only).
6. T is the trailer CRC (optional in service packets).

Table 3-11. PowerPRS SCIC to PowerPRS 64G Idle, Service, or Synchronization Packet, Byte H0

Byte	Information Carried				
	Bit 0	Bit 1	Bits 2:3	Bits 4:5	Bits 6:7
H0	Color	Parity	Protection	Color	Reserved

Table 3-12. PowerPRS SCIC to PowerPRS 64G Idle, Service, or Synchronization Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Color	Specifies the packet color and/or type: 0 Yellow type-1 and type-2 service packets 1 Yellow type-3 service packets and synchronization packets **Note:** This field is ignored in *ingress* idle packets.
1	Parity	Header parity. This field is set to ‘1’ in a synchronization packet.
2:3	Protection	Specifies the traffic type: 00 Idle, service, or synchronization packet
4:5	Color	Specifies the packet color and/or type: 00 Blue idle packet 01 Red idle packet 10 Yellow type-1 service packet 11 Yellow type-2 service packet 10 Yellow type-3 service packet 11 Synchronization packet
6:7	Reserved	Reserved.

3.2.4 Ingress Service Packet Format

The service packet format for ingress packets on the PowerPRS SCIC HSS interface is presented in *Figure 3-6.* The packet header format (byte H0) is presented and described in *Tables 3-13* and *3-14*.

Figure 3-6. PowerPRS C192 to PowerPRS SCIC Service Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
LU 0	H0	D	D	D	D	D	SG	D	…	D	D	D	D	D	D
LU 1	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
LU 2	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
LU 3	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D

Notes:

1. Each of the four parallel packets is distributed over two HSS pairs (for example, packet 0 is carried on HSS-0 and HSS-1, packet 1 is carried on HSS-2 and HSS-3, and so forth).
2. LU 0 and LU 2 are carried on the high channel and LU 1 and LU 3 are carried on the low channel.
3. H0 is the packet qualifier byte.
4. D is the 8b/10b-coded D21.5 character (alternating ‘01’).
5. SG is the send grant byte.

Table 3-13. PowerPRS C192 to PowerPRS SCIC Service Packet, Byte H0

Byte	Information Carried				
	Bit 0	Bit 1	Bits 2:3	Bits 4:5	Bits 6:7
H0 (high channel)	Color	Parity	Protection	Color	Reserved

Table 3-14. PowerPRS C192 to PowerPRS SCIC Service Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Color	Specifies the packet color and type: 0 Yellow type-1 or type-2 service packet 1 Yellow type-3 service packet
1	Parity	Header parity.
2:3	Protection	Specifies the traffic type: 00 Service packet
4:5	Color	Specifies the packet color and type: 10 Yellow type-1 service packet 11 Yellow type-2 service packet 10 Yellow type-3 service packet
6:7	Reserved	Reserved.

The format of the send grant byte carried in ingress service packets is identical to the format of the send grant byte carried in ingress idle packets (see *Table 3-10* on page 23).

3.2.5 Egress Data Packet Format

The data packet format for egress packets on the PowerPRS SCIC DASL interface is identical to the format of ingress data packets presented in *Figure 3-3* on page 22. The packet qualifier byte format is presented and described in *Tables 3-15* and *3-16.*

Table 3-15. PowerPRS 64G to PowerPRS SCIC Data Packet, Byte H0

Byte	Information Carried					
	Bit 0	Bit 1	Bits 2:3	Bit 4	Bit 5	Bits 6:7
H0	Reserved	Parity	Protection	Best effort	Reserved	Packet priority

Table 3-16. PowerPRS 64G to PowerPRS SCIC Data Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Reserved	Reserved.
1	Parity	Header parity.
2:3	Protection	Specifies the traffic type (red data packet or blue data packet): 01 Red (backup) 10 Red (active) 11 Blue (unfiltered)
4	Best Effort	Flags packet as best-effort bandwidth traffic when the PowerPRS 64G best-effort discard function is enabled: 1 Packet flagged as best-effort bandwidth traffic (optional discard). 0 Packet flagged as guaranteed bandwidth traffic (no discard).
5	Reserved	Reserved.
6:7	Packet Priority	Specifies the packet priority (data packets only): 00 Priority 0 (highest priority) 01 Priority 1 10 Priority 2 11 Priority 3 (lowest priority)

When the PowerPRS 64G output queue grant function is enabled, the remaining egress data packet header bytes (H1 through H4) carry the output queue grants used for ingress flow control. The output queue mapping in egress data packets follows the same pattern as the output port mapping in ingress data packets (see *Table 3-3* on page 21).

The data packet format for egress packets on the PowerPRS SCIC HSS interface is identical to the ingress data packet format presented in *Figure 3-2* on page 20. The packet qualifier byte format is presented and described in *Tables 3-17* and *3-18* (page 27).

Table 3-17. PowerPRS SCIC to PowerPRS C192 Data Packet, Byte H0

Byte	Information Carried					
	Bit 0	Bit 1	Bits 2:3	Bit 4	Bit 5	Bits 6:7
H0 (high channel)	Reserved	Parity	Protection	Best effort	Shared memory	Packet priority

Table 3-18. PowerPRS SCIC to PowerPRS C192 Data Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Reserved	Reserved.
1	Parity	See *Table 3-16* on page 26.
2:3	Protection	See *Table 3-16*.
4	Best Effort	See *Table 3-16*.
5	Shared Memory	Reports the status of the shared memory for the priority specified by the PowerPRS SCIC port number (for example, port 0 carries the shared memory grant for priority 0 [SM0], port 1 carries the shared memory grant for priority 1 [SM1], and so forth).
6:7	Packet Priority	See *Table 3-16*.

In NP4GS3 network processor applications, the egress data packet (or frame) format is the same as the ingress data packet format presented in *Figure 3-2* on page 20 except for the packet qualifier byte. *Tables 3-19* and *3-20* present and describe the packet qualifier byte format in NP4GS3 applications.

Table 3-19. PowerPRS SCIC to PowerPRS C192 Data Packet in NP4GS3 Applications, Byte H0

Byte	Information Carried					
	Bit 0	Bit 1	Bits 2:3	Bit 4	Bit 5	Bits 6:7
H0 (high channel)	Reserved	Parity	Protection	Shared memory	Reserved	Packet priority

Table 3-20. PowerPRS SCIC to PowerPRS C192 Data Packet in NP4GS3 Applications, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Reserved	Set to ‘1’.
1	Parity	See *Table 3-16* on page 26.
2:3	Protection	See *Table 3-16*.
4	Shared Memory	Reports the status of the shared memory for the priority specified by the PowerPRS SCIC port number (for example, port 0 carries the shared memory grant for priority 0 [SM0], port 1 carries the shared memory grant for priority 1 [SM1], and so forth).
5	Reserved	1 Indicates packet format. 0 Indicates frame format.
6:7	Packet Priority	See *Table 3-16*.

3.2.6 Egress Idle Packet Format

The idle packet format for egress packets on the PowerPRS SCIC DASL interface is presented in *Figure 3-7* on page 28. The packet qualifier byte format is identical to the packet qualifier byte in ingress idle packets (see *Tables 3-11* and *3-12* on page 24). Like egress data packets, the remaining egress idle packet header bytes (H1 through H4) carry output queue grants used for ingress flow control.

Figure 3-7. PowerPRS 64G to PowerPRS SCIC Idle Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
Master LU	H0	H1	H2/D	H3/D	H4/D	SCC	D	D	…	D	T/D	T/D	T/D	T/D	T
Slave LU	D	D	D	D	D	D	D	D	…	D	T/D	T/D	T/D	T/D	T
Slave LU	D	D	D	D	D	D	D	D	…	D	T/D	T/D	T/D	T/D	T
Slave LU	D	D	D	D	D	D	D	D	…	D	T/D	T/D	T/D	T/D	T

Notes:

1. Each of the four parallel packets is distributed over eight DASL pairs.
2. The master LU and one slave LU are carried on the master port and the remaining two slave LUs are carried on the slave port.
3. H0 through H4 are packet header bytes.
4. D is x‘CC’ (alternating ‘01’).
5. SCC is the side communication channel.
6. T is the trailer CRC.

The format of the side communication channel (SCC) byte carried in egress idle packets is identical to the format of the SCC byte carried in ingress idle packets (see *Table 3-9* on page 23).

The idle packet format for egress packets on the PowerPRS SCIC HSS interface is presented in *Figure 3-8.* The packet qualifier byte format is presented and described in *Tables 3-21* and *3-22* on page 29.

Figure 3-8. PowerPRS SCIC to PowerPRS C192 Idle Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
LU 0	H0	H1	H2/D	H3/D	H4/D	SCC	SM	K28.1	…	D	D	D	D	D	D
LU 1	D	D	D	D	D	D	D	K28.5	…	D	D	D	D	D	D
LU 2	D	D	D	D	D	D	D	K28.1	…	D	D	D	D	D	D
LU 3	D	D	D	D	D	D	D	K28.5	…	D	D	D	D	D	D

Notes:

1. Each of the four parallel packets is distributed over two HSS pairs (for example, packet 0 is carried on HSS-0 and HSS-1, packet 1 is carried on HSS-2 and HSS-3, and so forth).
2. LU 0 and LU 2 are carried on the high channel and LU 1 and LU 3 are carried on the low channel.
3. H0 through H4 are packet header bytes.
4. D is the 8b/10b-coded D21.5 character (alternating ‘01’).
5. SCC is the side communication channel.
6. SM is the shared memory grant byte.
7. K28.1 and K28.5 are 8b/10b-coded K characters.

Table 3-21. PowerPRS SCIC to PowerPRS C192 Idle Packet, Byte H0

Byte	Information Carried				
	Bit 0	Bit 1	Bits 2:3	Bits 4:5	Bits 6:7
H0 (high channel)	Extended flywheel	Parity	Protection	Color	Grant priority

Table 3-22. PowerPRS SCIC to PowerPRS C192 Idle Packet, Byte H0 Field Descriptions

Bit(s)	Field Name	Description
0	Extended Flywheel	Designates the range of output ports for which the idle packet is carrying output queue grants: 0 Ports 0 to 7 or ports 0 to 15, depending on the switch fabric port configuration 1 Ports 8 to 15 or ports 16 to 31, depending on the switch fabric port configuration
1	Parity	Header parity.
2:3	Protection	Specifies the traffic type: 00 Idle packet
4:5	Color	Specifies the idle packet color: 00 Blue 01 Red
6:7	Grant Priority	Specifies the grant priority: 00 Priority 0 (highest priority) 01 Priority 1 10 Priority 2 11 Priority 3 (lowest priority)

Table 3-23 presents the format for the shared memory grant bytes.

Table 3-23. PowerPRS C192 to PowerPRS SCIC Shared Memory Grant, SM Byte

Byte	Information Carried							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
H0 (high channel)	SM0	SM1	SM2	SM3	SM0	SM1	SM2	SM3

3.2.7 Egress Service Packet Format

The service packet format for egress packets on the PowerPRS SCIC HSS interface is presented in *Figure 3-9* on page 30. The packet qualifier byte format is identical to the packet qualifier byte in ingress service packets (see *Tables 3-13* and *3-14* on page 25). Like egress data and idle packets, the remaining egress service packet header bytes (H1 through H4) carry output queue grants used for ingress flow control.

Figure 3-9. PowerPRS SCIC to PowerPRS C192 Service Packet

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	…	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19
LU 0	H0	H1	H2/D	H3/D	H4/D	D	SM	D	…	D	D	D	D	D	D
LU 1	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
LU 2	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D
LU 3	D	D	D	D	D	D	D	D	…	D	D	D	D	D	D

Notes:

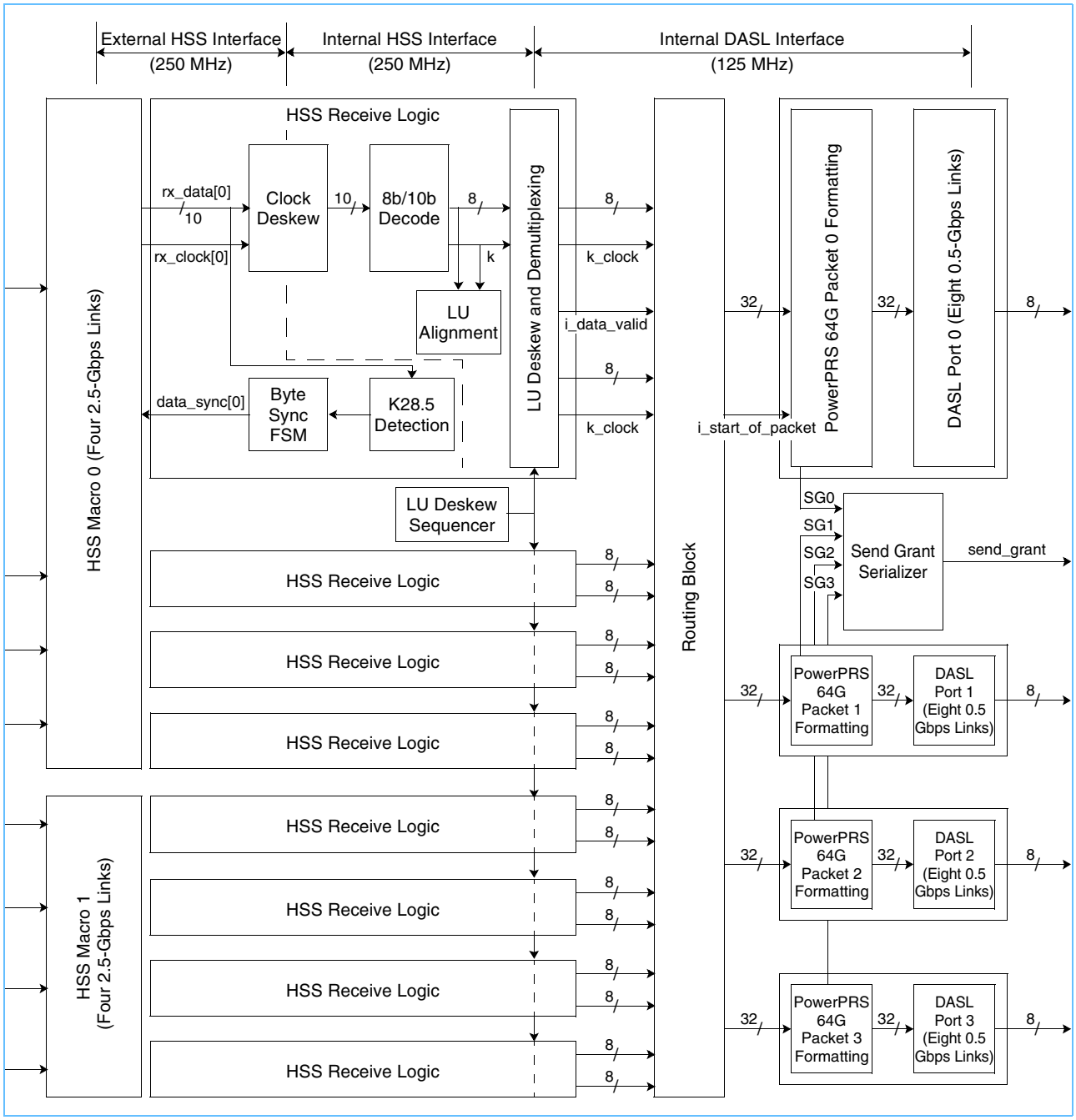
1. Each of the four parallel packets is distributed over two HSS pairs (for example, packet 0 is carried on HSS-0 and HSS-1, packet 1 is carried on HSS-2 and HSS-3, and so forth).
2. LU 0 and LU 2 are carried on the high channel and LU 1 and LU 3 are carried on the low channel.
3. H0 through H4 are packet header bytes.
4. D is x‘CC’.
5. SM is the shared memory grant byte.

The format of the shared memory grant byte carried in egress service packets is identical to the format of the shared memory grant byte carried in egress idle packets (see *Table 3-23* on page 29*)*.

3.3 Ingress Data Flow

Figure 3-10 illustrates ingress data flow through the PowerPRS SCIC.

Figure 3-10. Ingress Data Flow



3.3.1 HSS Receive Logic

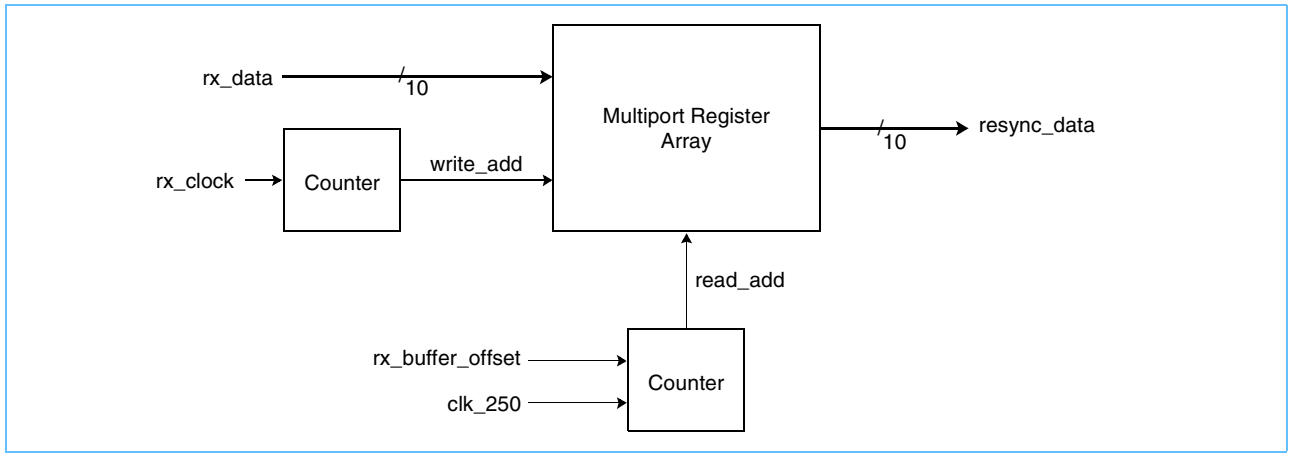
HSS receive logic is comprised of the clock deskew, 8b/10b decode, K28.5 detection, byte synchronization FSM, LU alignment, and LU deskew and demultiplexing blocks. The HSS receive logic is duplicated eight times in the PowerPRS SCIC and is also used in PowerPRS C192 and Q-64G applications. HSS receive logic is inactive (held in reset) when the corresponding HSS Receive Enable Port bit in the *HSS Receive Command Register* (page 71) is set to '0'.

3.3.1.1 Clock Deskew

The HSS macros use eight 10-bit data buses, each with a dedicated receive clock. The eight receive clocks are synchronous because they are generated from the same source, but they are not in phase. The clock deskew block realigns the eight HSS receive clocks with the PowerPRS SCIC internal clock. The internal clock is also synchronous but not in phase.

The clock deskew function is performed using a multiport register array (MPRA) and two counters. As illustrated in *Figure 3-11,* the MPRA input side is fed with a write address generated by an rx_clock-run counter and the output side is fed with a read address generated by an internal clk_250-run counter. The MPRA depth is 16. The offset value between the read and write addresses (the preset value of the read address counter) must be set in the *HSS Receive Buffer Offset Register* (page 79) during the HSS receive logic reset. An offset value of x'8' is recommended.

Figure 3-11. Clock Deskew Block



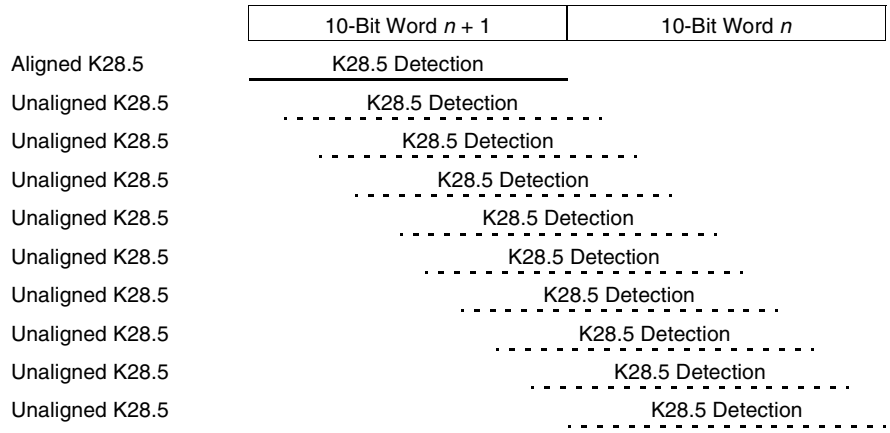
3.3.1.2 8b/10b Decode

The PowerPRS SCIC HSS interface uses Fibre Channel Standard 8b/10b data encoding to improve data transmission and synchronization. The 8b/10b decode block decodes the data and detects code violations. When a code violation is detected, it is reported in the *HSS Error 2 Register* (page 87).

3.3.1.3 K28.5 Detection

K28.5 is an 8b/10b code character used for synchronization. K characters are carried only in idle packets (see *Section 3.2 Packet Format According to Packet Type* on page 18 for byte location). As illustrated in *Figure 3-12* on page 33, the K28.5 detection block collects two consecutive 10-bit data words and decodes the K28.5 characters in each 10-bit combination.

Figure 3-12. K28.5 Detection Block



The presence of unaligned K28.5 characters during the HSS synchronization phase indicates incorrect “byte” boundaries. The HSS macro shifts the boundaries until the K28.5 characters are realigned.

3.3.1.4 Byte Synchronization FSM

The byte synchronization finite state machine (FSM) runs during the HSS synchronization phase. When the FSM receives unaligned K28.5 characters, it sends a request to the HSS macro to shift rx_data by one bit. When the FSM receives seven aligned K28.5 characters and no further unaligned K28.5 characters, it considers the rx_data byte boundaries corrected and the bytes synchronized on the HSS port.

The byte synchronization phase starts automatically when the HSS Receive Enable Port *N* bits are set to ‘1’ in the *HSS Receive Command Register* (page 71). At the end of the byte synchronization phase, the FSM reports a status of ‘01’ in the *HSS Synchronization Status Registers* (page 75) to indicate that byte synchronization is complete for the corresponding HSS port.

The byte synchronization FSM also reports the presence of unaligned K28.5 characters (in idle packets) during the data traffic phase. If one unaligned K28.5 character is detected on a single port, the HSS Receive Invalid K Character bit for the corresponding port is set in the *HSS Error 2 Register* (page 87). If three consecutive unaligned K28.5 characters are detected on a single port, the HSS Receive Synchronization Lost bit of the corresponding port is set in the *HSS Error 2 Register* and, if the Hardware Auto Disable on Synchronization Lost bit of the *HSS Receive Command Register* is set, the i_data_valid signal of the corresponding HSS port is deasserted.

3.3.1.5 LU Alignment

The LU alignment block validates K28.5 (and K28.1) position in all idle packets using packet size information deduced from the LU length. LU alignment is performed during synchronization to validate idle packet format. When LU alignment is complete, the LU alignment block reports a status of ‘10’ to the appropriate *HSS Synchronization Status Register.*

LU alignment validation is also performed on idle packets after synchronization (during the data mode) to validate K28.5 and K28.1 position. If one K28.5 (or K28.1) character is detected in the wrong position on a single port, the error is reported by setting the HSS Receive Invalid K Character bit of the corresponding port in the *HSS Error 2 Register.* If three consecutive K28.5 (or K28.1) characters are detected in the wrong position on

a single port, the HSS Receive Synchronization Lost bit of the corresponding port is set in the *HSS Error 2 Register* (page 87) and, if the Hardware Auto Disable on Synchronization Lost bit of the *HSS Receive Command Register* (page 71) is set, the i_data_valid signal of the corresponding HSS port is deasserted.

3.3.1.6 LU Deskew and Demultiplexing

Due to various delays that accumulate on the eight HSS paths (for example, clock resynchronization, card wiring, and internal HSS macro delay), the LUs are not synchronized when the PowerPRS SCIC receives them. The LU deskew block rearranges the LUs in sequential order (see *Section 3.2 Packet Format According to Packet Type* on page 18) during synchronization, when the LU traffic is comprised of idle packets only.

As illustrated in *Figure 3-13* on page 35, for each HSS port, the K28.5 position is extracted and reported to the local processor via the *HSS Synchronization Status Registers*. Depending on the application, the local processor calculates a positive or negative delay (in the number of cycles) so that the LUs follow the format presented in *Figure 3-4* on page 22. The local processor applies a delay to each port by writing delay values for each port in the *HSS Ingress Deskew Command Register* (page 78). The local processor then verifies that the LU deskew is correct by reading the appropriate *HSS Synchronization Status Register* a second time. Note that, because LU deskew is performed simultaneously on all eight HSS ports, traffic must start at the same time on all eight ports. Starting traffic on a single HSS port is not an option.

The second function of the LU deskew and demultiplexing block is to demultiplex the data format from one 8-bit bus running at 250 MHz to two 8-bit buses (a high channel and a low channel) running at 125 MHz. A k_clock signal, one per channel, indicates the eighth-byte position in each data or idle packet that corresponds to the K28.1 and K28.5 position in idle packets.

When the LU deskew and demultiplexing process is complete on all eight HSS ports, the Receive Data Mode bit in the *HSS Ingress Deskew Command Register* is set to ‘1’. This bit setting effects the correct demultiplexer position, validates the k_clock signals, and asserts the i_data_valid signal that, in turn, enables the routing block and the PowerPRS 64G packet formatting block.

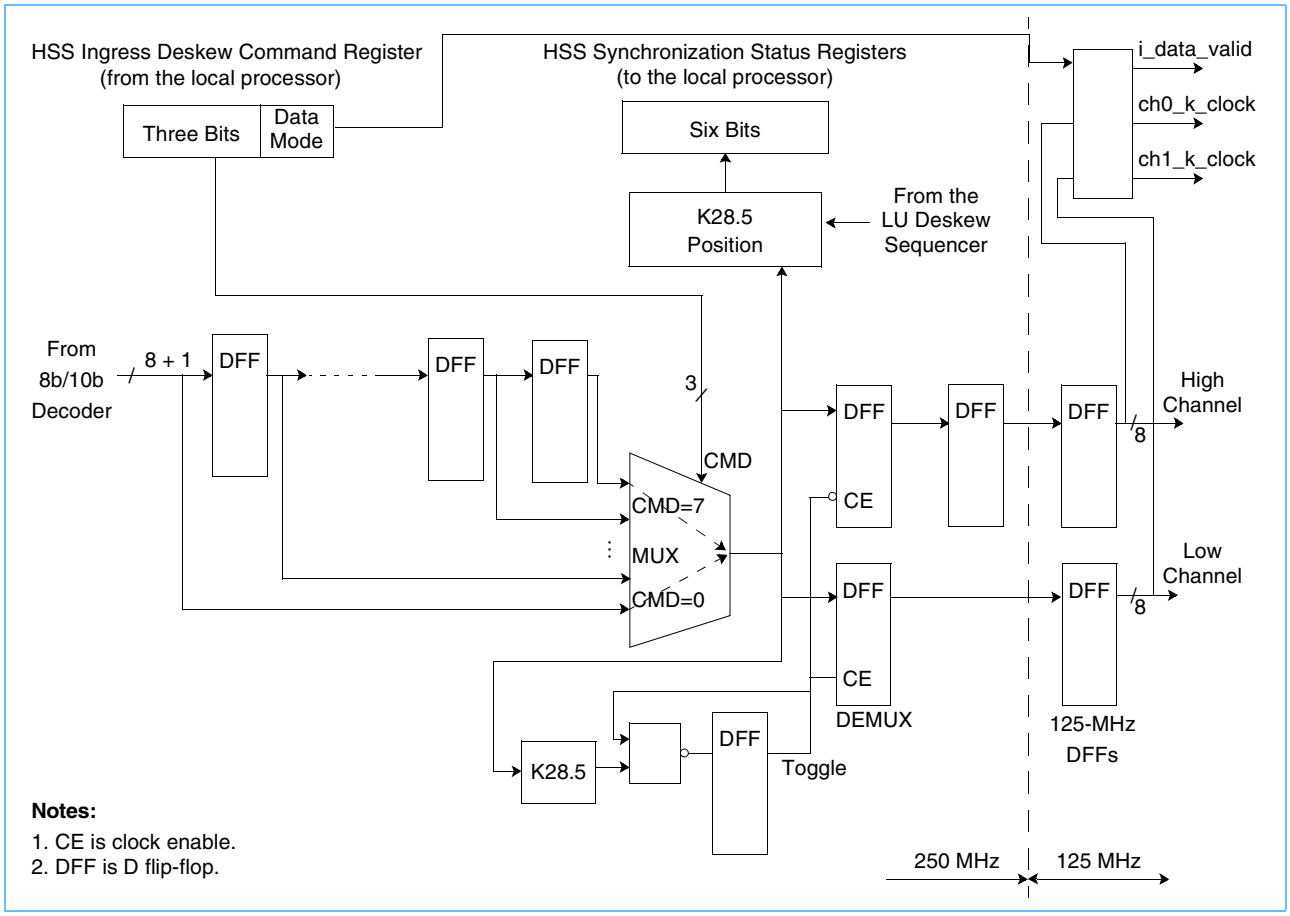
3.3.2 LU Deskew Sequencer

The LU deskew sequencer is a 250-MHz continuously running counter that counts the number of bytes in an LU. The LU deskew sequencer reports counter values to the LU deskew blocks, which use the values to determine relative K28.5 positions.

3.3.3 Routing Block

The routing block routes the bytes from the multiple HSS ports that comprise a single packet to the correct PowerPRS 64G packet formatting block. It also generates i_start_of_packet signals from the K clocks. The four output data buses and the four i_start_of_packet signals are held to ‘0’ when the eight i_data_valid input signals are deasserted.

Figure 3-13. LU Deskew and Demultiplexing Block



3.3.4 PowerPRS 64G Packet Formatting

The PowerPRS 64G packet formatting block performs the following functions on all packets:

- Analyzes the packet qualifier byte to characterize the packet (data, idle, or service).
- Extracts the send grant bits.
- Verifies the header parity bit.
- Calculates and accumulates the CRC value (between two idle packets).

This block performs the following functions on idle and synchronization packets only:

- Forces the payload characters to x‘CC’, with the exception of the idle packet SCC byte, which remains intact.
- Inserts the CRC into the last four packet bytes.

This block performs the following functions on service packets only:

- Inserts the CRC into the last four packet bytes when the Service Packet CRC Insert bit of the *General Configuration Register* (page 62) is set to ‘1’.

3.3.5 Send Grant Serializer

The send grant serializer supports only the send grant per-priority mode. The send grant serializer sends the following frame to the PowerPRS 64G:

0	0	0	0	1	SG0	SG1	SG2	SG3

SG0, SG1, SG2, and SG3 are the send grant values extracted from ingress packets from the PowerPRS C192 (SG0 corresponds to the send grant for priority 0, SG1 corresponds to the send grant for priority 1, and so forth).

Send grant framing runs at 16 ns, half the125-MHz internal/DASL clock speed.

Note: For testing, SG0 through SG3 values can be forced to the fixed values coded in bits 23:20 of the *General Configuration Register* (page 62) by setting the Force Send Grant Frame Value bit (bit 19) to ‘1’.

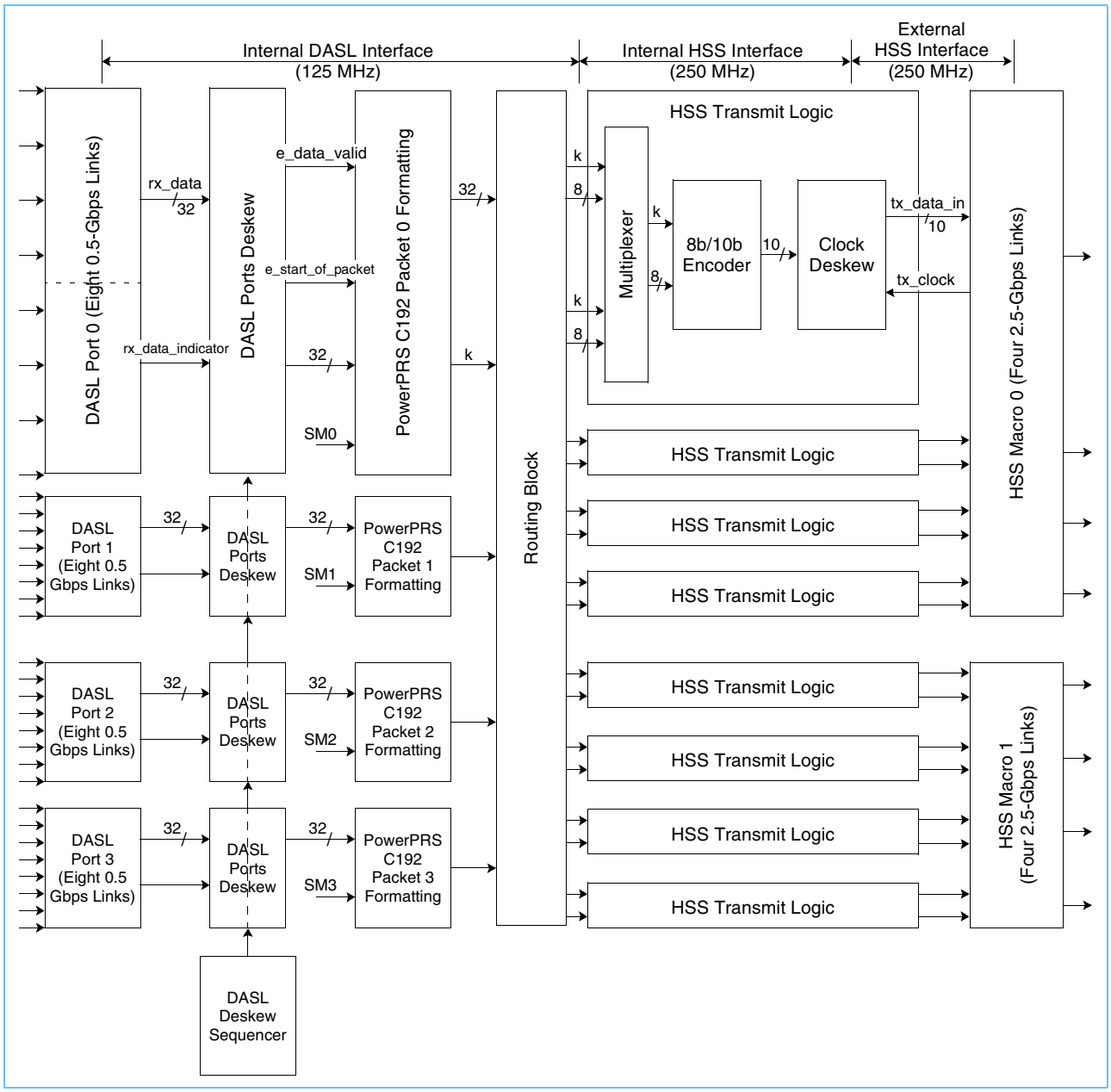
3.3.6 DASL Ports

The PowerPRS SCIC DASL interface implements four transmit ports configured into two subports each. Each transmit port has a 32-bit parallel input bus and an 8-bit serial output bus.

3.4 Egress Data Flow

The egress data flow is basically the ingress data flow in reverse. The functional blocks on the left side of *Figure 3-14* are the same as the functional blocks on the right side of *Figure 3-10* on page 31.

Figure 3-14. Egress Data Flow



3.4.1 DASL Ports

The PowerPRS SCIC DASL interface implements four receive ports configured into two subports each. Each receive port has an 8-bit serial input bus and a 32-bit parallel output bus. The DASL port clock source is the 125-MHz DASL clock, also known as the PowerPRS SCIC internal clock.

Upon completion of DASL receive port synchronization, the DASL ports assert the rx_data_indicator signal to indicate the start of the first valid packet. The rx_data_indicator signal remains active until the DASL port is disabled.

3.4.2 DASL Ports Deskew

The DASL picocode synchronizes the data between the two subports of a DASL port but not between the DASL ports themselves. The DASL ports deskew block rearranges the LUs on the four DASL ports in the sequence described in *Section 3.2 Packet Format According to Packet Type* on page 18. At the end of the DASL synchronization phase, the DASL ports deskew block asserts a repetitive e_start_of_packet signal using the rx_data_indicator signal asserted by the DASL macro and LU length information.

The DASL ports deskew block functions like the LU deskew block on the ingress path. The hardware writes the start-of-packet position for each packet in the *Egress Deskew Status Register* (page 67), and the local processor calculates a positive or negative delay (in number of cycles) to apply to each port. The local processor writes the delay values in the *Egress Deskew Command Register* (page 68) and sets the Egress Data Mode bit to ‘1’, indicating that the egress DASL ports deskew is complete.

The e_start_of_packet and e_data_valid signals are deasserted and the 32-bit data bus is forced to all zeros while the DASL ports deskew process is underway (the Egress Data Mode bit in the *Egress Deskew Command Register* is set to ‘0’).

3.4.3 PowerPRS C192 Packet Formatting

The PowerPRS C192 packet formatting block performs the following functions on all packets:

- Analyzes the packet qualifier byte to characterize the packet (data, idle, service, or synchronization).
- Extracts and verifies the header parity bit.
- Inserts the shared memory grant bits.
- Calculates and inserts a new parity bit.
- Accumulates the CRC.

This block performs the following functions on idle and synchronization packets only:

- Transforms the PowerPRS 64G idle or synchronization packet format to the PowerPRS C192 idle packet format by replacing the x‘CC’ bytes with D28.5 characters and, in the eighth-byte position, with K28.1 or K28.5 characters.
- Compares the accumulated and calculated CRCs.

3.4.4 Routing Block

The routing block routes the bytes from the four PowerPRS C192 packet formatting blocks to the correct HSS ports.

3.4.5 HSS Transmit Logic

The HSS transmit logic is comprised of the multiplexer, 8b/10b encoder, and clock deskew blocks. It is duplicated eight times in the PowerPRS SCIC and is also used in the PowerPRS C192 and Q-64G.

3.4.5.1 Multiplexer

The multiplexer multiplexes the data format from two 8-bit buses running at 125 MHz to one 8-bit bus running at 250 MHz.

3.4.5.2 8b/10b Encoder

The 8b/10b encoder characterizes the eight-bit bus input as either data or control.

3.4.5.3 Clock Deskew

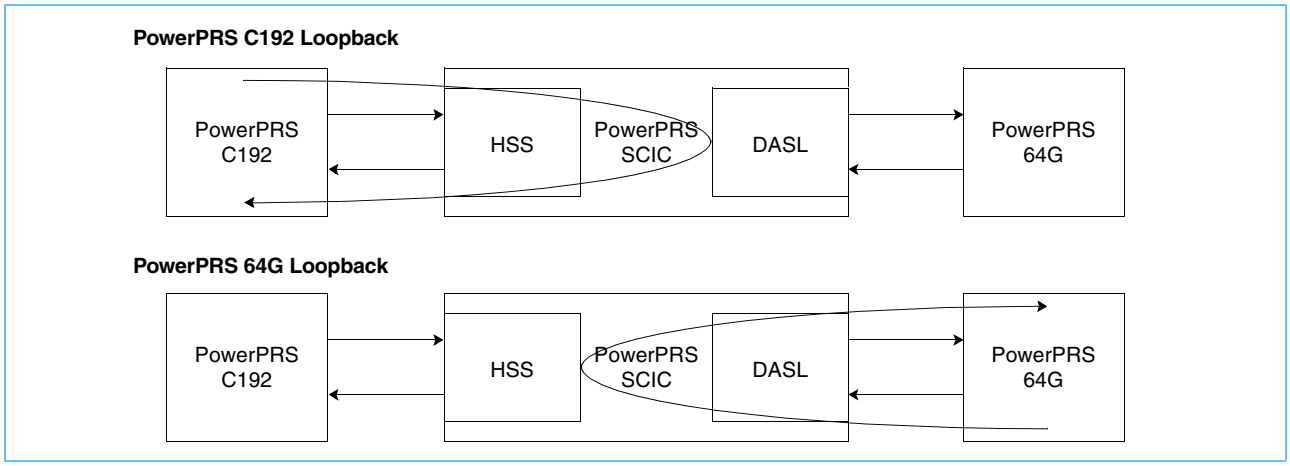
Each HSS transmit port has a dedicated transmit clock. The eight transmit clocks are synchronous because they are generated from the same source, but they are not in phase. The clock deskew block realigns the eight data buses clocked by the PowerPRS SCIC internal clock with the corresponding HSS transmit clock.

The clock deskew function on the egress path is performed using a multiport array register just like the clock deskew function on the ingress path (see *Figure 3-11* on page 32). The only difference between the two is that the tx_buffer_offset signal is applied as a preset value on the write address counter.

3.5 Internal Loopbacks

The PowerPRS SCIC supports the two internal loopbacks illustrated in *Figure 3-15*.

Figure 3-15. Internal Loopbacks

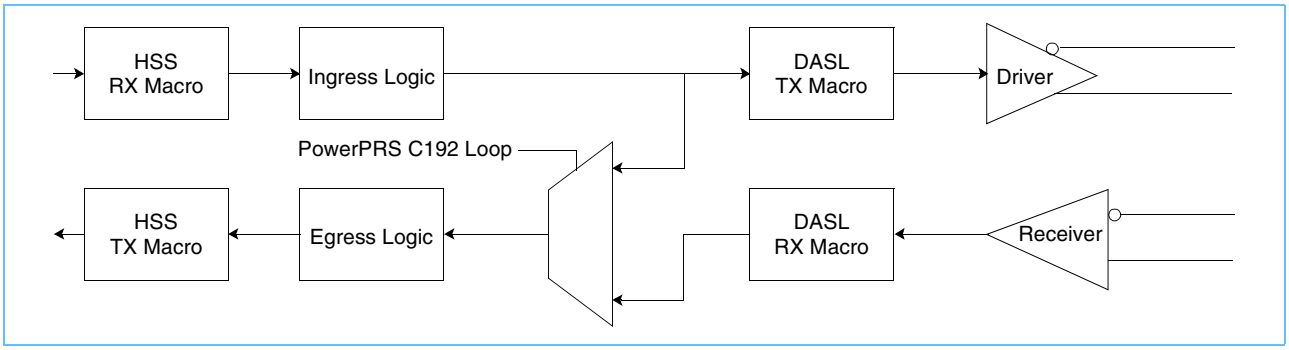


An internal loopback is performed on all ports at the same time.

3.5.1 PowerPRS C192 Loopback

The PowerPRS SCIC DASL transmit macro performs the PowerPRS C192 loopback. As illustrated in *Figure 3-16*, data from the PowerPRS C192 on the ingress path wraps back to the PowerPRS C192 on the egress path instead of continuing across the PowerPRS SCIC DASL interface to the PowerPRS 64G.

Figure 3-16. PowerPRS C192 Loopback



To perform a PowerPRS C192 loopback, the user must:

1. Reset the PowerPRS SCIC (see *Section 6.1 Reset Sequence* on page 111).
2. Set the C192 Loopback bit in the *General Configuration Register* (page 62) to ‘1’.
3. Start the synchronization process.
4. Start traffic when synchronization is complete.

After the PowerPRS C192 loopback is complete, the user must reset the PowerPRS SCIC to restart traffic along the normal data path.

3.5.2 PowerPRS 64G Loopback

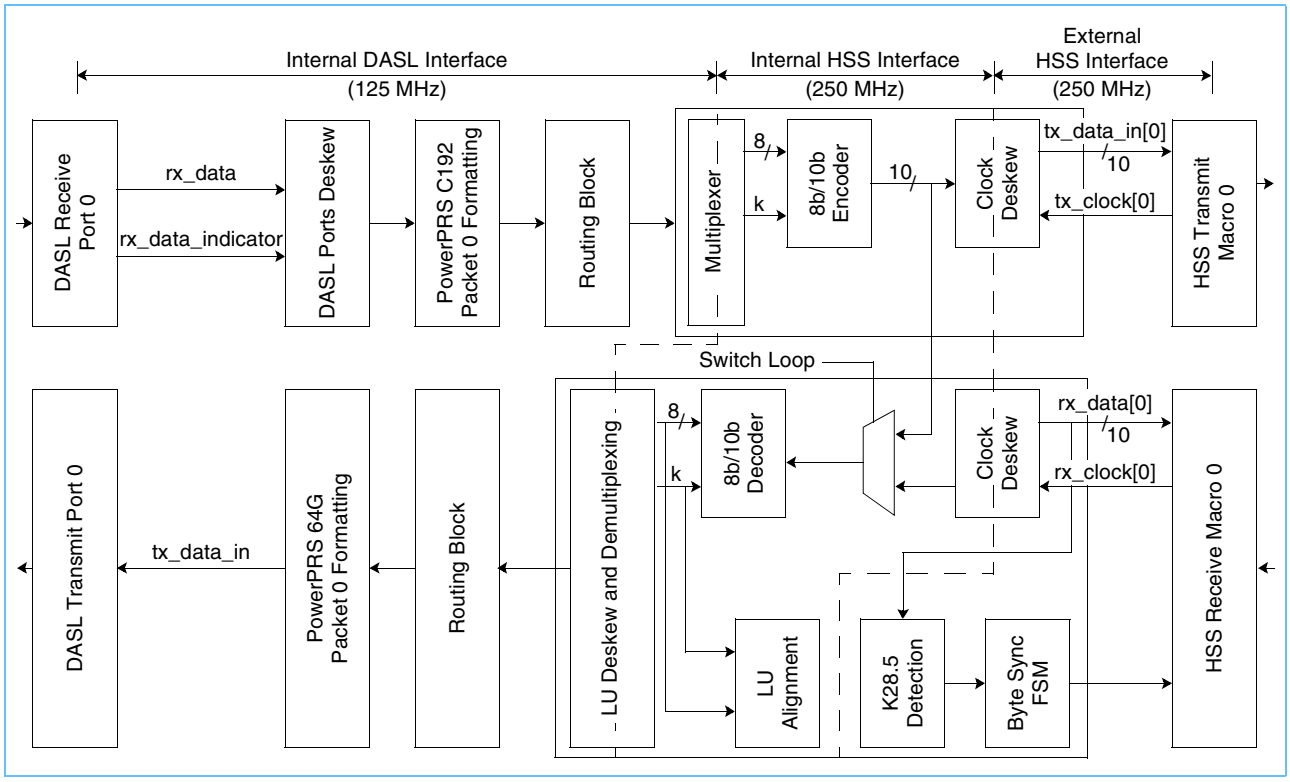
The PowerPRS SCIC HSS receive logic performs the PowerPRS 64G (or switch) loopback. As illustrated in *Figure 3-17* on page 41, data from the PowerPRS 64G on the egress path wraps back to the PowerPRS 64G on the ingress path instead of continuing across the PowerPRS SCIC HSS interface to the PowerPRS C192.

To perform a PowerPRS 64G loopback, the user must:

1. Reset the PowerPRS SCIC (see *Section 6.1 Reset Sequence*).
2. Set the Switch Loopback bit in the *General Configuration Register* to ‘1’.
3. Start the synchronization process.
4. Start traffic when synchronization is complete.

After the PowerPRS 64G loopback is complete, the user must reset the PowerPRS SCIC to restart traffic along the normal data path.

Figure 3-17. PowerPRS 64G Loopback

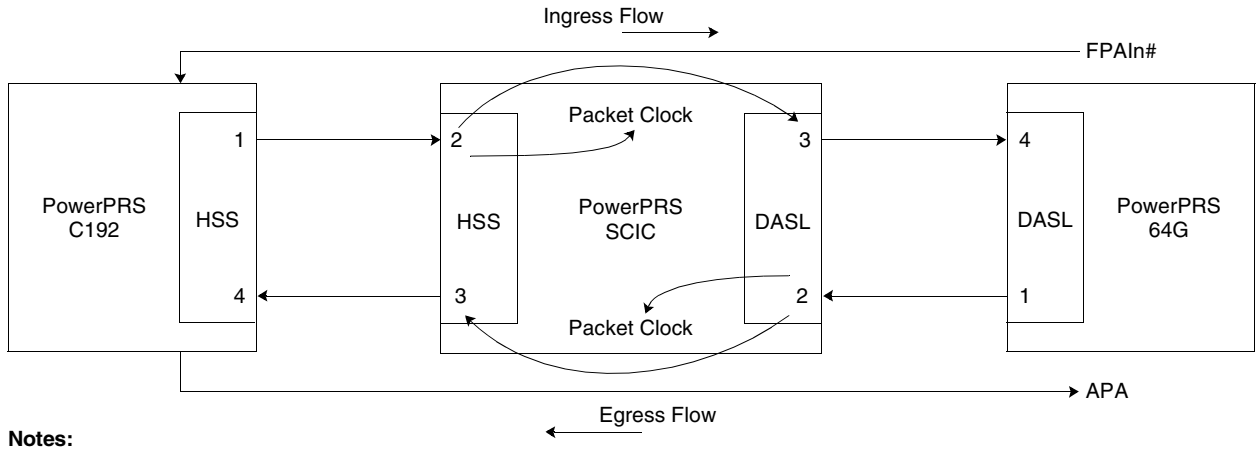


3.6 Synchronization

3.6.1 Global Synchronization

Synchronization between the three devices shown in *Figure 3-18* on page 42 can be performed simultaneously on the ingress and egress paths. *Sections 3.6.1.1* and *3.6.1.2* list the synchronization steps on each path.

Figure 3-18. Global Synchronization



Notes:
APA is adaptor port available.
FPA is fabric port available.

3.6.1.1 Ingress Path

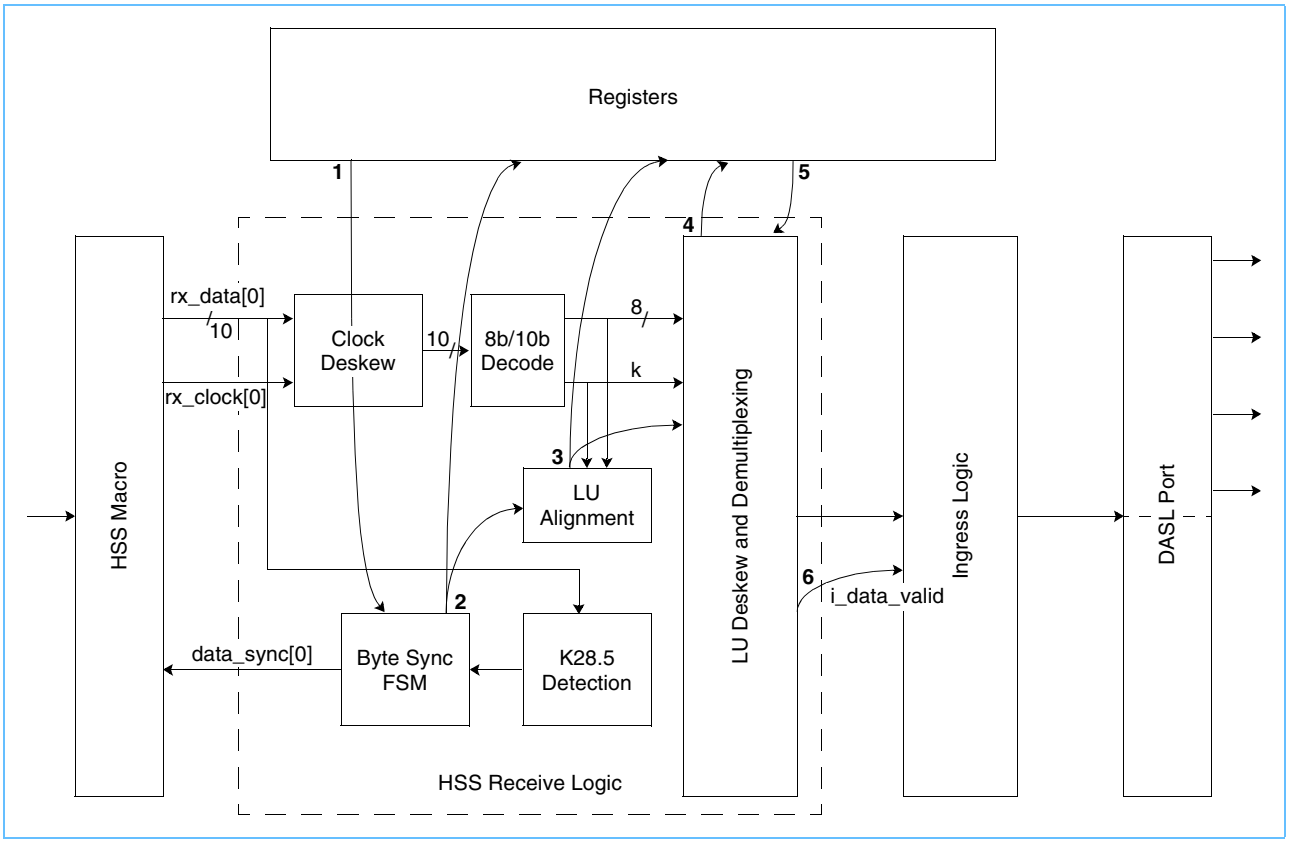
1. When the PowerPRS C192 receives the command to begin synchronization, it starts transmitting idle packets to the PowerPRS SCIC.
2. The PowerPRS SCIC receives the idle packets and starts its internal synchronization process at the byte level (K28.5 detection) and then at the LU level (LU alignment and LU deskew). When packet synchronization is complete, the PowerPRS SCIC generates the packet clock (i_start_of_packet signal).
3. The PowerPRS SCIC transforms the idle packets into synchronization packets and forwards them across the DASL interface to the PowerPRS 64G. Upon receipt of the synchronization packets, the switch begins its synchronization.
4. The PowerPRS 64G completes its synchronization and sends an FPAIn# signal to the PowerPRS C192.
5. The PowerPRS 64G local processor sets the Idle Mode bit in the *HSS Ingress Deskew Command Register* (page 78) to ‘1’, and the PowerPRS SCIC stops transforming idle packets into synchronization packets.

3.6.1.2 Egress Path

1. When the PowerPRS 64G receives the command to begin synchronization, it starts transmitting synchronization packets to the PowerPRS SCIC.
2. When the PowerPRS SCIC detects the onset of synchronization (rx_data_indicator signals asserted for the four DASL ports), the local processor enables the DASL ports deskew process. Once completed, the PowerPRS SCIC can generate the packet clock (e_start_ of_packet signal).
3. The PowerPRS SCIC transforms the synchronization packets into idle packets and forwards them across the HSS interface to the PowerPRS C192. Upon receipt of the idle packets, the PowerPRS C192 begins its synchronization at the byte level (K28.5 detection) and then at the LU level (LU deskew).
4. The PowerPRS C192 completes its synchronization and sends an APA signal to the switch card to stop the PowerPRS 64G from sending synchronization packets to thePowerPRS SCIC.

3.6.2 Internal HSS Interface Synchronization

Figure 3-19. Internal HSS Synchronization



Internal HSS interface synchronization on the ingress (receive) side is comprised of several steps performed by either the PowerPRS SCIC local processor or hardware. These steps must be performed in the following order to ensure successful synchronization:

1. The local processor sets the HSS Receive Enable Port *N* fields in the *HSS Receive Command Register* (page 71) to ‘1’, which starts the byte synchronization FSM and the synchronization process.
2. When byte synchronization is complete, the PowerPRS SCIC reports this status (‘01’) to the *HSS Synchronization Status Registers* (page 75) and to the LU alignment block. LU alignment begins.
3. When LU alignment is complete, the PowerPRS SCIC reports this status (‘10’) to the *HSS Synchronization Status Registers* and to the LU deskew and demultiplexing block.
4. The LU deskew block writes the K28.5 position into the *HSS Synchronization Status Registers* and updates the HSS RX Synchronization Status Port *N* field to ‘11’.
5. When the eight HSS RX Synchronization Status Port fields are set to ‘11’, the local processor calculates the deskew command values and writes them into the *HSS Ingress Deskew Command Register* (page 78) and then sets the Receive Data Mode bit to ‘1’.
6. The LU deskew and demultiplexing block enables the demultiplexer, generates the k_clock, and then generates the i_data_valid signal to indicate to the ingress logic that the data is valid.

3.6.3 Internal DASL Interface Synchronization

Internal DASL interface synchronization on the ingress (receive) side is comprised of the following steps:

1. The local processor starts the DASL receive macro by writing the DASL programming registers (see *Section 5.4* on page 96).
2. When the DASL rx_data_indicator signal is asserted, the PowerPRS SCIC reports it to the *DASL Status Register* (page 99). The local processor uses the DASL signal status and the Start of Packet bit values in the *Egress Deskew Status Register* (page 67) to start the DASL ports deskew process.
3. When the DASL ports deskew process is complete (the local processor has calculated and written the Egress Deskew Command bits in the *Egress Deskew Command Register* [page 68]), the PowerPRS SCIC sets the Egress Data Mode bit to '1' to indicate that the synchronization process is complete and hardware is processing data.

3.7 Clock Overview

3.7.1 Source Clocks

As shown in *Figure 3-20* on page 45, the PowerPRS SCIC has two card-generated source clocks, one running at 62.5 MHz and the other running at 125 MHz. These two synchronous clocks are generated from the same source as the PowerPRS 64G clock. The 62.5-MHz source clock (DaslClockIn_N/P) feeds into the DASL phase-locked loop (PLL), which generates a 500-MHz clock. A counter divides the 500-MHz clock into the 125- and 250-MHz clocks used by the DASL macros and internal logic, respectively. The 125-MHz source clock (HssClockIn_N/P) feeds into the HSS PLL, which generates the 625-MHz clock used by the HSS macros. Each HSS transmit and receive macro has a dedicated PLL that generates its own internal clocks (2.5 GHz, or 1.25 GHz and 250 MHz). Each HSS port has a dedicated 250-MHz transmit and receive clock that is synchronous but not in phase with the clocks on the other HSS ports or the 250-MHz internal clock.

3.7.2 Processor Clock

The processor clock is also generated by the card and is used for both the serial host interface (SHI) and the eight-bit parallel processor interface.

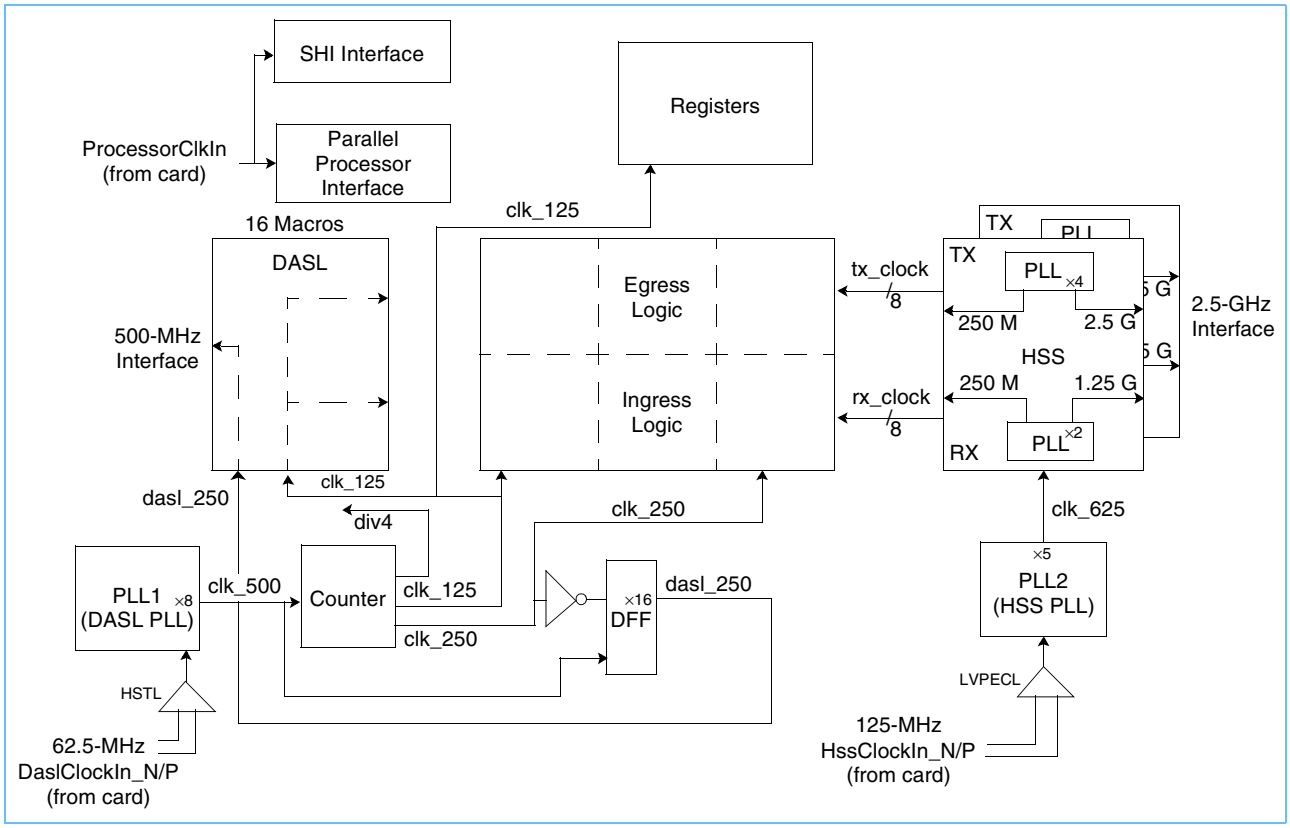
3.7.3 Clock Range

The PowerPRS SCIC range specifications for the two source clocks and the processor clock are presented in *Table 3-24*.

Table 3-24. Clock Range Specifications

Clock	Clock Range (MHz)	
	Minimum	Maximum
DaslClockIn_N DaslClockIn_P	53.125	62.5
HssClockIn_N HssClockIn_P	106.25	125
ProcessorClkIn	25	66

Figure 3-20. PowerPRS SCIC Clocking



4. Programming Interface

The programming interface provides the following functions:

- Read/write access to all PowerPRS SCIC registers for device initialization and control
- DASL picocode downloading
- Error reporting

The PowerPRS SCIC features two programming interfaces:

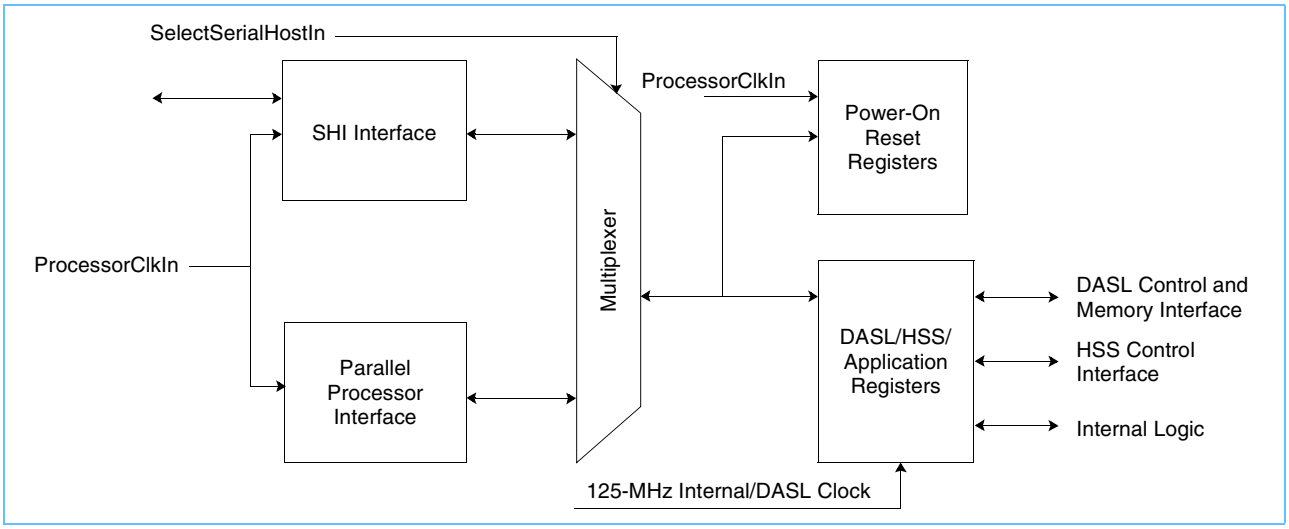
- Serial host interface (SHI)
- Parallel processor interface (eight bits)

Only one programming interface is used per application. The interface is selected using the SelectSerialHostIn pin:

- SelectSerialHostIn = '1': SHI is selected
- SelectSerialHostIn = '0': parallel processor interface is selected

Figure 4-1 presents an overview of the programming interface and register structure. Because only one programming interface can be used in any given application, a single clock input signal (ProcessorClkIn) is used for both interfaces.

Figure 4-1. Global Structure of the Programming Interface and Registers



The programming interface (SHI or eight-bit parallel processor) collects PowerPRS SCIC interrupt signals and forwards them to the attached processor. It monitors all interrupt signals generated by the other PowerPRS SCIC functional blocks and, when an interrupt signal is detected, latches and holds the value until the *Status Register* (page 53) is read and reset.

The InterruptOut# signal driver is low when an interruption is pending (active); otherwise, it is in a high impedance state (inactive). The user must implement a card-level pullup resistor to keep the InterruptOut# signal inactive.

4.1 Serial Host Interface

The serial host interface (SHI) provides access to all PowerPRS SCIC internal resources through three input signals and one output signal:

- ProcessorClkIn
- SHISelectIn#
- SHIDataIn
- SHIDataOut

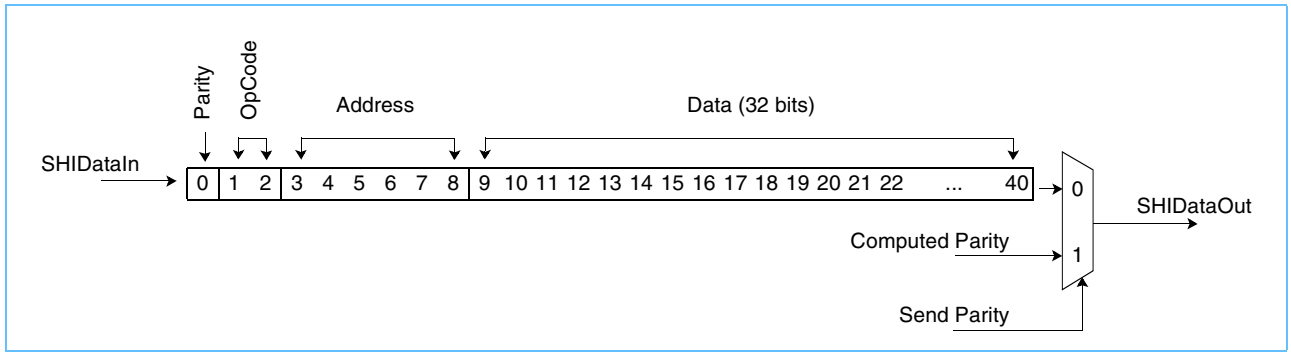
The SHI and internal SHI logic are synchronized to the ProcessorClkIn signal. The processor clock operates at a lower frequency than the system clock and is used for both processor interfaces.

4.1.1 SHI Instruction Register

SHI instructions are decoded into four register fields:

- Parity (1 bit)
- OpCode (2 bits)
- Address (6 bits)
- Data (32 bits)

The parity bit (bit 0) is the most significant bit of the *SHI Instruction Register* and is the last bit scanned into the register.



Bit(s)	Field Name	Description
0	Parity	If the parity is correct, executes the instruction. If the parity is incorrect, inhibits the instruction.
1:2	OpCode	Specifies the SHI command to be executed: 00 No operation (33 bits). Required after a “read status” or “read register” command. Clears the data field. 01 Read status (3 bits). Loads the content of the *Status Register* (page 53) into the data field while simultaneously clearing the *Status Register*. This command requires the “no operation” command to send the *Status Register* content and parity over the SHIDataOut signal and clear the data field. 10 Write register (41 bits). Writes the value of the data field into the register specified by the address field. 11 Read register (9 bits). Loads the content of the register specified by the address field into the data field. This command requires the “no operation” command to send the read result and parity over the SHIDataOut signal and clear the data field.
3:8	Address	Specifies the internal register to be read or written.
9:40	Data	Contains the value to be written or the value that has been returned.

4.1.2 SHI Parity Checking

Each instruction scanned into the *SHI Instruction Register* (page 48) has one bit of parity protection. If a parity error is detected on a received instruction, then the execution of that instruction is inhibited and the SHI Parity Error bit is set to ‘1’ in the *Status Register* (page 53). All *SHI Instruction Register* bits are protected by an odd parity bit. That is, if the SHISelectIn# signal is active during *n* number of ProcessorClkIn cycles, then parity is checked on *n* bits.

4.1.3 SHI Parity Generation

Both incoming and outgoing instructions carry odd parity. Parity is computed for each ProcessorClkIn cycle when the SHISelectIn# signal is active. Computed parity is sent on the SHIDataOut signal when the SHISelectIn# signal is deasserted.

4.1.4 SHI Operation

An SHI instruction operation is invoked when the SHISelectIn# signal is deasserted (set to '0'). Serial data transferred over the SHIDataIn signal is shifted into the *SHI Instruction Register* beginning with the least significant bit of the instruction and ending with the most significant bit. The scan operation is synchronized with the ProcessorClkIn signal. SHI instructions are executed one cycle after the SHISelectIn# signal is deasserted.

4.2 Parallel Processor Interface

The parallel processor interface uses an eight-bit data bus with an eight-bit address bus (MpAddrBusIn[7:0]) and operates in 32-bit burst mode. The parallel processor accesses the PowerPRS SCIC’s 32-bit registers using a four-byte burst:

1. Data bits 7:0
2. Data bits 15:8
3. Data bits 23:16
4. Data bits 31:24

The parallel processor interface provides the handshake protocol necessary to communicate with the attached processor:

- Address bus decoding
- Wait state insertion
- Data bus driver control
- Data and address bus odd parity checking (optional)

The parallel processor interface is clocked by the external processor clock. This clock is not synchronous with the switch fabric clock.

Note: The parallel processor interface requires only six address bits to be compatible with the SHI. Consequently, MpAddrBusIn[7:6] are implemented but not used. These two signal bits can be left unconnected.

5. Register Descriptions

This section describes the registers, including field definitions, that provide the mechanism for PowerPRS SCIC configuration specification and status reporting.

Registers x‘00’ to x‘09’ are power-on registers; they are reset by activating the PowerOnResetIn# signal and are clocked by the ProcessorClkIn signal. These registers can be accessed before the phase-locked loop (PLL) is started or the flush is complete. All bits in the remaining registers are set to ‘0’ during a flush, unless otherwise specified.

Table 5-1 identifies each register and provides the page number where the corresponding description is located. In the register descriptions:

- *Reserved* bits return ‘0’ when read and ignore all write values.
- *Spare* bits can be read or written but do not affect device operation.

Table 5-1. Register Map (Page 1 of 2)

Register Name	Address	Access	Page
Power-On Registers: x‘00’ to x‘09’			
Status Register	x‘00’	Read/Clear and Read Only	53
Internal/DASL PLL Programming Register	x‘01’	Read/Write	55
Internal/DASL PLL Status Register	x‘02’	Read Only	56
HSS PLL Programming Register	x‘03’	Read/Write	56
HSS PLL Status Register	x‘04’	Read Only	57
Reset Register	x‘05’	Read/Write	58
Interrupt Mask Register	x‘06’	Read/Write	59
BIST Counter Register	x‘07’	Read/Write	60
BIST Data Register	x‘08’	Read/Write	60
BIST Select Register	x‘09’	Read/Write	61
Application Registers: x‘0A’ to x‘0F’			
General Configuration Register	x‘0A’	Read/Write	62
Yellow Packet Register	x‘0B’	Read/Clear	64
Packet Error Register	x‘0C’	Read/Clear	66
Egress Deskew Status Register	x‘0D’	Read Only	67
Egress Deskew Command Register	x‘0E’	Read/Write	68
Debug Bus Select Register	x‘0F’	Read/Write	69
HSS Programming Registers: x‘10’ to x‘29’			
HSS Receive Command Register	x‘10’	Read/Write	71
HSS Transmit Command Register	x‘11’	Read/Write	73
HSS Synchronization Status 1 Register	x‘12’	Read Only	75
HSS Synchronization Status 2 Register	x‘13’	Read Only	76
HSS Synchronization Status 3 Register	x‘14’	Read Only	77

Table 5-1. Register Map (Page 2 of 2)

Register Name	Address	Access	Page
HSS Ingress Deskew Command Register	x‘15’	Read/Write	78
HSS Receive Buffer Offset Register	x‘16’	Read/Write	79
HSS Transmit Buffer Offset Register	x‘17’	Read/Write	80
HSS Receive BIST Command Register	x‘18’	Read/Write	81
HSS Transmit BIST Command Register	x‘19’	Read/Write	83
HSS Error 1 Register	x‘1A’	Read Only	85
HSS Error 2 Register	x‘1B’	Read/Clear	87
HSS Force Error Register	x‘1C’	Read/Write	89
HSS Power Level Register	x‘1D’	Read/Write	90
HSS FIR C0 Register	x‘1E’	Read/Write	91
HSS FIR C1 Register	x‘1F’	Read/Write	92
HSS FIR C2 Register	x‘20’	Read/Write	93
HSS FIR C3 Register	x‘21’	Read/Write	94
HSS Phase Rotator/Sample Registers	x‘22 to x‘29’	Read Only and Read/Write	95
DASL Programming Registers: x‘30’ to x‘3E’			
DASL Output Driver Enable Register	x‘30’	Read/Write	96
Output Port Enable Register	x‘31’	Read/Write	97
Input Port Enable Register	x‘33’	Read/Write	98
DASL Status Register	x‘34’	Read Only	99
SDC RLOS Enable Register	x‘35’	Read/Write	100
DASL Synchronization Hunt Register	x‘36’	Read/Write	101
Picoprocessor Instruction Memory Access Register	x‘37’	Read/Write	102
DASL Configuration Register	x‘38’	Read/Write	103
DASL Port Error/Quality Register	x‘39’	Read Only	104
DASL Port Quality Mask Register	x‘3A’	Read/Write	105
SDC Resource Control Register	x‘3B’	Read/Write	106
SDC Resource Address Register	x‘3C’	Read/Write	108
SDC Resource Data Register	x‘3D’	Read/Write	108
SDC Status Register	x‘3E’	Read Only	109

5.1 Power-On Registers

5.1.1 Status Register

The PowerPRS SCIC *Status Register* reports self-test status and error-related events. It is accessed by one of the following methods:

- Serial host interface (SHI) read status command (see the *SHI Instruction Register* [page 48])
- Parallel processor read command at address x‘0’ (see *Section 4.2 Parallel Processor Interface* on page 49)

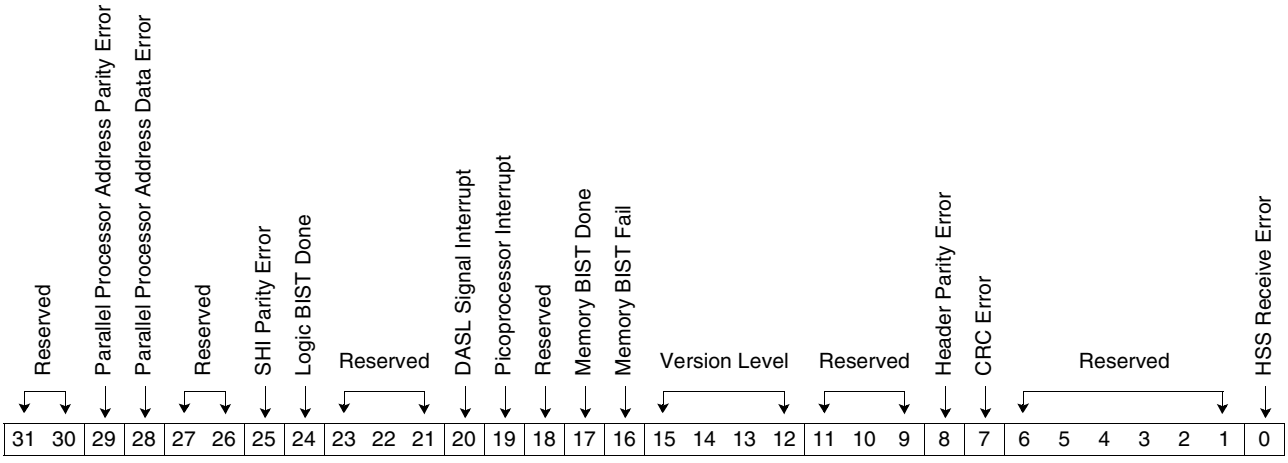
Most of the bits in this register send interrupt signals to the local processor (exceptions are identified in the bit descriptions below). An interrupt signal is masked by setting the corresponding bit in the *Interrupt Mask Register* (page 59). When an event for which the interrupt mask bit is set to '1' occurs, the corresponding bit in this register is set to ‘1’ but an InterruptOut# signal is not asserted. The InterruptOut# signal, which interrupts the local processor, is asserted only if the Global Interrupt Mask bit *is not* set and the Off-Chip Driver Enable bit *is* set in the *Reset Register* (page 58).

Note: Bits 8, 7, 0 are reset when the register that logs the corresponding error is read.

Address x‘00’

Access Type Read/Clear (bits 29, 28, 25, 20, and 19)
Read Only (bits 24, 17, 16, 15:12, 8, 7, and 0)

Reset Value ‘0000 0000 0000 0000 0011 0000 0000 0000’



Bit(s)	Field Name	Description
31:30	Reserved	Reserved.
29	Parallel Processor Address Parity Error	Set to ‘1’ when a parity error is detected on the address during a processor instruction.
28	Parallel Processor Data Parity Error	Set to ‘1’ when a parity error is detected on the data during a processor write instruction.
27:26	Reserved	Reserved.
25	SHI Parity Error	Set to ‘1’ when the serial host interface detects a parity error in the instruction.

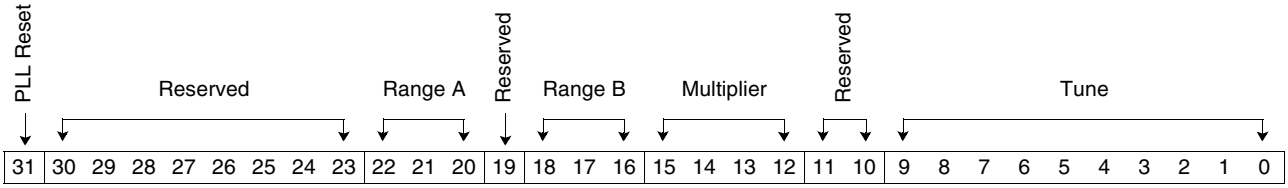
Bit(s)	Field Name	Description
24	Logic BIST Done	Set to ‘1’ when the built-in self-test (BIST) controller completes internal processing after a logic BIST request command. This command is issued by setting the Logic BIST Requested bit in the *Reset Register* (page 58). Bits 23:16 and 11:0 are forced to ‘0’ while the BIST is running. This bit does not generate an interrupt.
23:21	Reserved	Reserved.
20	DASL Signal Interrupt	Set to ‘1’ when an interrupt is generated because a DASL Signal Lost Port *N* bit in the *DASL Status Register* (page 99) has changed.
19	Picoprocessor Interrupt	Set to ‘1’ when the internal processor generates an interrupt.
18	Reserved	Reserved.
17	Memory BIST Done	Set to ‘1’ when the BIST controller completes internal processing after a memory BIST request command. This command is issued by setting the Memory BIST Requested bit in the *Reset Register*. This bit does not generate an interrupt.
16	Memory BIST Fail	Set to ‘1’ when, after completion of the memory BIST process, at least one memory BIST check failed on one RAM. This bit is valid only if the Memory BIST Done bit is asserted. This bit does not generate an interrupt.
15:12	Version Level	Indicates the current version of the device.
11:9	Reserved	Reserved.
8	Header Parity Error	Set to ‘1’ when a parity error is detected in an incoming packet header. The port number and packet direction (ingress or egress) are identified in the *Packet Error Register* (page 66).
7	CRC Error	Set to ‘1’ when a cyclic redundancy check (CRC) error is detected in an idle packet trailer byte. The input port is identified in the *Packet Error Register.*
6:1	Reserved	Reserved.
0	HSS Receive Error	Set to ‘1’ when a signal lost, code violation, invalid K character, or synchronization lost error has occurred on a high-speed SerDes (HSS) receive port. The error type and port number are identified in either the *HSS Error 1 Register* (page 85) or the *HSS Error 2 Register* (page 87).

5.1.2 Internal/DASL PLL Programming Register

Address x‘01’

Access Type Read/Write

Reset Value ‘1000 0000 0000 0000 0000 0000 0000 0000’



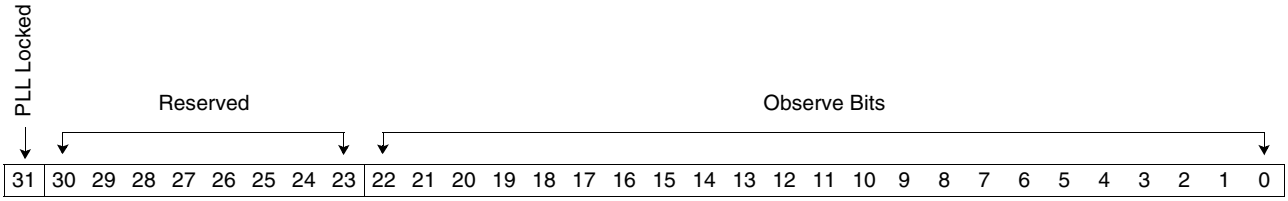
Bit(s)	Field Name	Description
31	PLL Reset	When set to ‘1’, holds the PLL in a reset state. This bit is released when the reference clock (DaslClockIn_N/P) is stable and the PLL is correctly programmed.
30:23	Reserved	Reserved.
22:20	Range A	Used to select the PLL output frequency. These bits must be set to ‘111’.
19	Reserved	Reserved.
18:16	Range B	Not used. These bits must be set to ‘111’.
15:12	Multiplier	Defines the PLL feedback divider. These bits must be set to ‘0001’.
11:10	Reserved	Reserved.
9:0	Tune	Used to optimize PLL stability and jitter. These bits must be set to ‘00 1101 0010’.

5.1.3 Internal/DASL PLL Status Register

Address x‘02’

Access Type Read Only

Reset Value ‘u000 0000 0uuu uuuu uuuu uuuu uuuu uuuu’, where ‘u’ = undefined



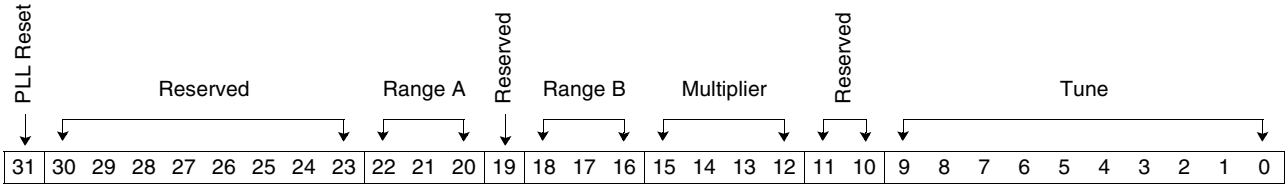
Bit(s)	Field Name	Description
31	PLL Locked	When set to ‘1’, the feedback clock (div4) is in phase with the reference clock (DaslClockIn_N/P).
30:23	Reserved	Reserved.
22:0	Observe Bits	Twenty-three bits used for testing.

5.1.4 HSS PLL Programming Register

Address x‘03’

Access Type Read/Write

Reset Value ‘1000 0000 0000 0000 0000 0000 0000 0000’



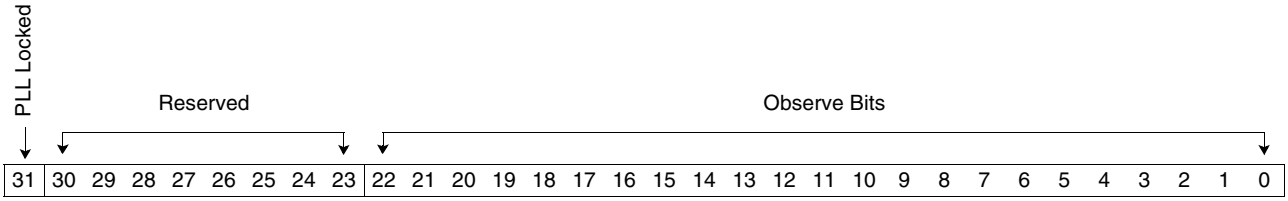
Bit(s)	Field Name	Description
31	PLL Reset	When set to ‘1’, holds the PLL in a reset state. This bit is released when the reference clock (HssClockIn_N/P) is stable and the PLL is correctly programmed.
30:23	Reserved	Reserved.
22:20	Range A	Used to select the PLL frequency. These bits must be set to ‘011’.
19	Reserved	Reserved.
18:16	Range B	Not used. These bits must be set to ‘011’.
15:12	Multiplier	Defines the PLL feedback divider. These bits must be set to ‘1010’.
11:10	Reserved	Reserved.
9:0	Tune	Used to optimize PLL stability and jitter. These bits must be set to ‘01 1111 0110’.

5.1.5 HSS PLL Status Register

Address x‘04’

Access Type Read Only

Reset Value ‘u000 0000 0uuu uuuu uuuu uuuu uuuu uuuu’, where ‘u’ = undefined



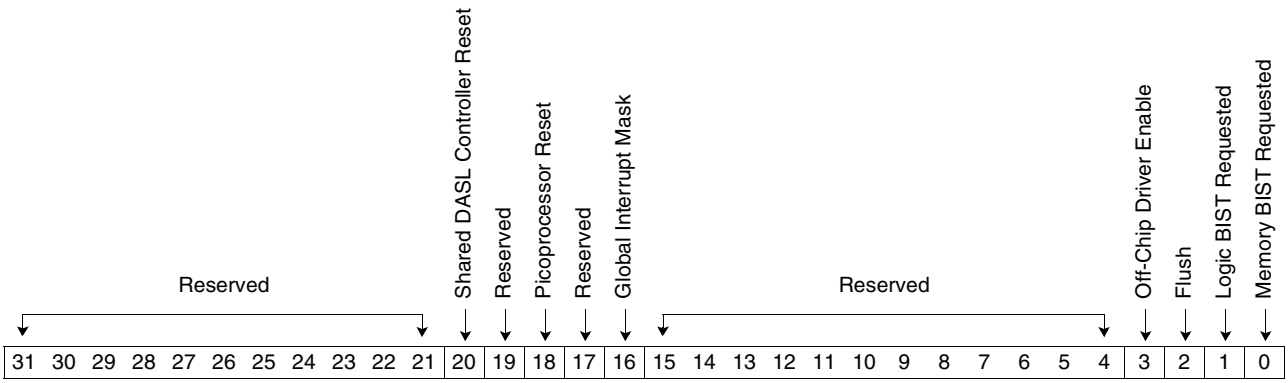
Bit(s)	Field Name	Description
31	PLL Locked	When set to ‘1’, the feedback clock is in phase with the reference clock (HssClockIn_N/P).
30:23	Reserved	Reserved.
22:0	Observe Bits	Twenty-three bits used for testing.

5.1.6 Reset Register

Address x‘05’

Access Type Read/Write

Reset Value ‘0000 0000 0001 0101 0000 0000 0000 0100’



Bit(s)	Field Name	Description
31:21	Reserved	Reserved.
20	Shared DASL Controller Reset	When set to ‘1‘, forces the DASL logic into a reset state. This bit must remain asserted until the *DASL Configuration Register* (page 103) is fully programmed.
19	Reserved	Reserved.
18	Picoprocessor Reset	When set to ‘1’, forces the internal picoprocessor into a reset state. This bit must remain asserted until the instruction memory is fully programmed.
17	Reserved	Reserved.
16	Global Interrupt Mask	1 Disables event- and error-generated interrupts to the local processor. The InterruptOut# signal (active low) is tristated and pulled up with an external resistor. The *Status Register* (page 53) bits are asserted when the corresponding events or errors occur. 0 Enables event- and error-generated interrupts to the local processor.
15:4	Reserved	Reserved.
3	Off-Chip Driver Enable	1 Enables all off-chip drivers until another configuration disables them. 0 Disables (tristates) all drivers except the SHI and parallel processor interface, which remain enabled.
2	Flush	When set to ‘1’, keeps all device logic except the SHI and parallel processor interface internal logic in a reset state.
1	Logic BIST Requested	When set to ‘1’, enables the BIST controller to start executing the internal logic BIST as soon as the flush bit is deasserted. This bit can only be asserted while the flush bit is active. Logic BIST completion is reported in the *Status Register*. See*Section 6.2 Logic BIST Execution Sequence* on page 111 for more information.
0	Memory BIST Requested	When set to ‘1‘, enables the BIST controller to start executing the memory BIST as soon as the flush bit is deasserted. This bit can only be asserted while the flush bit is active. Memory BIST completion and results are reported in the *Status Register*. See*Section 6.3 Memory BIST Execution Sequence* on page 112 for more information.

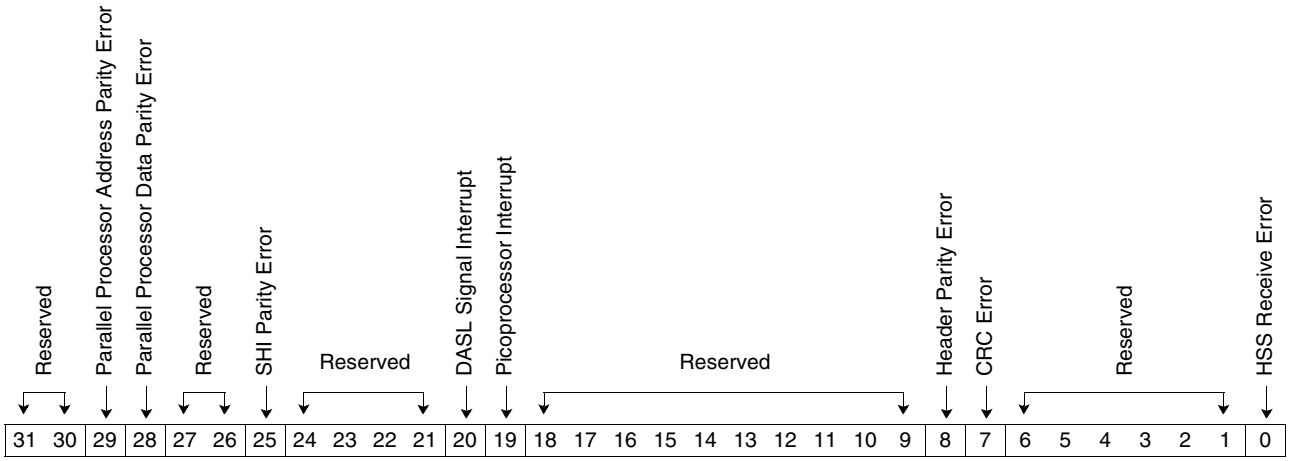
5.1.7 Interrupt Mask Register

This register sets interrupt masks for the *Status Register* (page 53) application bits. Note that, when an event for which the mask bit is set to '1' occurs, the corresponding bit in the *Status Register* is set to '1' but the InterruptOut# signal is not asserted. For information about an event or error masked herein, see the *Status Register* bit descriptions.

Address x'06'

Access Type Read/Write

Reset Value '0000 0000 0000 0000 0000 0000 0000 0000'



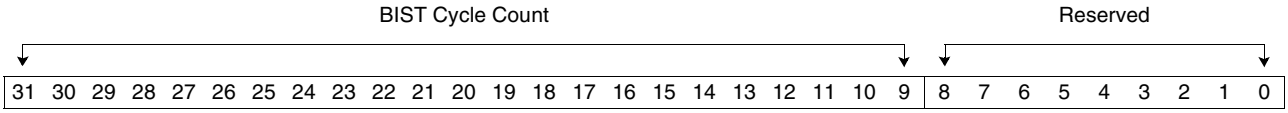
Bit(s)	Field Name	Description
31:30	Reserved	Reserved.
29	Parallel Processor Address Parity Error	When set to '1', masks this interrupt.
28	Parallel Processor Data Parity Error	When set to '1', masks this interrupt.
27:26	Reserved	Reserved.
25	SHI Parity Error	When set to '1', masks this interrupt.
24:21	Reserved	Reserved.
20	DASL Signal Interrupt	When set to '1', masks this interrupt.
19	Picoprocessor Interrupt	When set to '1', masks this interrupt.
18:9	Reserved	Reserved.
8	Header Parity Error	When set to '1', masks this interrupt.
7	CRC Error	When set to '1', masks this interrupt.
6:1	Reserved	Reserved.
0	HSS Receive Error	When set to '1', masks this interrupt.

5.1.8 BIST Counter Register

Address x‘07’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:9	BIST Cycle Count	Specifies the number of BIST cycles to be performed.
8:0	Reserved	Reserved.

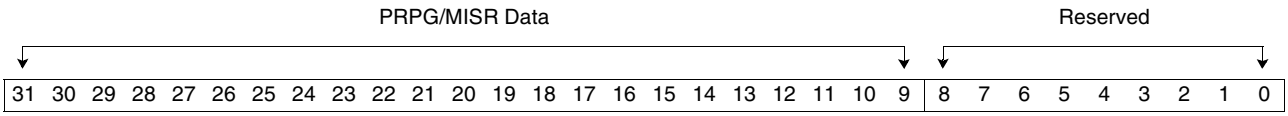
5.1.9 BIST Data Register

This register, along with the *BIST Select Register* (page 61), provides indirect access to the internal pseudo-random pattern generator (PRPG) and multiple input signature (MISR) registers.

Address x‘08’

Access Type Read/Write

Reset Value Undefined



Bit(s)	Field Name	Description
31:9	PRPG/MISR Data	Contains the data that has been or will be exchanged using the settings provided in the *BIST Select Register.*
8:0	Reserved	Reserved.

5.1.10 BIST Select Register

This register, along with the *BIST Data Register* (page 60), provides indirect access to the internal PRPG and MISR registers.

Write access to an internal PRGP or MISR register requires two SHI commands:

1. Write the BIST Register Select field in this register with the value specifying which internal PRPG or MISR register is to be accessed.
2. Write the *BIST Data Register* with the value desired for the internal PRPG or MISR register specified in step 1. The internal PRPG or MISR register is loaded.

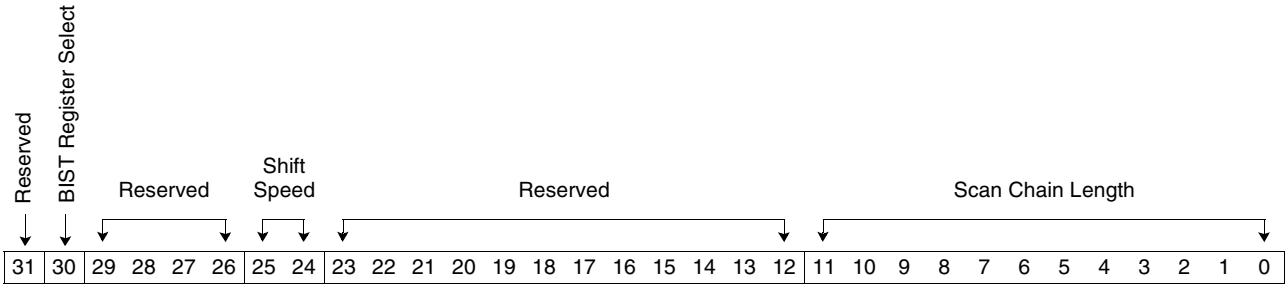
Read access to an internal PRGP or MISR register requires two SHI commands:

1. Write the BIST Register Select field in this register with the value specifying which internal PRPG or MISR register is to be accessed.
2. Read the *BIST Data Register*. The value for the internal PRPG or MISR register specified in step 1 is returned.

Address x‘09’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	Reserved	Reserved.
30	BIST Register Select	Specifies the BIST register: 0 PRPG 1 MISR
29:26	Reserved	Reserved.
25:24	Shift Speed	Defines the delay between the A and B clock pulses while shifting occurs during the BIST: 00 8 ns 01 16 ns 10 24 ns 11 32 ns
23:12	Reserved	Reserved.
11:0	Scan Chain Length	Specifies the scan chain length.

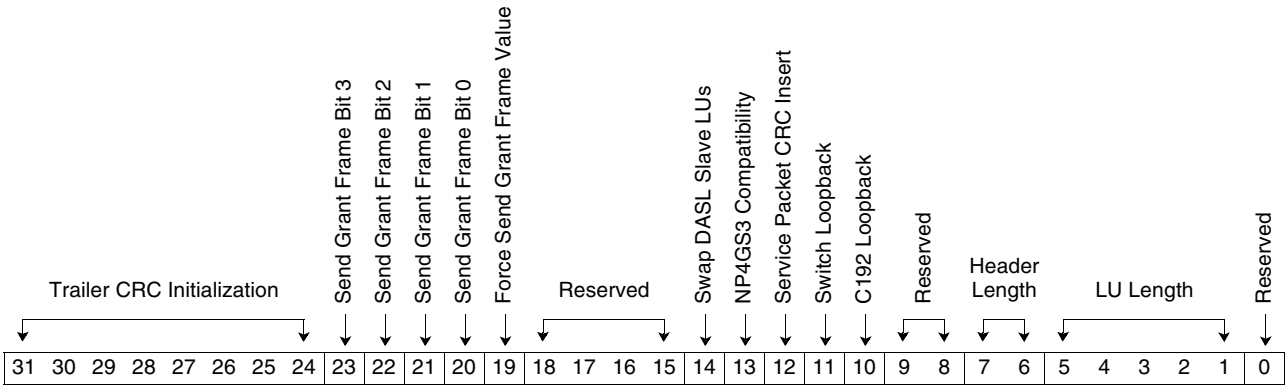
5.2 Application Registers

5.2.1 General Configuration Register

Address x‘0A’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:24	Trailer CRC Initialization	Specifies the initialization value to be used for the eight-bit idle packet trailer CRC: LU Length — Trailer CRC Initialization Register 16 — x‘D0’ 17 — x‘DD’ 18 — x‘04’ 19 — x‘FA’ 20 — x‘07’
23	Send Grant Frame Bit 3	When bit 19 is set to ‘1’, specifies the value forced into bit 3 of the ingress packet send grant frame.
22	Send Grant Frame Bit 2	When bit 19 is set to ‘1’, specifies the value forced into bit 2 of the ingress packet send grant frame.
21	Send Grant Frame Bit 1	When bit 19 is set to ‘1’, specifies the value forced into bit 1 of the ingress packet send grant frame.
20	Send Grant Frame Bit 0	When bit 19 is set to ‘1’, specifies the value forced into bit 0 of the ingress packet send grant frame.
19	Force Send Grant Frame Value	0 The send grant values decoded from ingress packets received from the PowerPRS C192 comprise the send grant frame. 1 The send grant frame values defined in bits 23:20 comprise the send grant frame.
18:15	Reserved	Reserved.
14	Swap DASL Slave LUs	Indicates whether or not slave LU 2 is swapped with slave LU 3 on the DASL slave port: 0 The two DASL slave LUs *are not* swapped (compatible with the IBM Packet Routing Switch Serial Interface Converter). 1 The two DASL slave LUs *are* swapped (compatible with the IBM PowerNP NP4GS3 Network Processor). **Note:** In all applications, the master LU is always swapped with slave LU 1 on the DASL master port.
13	NP4GS3 Compatibility	0 Standard applications 1 NP4GS3 applications **Note:** This bit is set according to the bit position of the send grant in the packet qualifier byte of ingress data packets (see *Tables 3-1* and *3-4* on page 20) and the shared memory grant in the packet qualifier byte of egress data packets (see *Tables 3-17* and *3-19* on page 26).

Bit(s)	Field Name	Description
12	Service Packet CRC Insert	0 The CRC *is not* inserted in ingress service packets. 1 The CRC *is* inserted in ingress service packets. This field applies only to ingress service packets; egress service packets do not carry CRC values.
11	Switch Loopback	When set to '1', initiates the switch loopback procedure (see *Section 3.5.2 PowerPRS 64G Loopback* on page 40).
10	C192 Loopback	When set to '1', initiates the PowerPRS C192 loopback procedure (see *Section 3.5.1 PowerPRS C192 Loopback* on page 40).
9:8	Reserved	Reserved.
7:6	Header Length	Specifies the packet header length: 00 Five bytes 01 Three bytes 1*x* Two bytes
5:1	LU Length	Specifies the LU length: 10000 16 bytes 10001 17 bytes 10010 18 bytes 10011 19 bytes 10100 20 bytes The LU length is one-fourth the packet length. For example, the LU length is 16 bytes for a 64-byte packet.
0	Reserved	Reserved.

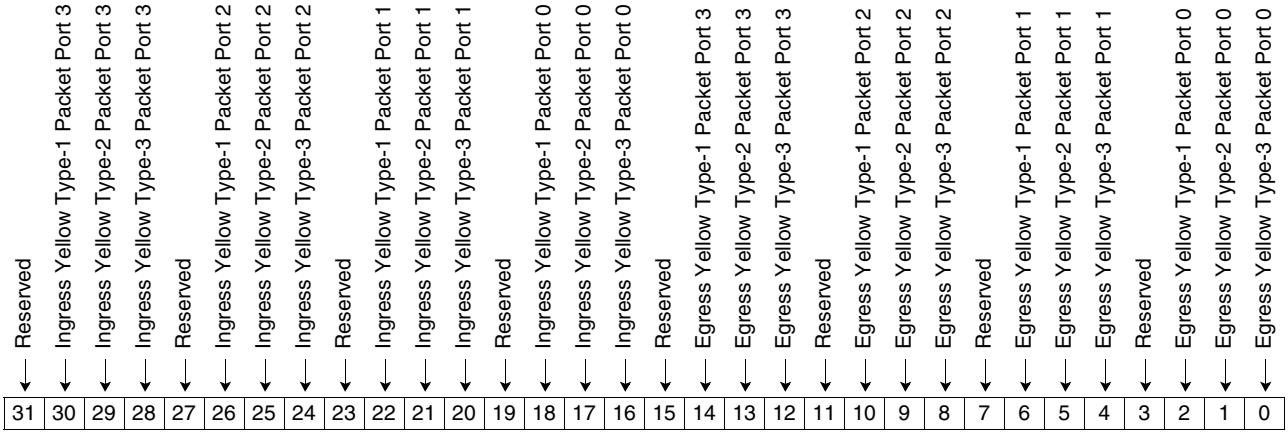
5.2.2 Yellow Packet Register

This register reports the detection of service packets (also called yellow packets) on the ingress and egress paths. The three types of service packets are described in *Section 3.1.3 Service Packets* on page 17.

Address x‘0B’

Access Type Read/Clear

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	Reserved	Reserved.
30	Ingress Yellow Type-1 Packet Port 3	When set to ‘1’, at least one yellow type-1 service packet has been detected on the ingress port.
29	Ingress Yellow Type-2 Packet Port 3	When set to ‘1’, at least one yellow type-2 service packet has been detected on the ingress port.
28	Ingress Yellow Type-3 Packet Port 3	When set to ‘1’, at least one yellow type-3 service packet has been detected on the ingress port.
27	Reserved	Reserved.
26	Ingress Yellow Type-1 Packet Port 2	See the description for bit 30.
25	Ingress Yellow Type-2 Packet Port 2	See the description for bit 29.
24	Ingress Yellow Type-3 Packet Port 2	See the description for bit 28.
23	Reserved	Reserved.
22	Ingress Yellow Type-1 Packet Port 1	See the description for bit 30.
21	Ingress Yellow Type-2 Packet Port 1	See the description for bit 29.
20	Ingress Yellow Type-3 Packet Port 1	See the description for bit 28.
19	Reserved	Reserved.

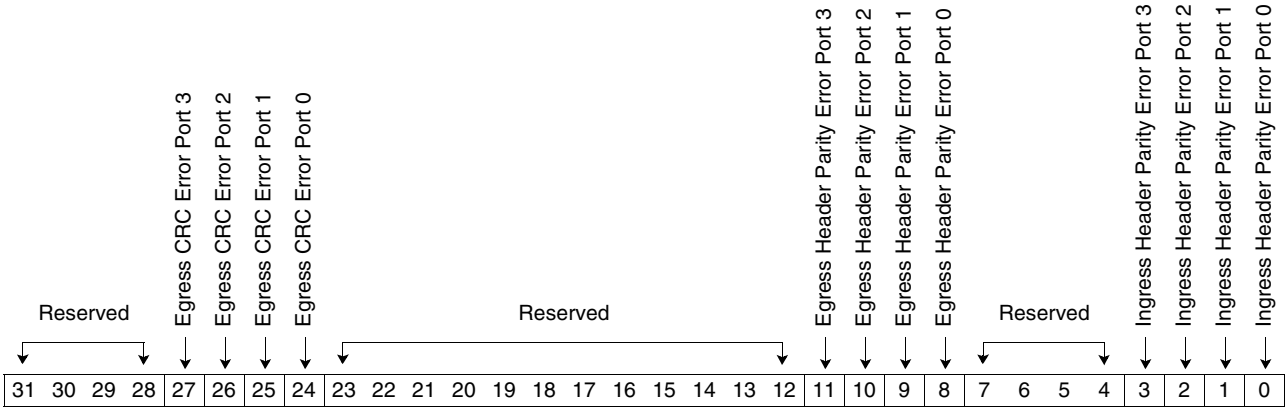
Bit(s)	Field Name	Description
18	Ingress Yellow Type-1 Packet Port 0	See the description for bit 30.
17	Ingress Yellow Type-2 Packet Port 0	See the description for bit 29.
16	Ingress Yellow Type-3 Packet Port 0	See the description for bit 28.
15	Reserved	Reserved.
14	Egress Yellow Type-1 Packet Port 3	When set to ‘1’, at least one yellow type-1 service packet has been detected on the egress port.
13	Egress Yellow Type-2 Packet Port 3	When set to ‘1’, at least one yellow type-2 service packet has been detected on the egress port.
12	Egress Yellow Type-3 Packet Port 3	When set to ‘1’, at least one yellow type-3 service packet has been detected on the egress port.
11	Reserved	Reserved.
10	Egress Yellow Type-1 Packet Port 2	See the description for bit 14.
9	Egress Yellow Type-2 Packet Port 2	See the description for bit 13.
8	Egress Yellow Type-3 Packet Port 2	See the description for bit 12.
7	Reserved	Reserved.
6	Egress Yellow Type-1 Packet Port 1	See the description for bit 14.
5	Egress Yellow Type-2 Packet Port 1	See the description for bit 13.
4	Egress Yellow Type-3 Packet Port 1	See the description for bit 12.
3	Reserved	Reserved.
2	Egress Yellow Type-1 Packet Port 0	See the description for bit 14.
1	Egress Yellow Type-2 Packet Port 0	See the description for bit 13.
0	Egress Yellow Type-3 Packet Port 0	See the description for bit 12.

5.2.3 Packet Error Register

Address x‘0C’

Access Type Read/Clear

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:28	Reserved	Reserved.
27	Egress CRC Error Port 3	When set to ‘1’, at least one CRC error has been detected on the egress port.
26	Egress CRC Error Port 2	See the description for bit 27.
25	Egress CRC Error Port 1	See the description for bit 27.
24	Egress CRC Error Port 0	See the description for bit 27.
23:12	Reserved	Reserved.
11	Egress Header Parity Error Port 3	When set to ‘1’, at least one header parity error has been detected on the egress port.
10	Egress Header Parity Error Port 2	See the description for bit 11.
9	Egress Header Parity Error Port 1	See the description for bit 11.
8	Egress Header Parity Error Port 0	See the description for bit 11.
7:4	Reserved	Reserved.
3	Ingress Header Parity Error Port 3	When set to ‘1’, at least one header parity error has been detected on the ingress port.
2	Ingress Header Parity Error Port 2	See the description for bit 3.
1	Ingress Header Parity Error Port 1	See the description for bit 3.
0	Ingress Header Parity Error Port 0	See the description for bit 3.

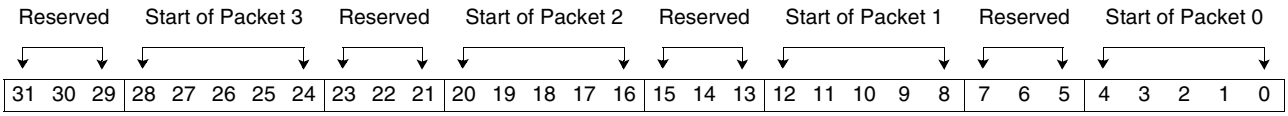
5.2.4 Egress Deskew Status Register

Start of Packet *N* field values are valid only when the four rx_data_indicator signals are active (set to '1'). The rx_data_indicator signals are set in the *DASL Status Register* (page 99), bits 3:0.

Address x'0D'

Access Type Read Only

Reset Value '0000 0000 0000 0000 0000 0000 0000 0000'



Bit(s)	Field Name	Description
31:29	Reserved	Reserved.
28:24	Start of Packet 3	Indicates the starting position of packet 3 (that is, the value of the egress deskew sequencer when the start of packet 3 is detected).
23:21	Reserved	Reserved.
20:16	Start of Packet 2	Indicates the starting position of packet 2 (that is, the value of the egress deskew sequencer when the start of packet 2 is detected).
15:13	Reserved	Reserved.
12:8	Start of Packet 1	Indicates the starting position of packet 1 (that is, the value of the egress deskew sequencer when the start of packet 1 is detected).
7:5	Reserved	Reserved.
4:0	Start of Packet 0	Indicates the starting position of packet 0 (that is, the value of the egress deskew sequencer when the start of packet 0 is detected).

5.2.5 Egress Deskew Command Register

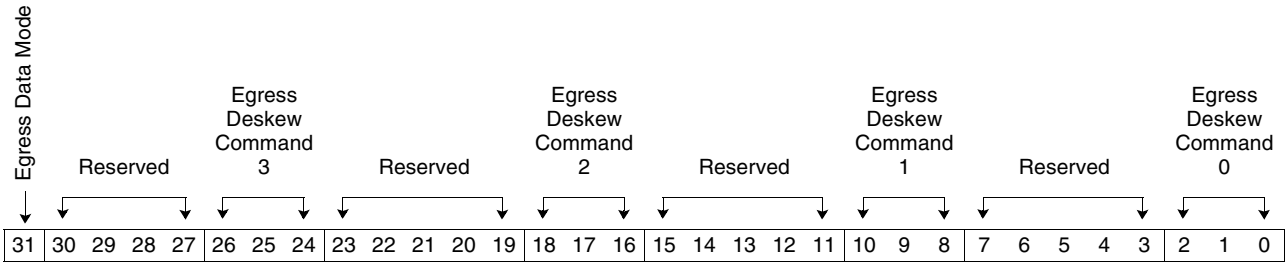
The local processor writes this register in two steps:

1. Writes the Egress Deskew Command *N* field values.
2. Sets the Egress Data Mode bit to ‘1’ (when the DASL ports deskew process is complete).

Address x‘0E’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



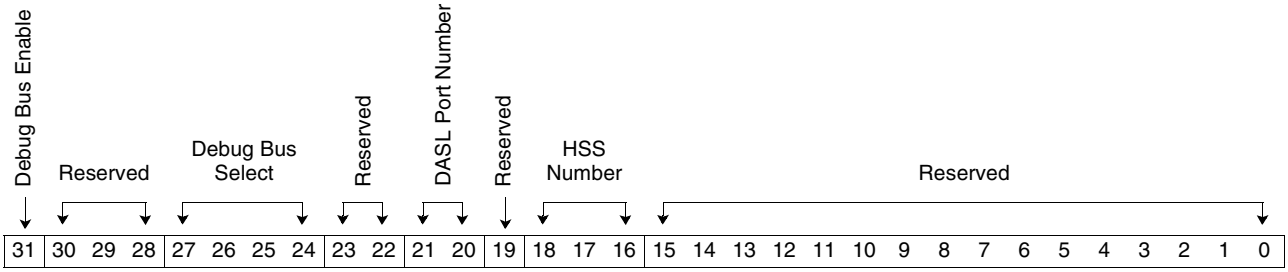
Bit(s)	Field Name	Description
31	Egress Data Mode	0 Egress DASL ports deskew process has not started or is incomplete. Data sent from the egress DASL ports deskew block to the PowerPRS C192 packet formatting block is invalid. 1 Egress DASL ports deskew is complete; data mode can begin.
30:27	Reserved	Reserved.
26:24	Egress Deskew Command 3	Controls the deskew multiplexer position: 000 0 cycles 100 4 cycles 001 1 cycle 101 5 cycles 010 2 cycles 110 6 cycles 011 3 cycles 111 7 cycles
23:19	Reserved	Reserved.
18:16	Egress Deskew Command 2	See the description for bits 26:24.
15:11	Reserved	Reserved.
10:8	Egress Deskew Command 1	See the description for bits 26:24.
7:3	Reserved	Reserved.
2:0	Egress Deskew Command 0	See the description for bits 26:24.

5.2.6 Debug Bus Select Register

Address x‘0F’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	Debug Bus Enable	When set to ‘1’, enables the debug bus drivers and the Osc625Probe_N/P driver.
30:28	Reserved	Reserved.
27:24	Debug Bus Select	Specifies the functional block or other device element for which the DebugBus[17:0] pins provide information: 0000 Reserved 0001 HSS receive logic 0010 Ingress routing block 0011 PowerPRS 64G packet formatting 0100 DASL receive ports 0101 DASL ports deskew 0110 PowerPRS C192 packet formatting 0111 DASL picoprocessor instruction address and companion clock 1000 DASL picoprocessor internal information 1001 Clocks and miscellaneous signals *Table 5-2* on page 70 presents the DebugBus[17:0] pin information for each bit setting.
23:22	Reserved	Reserved.
21:20	DASL Port Number	Specifies the DASL port number: 00 DASL port 0 01 DASL port 1 10 DASL port 2 11 DASL port 3 This field is valid only when the Debug Bus Select field is set to ‘0010’, ‘0011’, ‘0100’, ‘0101’, or ‘0110’.
19	Reserved	Reserved.
18:16	HSS Number	Specifies the HSS number: 000 HSS-0 001 HSS-1 010 HSS-2 011 HSS-3 100 HSS-4 101 HSS-5 110 HSS-6 111 HSS-7 This field is valid only when the Debug Bus Select field is set to ‘0001’.
15:0	Reserved	Reserved.

Table 5-2. DebugBus[17:0] Pin Information by Debug Bus Select Field Value

Debug Bus Select Field Value	DebugBus[17:0] Pin(s)	Signal Carried
'0001' (HSS Number field specifying one of eight HSSs)	**HSS Receive Logic**	
	DebugBusOut[17:16]	'00'
	DebugBusOut[15:8]	i_chan0_data
	DebugBusOut[7]	i_chan0_k_clock
	DebugBusOut[6]	i_data_valid
	DebugBusOut[5:4]	rx_synchro_status
	DebugBusOut[3]	rx_data_mode
	DebugBusOut[2]	rx_invalid_k
	DebugBusOut[1]	rx_synchro_lost
	DebugBusOut[0]	'0'
'0010' (DASL Port Number field specifying one of four ports)	**Ingress Routing Block**	
	DebugBusOut[17]	'0'
	DebugBusOut[16]	i_start_of_packet
	DebugBusOut[15:0]	i_packet_data[31:16]
'0011' (DASL Port Number field specifying one of four ports)	**PowerPRS 64G Packet Formatting**	
	DebugBusOut[17]	send_grant
	DebugBusOut[16]	tx_sop
	DebugBusOut[15:0]	tx_data_in[31:16]
'0100' (DASL Port Number field specifying one of four ports)	**DASL Receive Ports**	
	DebugBusOut[17]	'0'
	DebugBusOut[16]	rx_data_indicator
	DebugBusOut[15:0]	rx_data[31:16]
'0101' (DASL Port Number field specifying one of four ports)	**DASL Ports Deskew**	
	DebugBusOut[17]	e_data_valid
	DebugBusOut[16]	e_start_of_packet
	DebugBusOut[15:0]	e_dasl_data[31:16]
'0110' (DASL Port Number field specifying one of four ports)	**PowerPRS C192 Packet Formatting**	
	DebugBusOut[17]	'0'
	DebugBusOut[16]	e_k_pulse
	DebugBusOut[15:0]	e_packet_data[31:16]
'0111'	**DASL Picoprocessor Instruction Address and Companion Clock**	
	DebugBusOut[17:16]	'00'
	DebugBusOut[15:0]	m3_debug0
'1000'	**DASL Picoprocessor Internal Information**	
	DebugBusOut[17:16]	'00'
	DebugBusOut[15:0]	m3_debug1
'1001'	**Clocks and Miscellaneous Signals**	
	DebugBusOut[17:2]	'0000 0000 0000 0000'
	DebugBusOut[1]	bclk_ocm_dbg
	DebugBusOut[0]	synchronous_flush_b_rdv_dbg

5.3 HSS Programming Registers

5.3.1 HSS Receive Command Register

This register:

- Defines the main parameters of the high-speed SerDes (HSS) receive ports
- Enables the HSS receive macro
- Enables the HSS receive ports

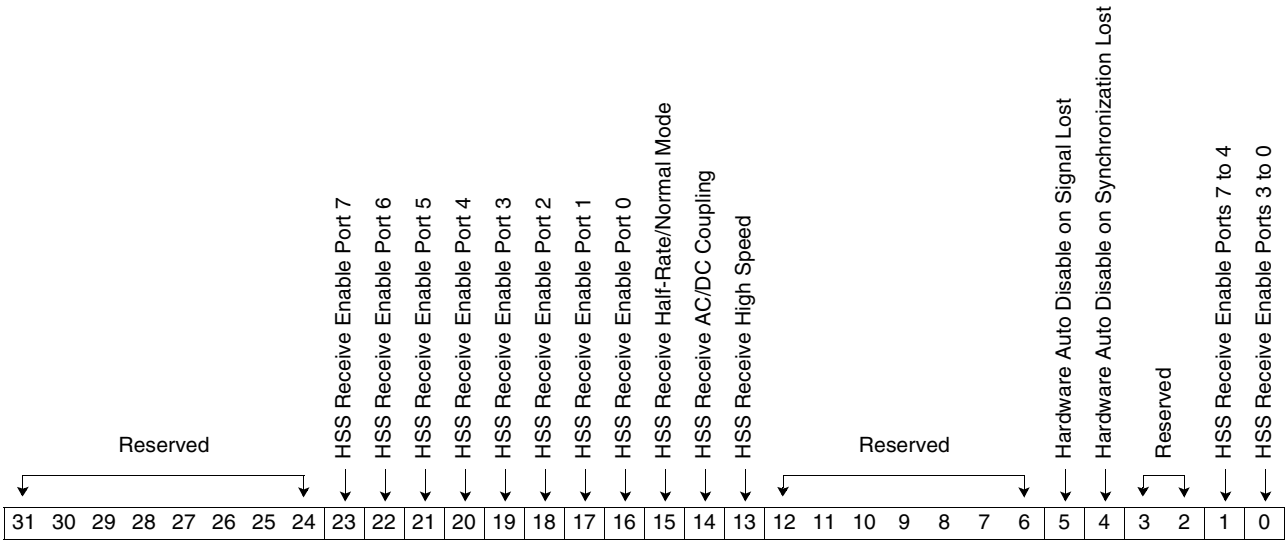
Write access to this register requires three steps:

1. Write the main parameters (bits 15:13 and 5:4).
2. Set bits 1:0 to '1' to enable the two HSS receive macros and then wait for the HSS receive PLLs to lock (bits 1:0 of the *HSS Error 1 Register* [page 85] set to '0').
3. Wait until all the HSS Receive Signal Lost Port *N* bits (15:8) in the *HSS Error 1 Register* are set to '0', then set bits 23:16 to '1' to enable the eight HSS receive ports.

Address x'10'

Access Type Read/Write

Reset Value '0000 0000 0000 0000 0000 0000 0000 0000'



Bit(s)	Field Name	Description
31:24	Reserved	Reserved.
23	HSS Receive Enable Port 7	1 Enables the HSS receive logic (synchronization and supervision) for the port. When this bit is asserted, the HSS receive synchronization process begins. 0 Disables the HSS receive logic, holding the port in a reset state. In this state, the port cannot receive packets.
22	HSS Receive Enable Port 6	See the description for bit 23.
21	HSS Receive Enable Port 5	See the description for bit 23.

Bit(s)	Field Name	Description
20	HSS Receive Enable Port 4	See the description for bit 23.
19	HSS Receive Enable Port 3	See the description for bit 23.
18	HSS Receive Enable Port 2	See the description for bit 23.
17	HSS Receive Enable Port 1	See the description for bit 23.
16	HSS Receive Enable Port 0	See the description for bit 23.
15	HSS Receive Half-Rate/Normal Mode	1 Specifies half-rate mode on all HSS receive ports. 0 Specifies the normal rate on all HSS receive ports. **Note:** Half-rate mode reduces the receive frequency by a factor of two on all HSS ports and should only be used during HSS testing.
14	HSS Receive AC/DC Coupling	1 Specifies dc coupling on all HSS receive ports. In this mode, the receiver sources current to and the driver sinks current from the transmission path. 0 Specifies ac coupling on all HSS receive ports. In this mode, the driver sources current to and sinks current from the transmission path.
13	HSS Receive High Speed	Enables the HSS receive PLL voltage-controlled oscillator (VCO) to operate at high speed. This bit must be set to ‘0’.
12:6	Reserved	Reserved.
5	Hardware Auto Disable on Signal Lost	When set to ‘1’, allows the hardware to automatically deassert the HSS receive logic i_data_valid signal when a signal is lost. This bit disables the DASL transmit ports (forces all DASL outputs to ‘0’) when the DASL Auto Disable Control bit in the *HSS FIR C0 Register* (page 91) is set to ‘0’. This bit must be set to ‘1’ in normal mode or PowerPRS C192 loopback mode and to ‘0’ in PowerPRS 64G (switch) loopback mode.
4	Hardware Auto Disable on Synchronization Lost	When set to ‘1’, allows the hardware to automatically deassert the HSS receive logic i_data_valid signal when synchronization is lost. This bit disables the DASL transmit ports (forces all DASL outputs to ‘0’) when the DASL Auto Disable Control bit in the *HSS FIR C0 Register* is set to ‘0’. This bit must be set to ‘1’ in normal mode or PowerPRS C192 loopback mode and to ‘0’ in PowerPRS 64G (switch) loopback mode.
3:2	Reserved	Reserved.
1	HSS Receive Enable Ports 7 to 4	1 Enables the HSS receive macro for ports 7 to 4. 0 Disables the HSS receive macro for ports 7 to 4, holding the ports in a reset state.
0	HSS Receive Enable Ports 3 to 0	1 Enables the HSS receive macro for ports 3 to 0. 0 Disables the HSS receive macro for ports 3 to 0, holding the ports in a reset state.

5.3.2 HSS Transmit Command Register

This register:

- Defines the main parameters of the HSS transmit ports
- Enables the HSS transmit macro
- Enables the HSS transmit ports

Write access to this register requires four steps:

1. Write the main parameters (bits 15:13).
2. Set bits 1:0 to ‘1’ to enable the two HSS transmit macros and then wait for the HSS transmit PLLs to lock (bits 3:2 of the *HSS Error 1 Register* [page 85] set to ‘0’)
3. Set bits 23:16 to ‘1’ to enable the eight HSS transmit ports.
4. Set bits 31:24 to ‘1’ to enable the HSS port drivers.

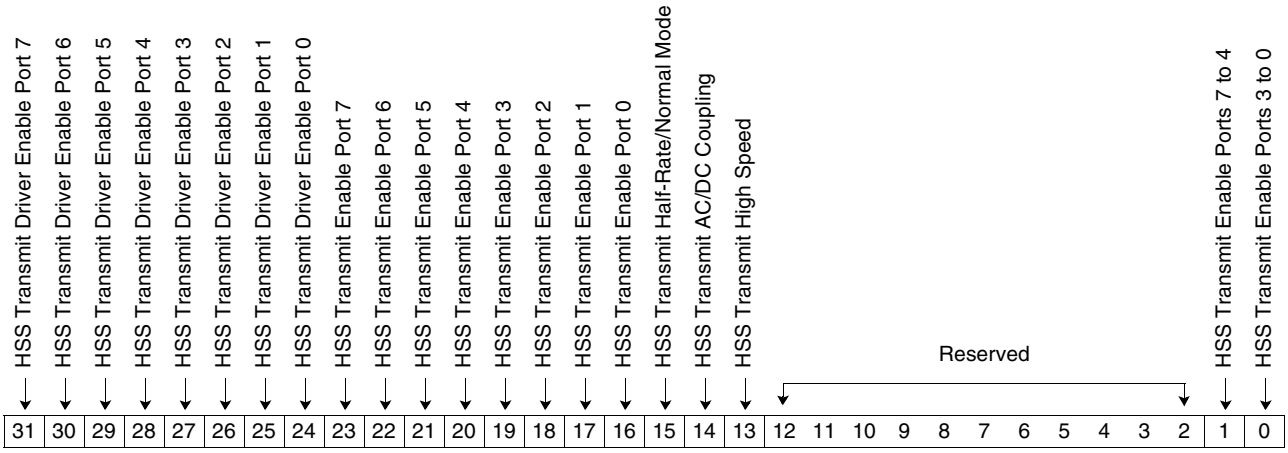
To enable an HSS port driver, three conditions must be met:

- The Off-Chip Driver Enable bit in the *Reset Register* (page 58) must be set to ‘1’.
- The FullyInsertedIn# signal must be active (low level).
- The corresponding HSS Transmit Driver Enable Port *N* bit must be set to ‘1’.

Address x‘11’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	HSS Transmit Driver Enable Port 7	1 Enables the HSS transmit port driver. 0 Disables the HSS transmit port driver, holding it in a high impedance state.
30	HSS Transmit Driver Enable Port 6	See the description for bit 31.
29	HSS Transmit Driver Enable Port 5	See the description for bit 31.
28	HSS Transmit Driver Enable Port 4	See the description for bit 31.

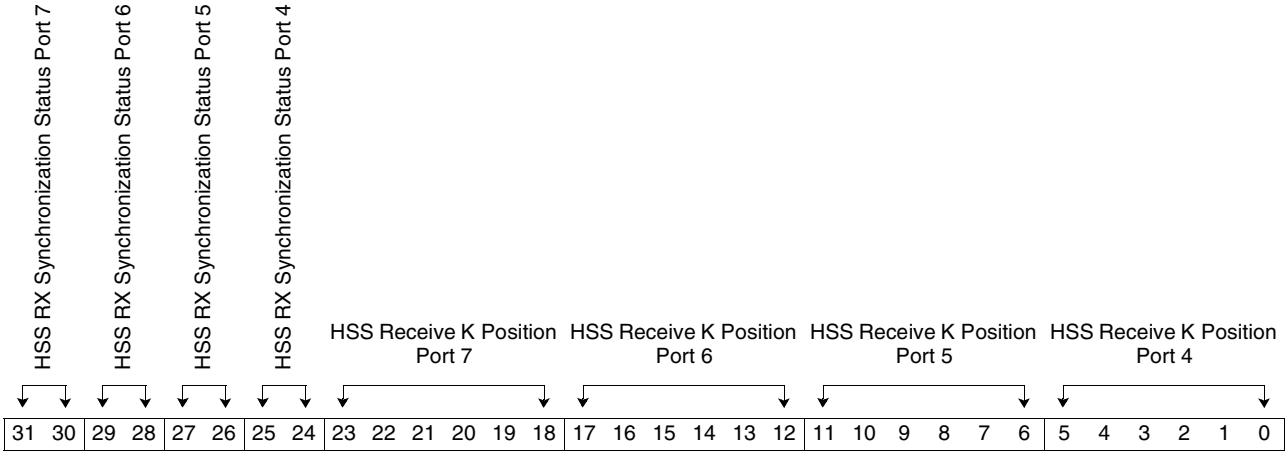
Bit(s)	Field Name	Description
27	HSS Transmit Driver Enable Port 3	See the description for bit 31.
26	HSS Transmit Driver Enable Port 2	See the description for bit 31.
25	HSS Transmit Driver Enable Port 1	See the description for bit 31.
24	HSS Transmit Driver Enable Port 0	See the description for bit 31.
23	HSS Transmit Enable Port 7	1 Enables the HSS transmit logic for the port so that normal data transmission can occur. 0 Disables the HSS transmit logic, holding the port in a reset state.
22	HSS Transmit Enable Port 6	See the description for bit 23.
21	HSS Transmit Enable Port 5	See the description for bit 23.
20	HSS Transmit Enable Port 4	See the description for bit 23.
19	HSS Transmit Enable Port 3	See the description for bit 23.
18	HSS Transmit Enable Port 2	See the description for bit 23.
17	HSS Transmit Enable Port 1	See the description for bit 23.
16	HSS Transmit Enable Port 0	See the description for bit 23.
15	HSS Transmit Half-Rate/Normal Mode	1 Specifies half-rate mode on all HSS transmit ports. 0 Specifies the normal rate on all HSS transmit ports. **Note:** Half-rate mode reduces the receive frequency by a factor of two on all HSS ports and should only be used during HSS testing.
14	HSS Transmit AC/DC Coupling	1 Specifies dc coupling on all HSS transmit ports. In this mode, the receiver sources current to and the driver sinks current from the transmission path. 0 Specifies ac coupling on all HSS transmit ports. In this mode, the driver sources current to and sinks current from the transmission path.
13	HSS Transmit High Speed	Enables the HSS transmit PLL VCO to operate at high speed. This bit must be set to ‘0’.
12:2	Reserved	Reserved.
1	HSS Transmit Enable Ports 7 to 4	1 Enables the HSS transmit macro for ports 7 to 4. 0 Disables the HSS transmit macro for ports 7 to 4, holding the ports in a reset state.
0	HSS Transmit Enable Ports 3 to 0	1 Enables the HSS transmit macro for ports 3 to 0. 0 Disables the HSS transmit macro for ports 3 to 0, holding the ports in a reset state.

5.3.3 HSS Synchronization Status 1 Register

Address x‘12’

Access Type Read Only

Reset Value ‘0000 0000 uuuu uuuu uuuu uuuu uuuu uuuu’, where ‘u’ = undefined



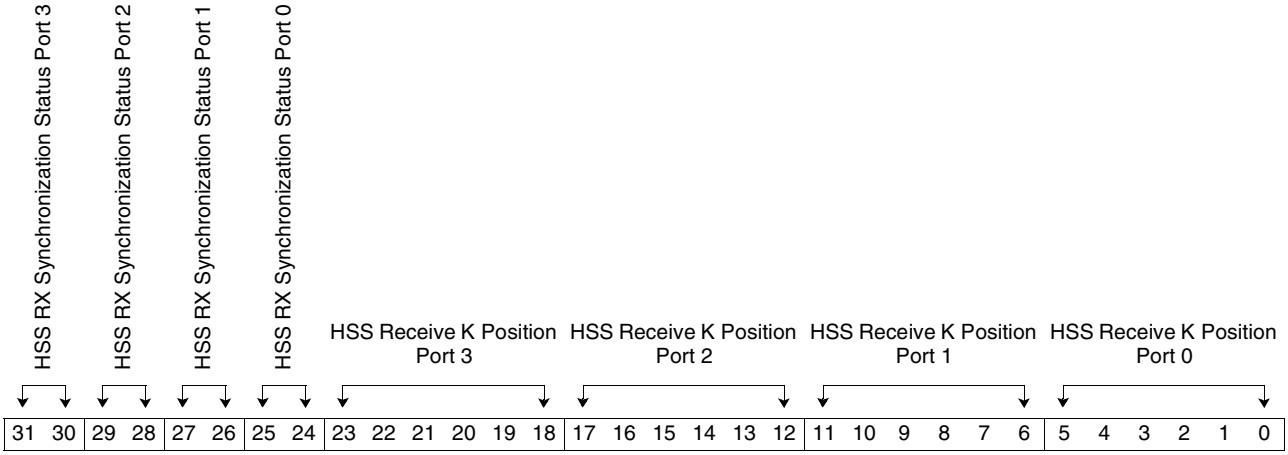
Bit(s)	Field Name	Description
31:30	HSS RX Synchro-nization Status Port 7	Indicates the status of the port synchronization process: 00 HSS receive logic is either disabled or byte synchronization is incomplete. 01 Byte synchronization is complete. 10 LU alignment is complete. 11 The K28.5 position is valid and written in the corresponding HSS Receive K Position Port field.
29:28	HSS RX Synchro-nization Status Port 6	See the description for bits 31:30.
27:26	HSS RX Synchro-nization Status Port 5	See the description for bits 31:30.
25:24	HSS RX Synchro-nization Status Port 4	See the description for bits 31:30.
23:18	HSS Receive K Position Port 7	Indicates the HSS receive port K28.5 position.
17:12	HSS Receive K Position Port 6	See the description for bits 23:18.
11:6	HSS Receive K Position Port 5	See the description for bits 23:18.
5:0	HSS Receive K Position Port 4	See the description for bits 23:18.

5.3.4 HSS Synchronization Status 2 Register

Address x‘13’

Access Type Read Only

Reset Value ‘0000 0000 uuuu uuuu uuuu uuuu uuuu uuuu’, where ‘u’ = undefined



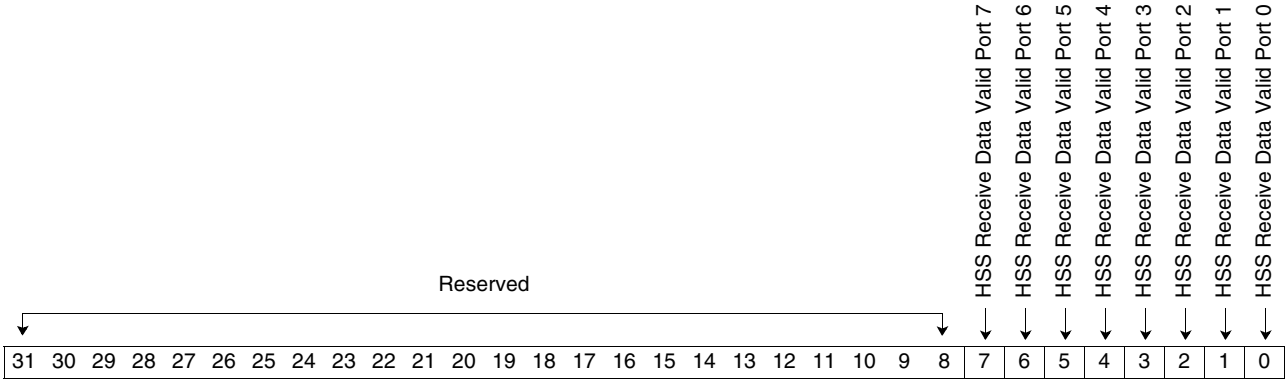
Bit(s)	Field Name	Description
31:30	HSS RX Synchro-nization Status Port 3	Indicates the status of the port synchronization process: 00 HSS receive logic is either disabled or byte synchronization is incomplete. 01 Byte synchronization is complete. 10 LU alignment is complete. 11 The K28.5 position is valid and written in the corresponding HSS Receive K Position Port field.
29:28	HSS RX Synchro-nization Status Port 2	See the description for bits 31:30.
27:26	HSS RX Synchro-nization Status Port 1	See the description for bits 31:30.
25:24	HSS RX Synchro-nization Status Port 0	See the description for bits 31:30.
23:18	HSS Receive K Position Port 3	Indicates the HSS receive port K28.5 position.
17:12	HSS Receive K Position Port 2	See the description for bits 23:18.
11:6	HSS Receive K Position Port 1	See the description for bits 23:18.
5:0	HSS Receive K Position Port 0	See the description for bits 23:18.

5.3.5 HSS Synchronization Status 3 Register

Address x‘14’

Access Type Read Only

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:8	Reserved	Reserved.
7	HSS Receive Data Valid Port 7	Indicates the status of the HSS receive port i_data_valid signal: 0 The data is invalid. 1 The data is valid.
6	HSS Receive Data Valid Port 6	See the description for bit 7.
5	HSS Receive Data Valid Port 5	See the description for bit 7.
4	HSS Receive Data Valid Port 4	See the description for bit 7.
3	HSS Receive Data Valid Port 3	See the description for bit 7.
2	HSS Receive Data Valid Port 2	See the description for bit 7.
1	HSS Receive Data Valid Port 1	See the description for bit 7.
0	HSS Receive Data Valid Port 0	See the description for bit 7.

5.3.6 HSS Ingress Deskew Command Register

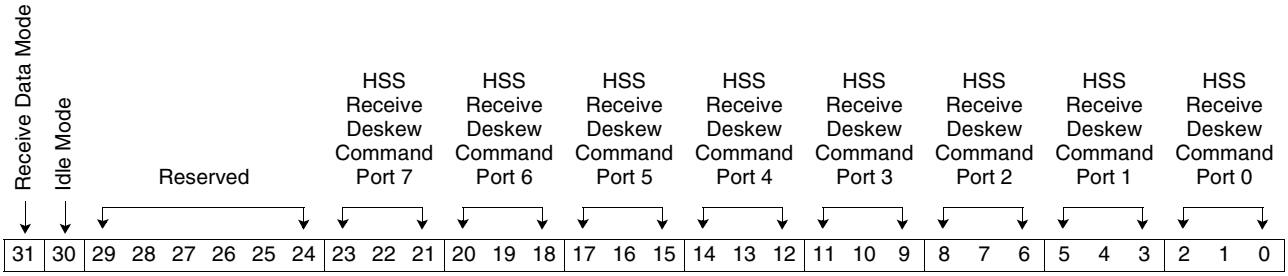
The local processor writes this register in three steps:

1. Writes the HSS Receive Deskew Command Port *N* fields (bits 23:0).
2. Sets the Receive Data Mode bit to ‘1’ when the LU deskew process is complete.
3. Sets the Idle Mode bit to ‘1’ when synchronization is complete in the PowerPRS 64G DASL receive ports.

Address x‘15’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	Receive Data Mode	Set to ‘1’ when the HSS receive logic LU deskew process is complete. Hardware completes the receive synchronization process and then starts link supervision and packet reception on all HSS ports by asserting the i_data_valid signal.
30	Idle Mode	0 The ingress logic transforms HSS idle packets into DASL synchronization packets. 1 The ingress logic transforms HSS idle packets into DASL idle packets. **Note:** This bit must be set to ‘0’ during the synchronization process and to ‘1’ for normal data transmission.
29:24	Reserved	Reserved.
23:21	HSS Receive Deskew Command Port 7	Specifies the number of delay cycles applied to the LUs on the HSS receive port: 000 0 cycles 100 4 cycles 001 1 cycle 101 5 cycles 010 2 cycles 110 6 cycles 011 3 cycles 111 7 cycles
20:18	HSS Receive Deskew Command Port 6	See the description for bits 23:21.
17:15	HSS Receive Deskew Command Port 5	See the description for bits 23:21.
14:12	HSS Receive Deskew Command Port 4	See the description for bits 23:21.
11:9	HSS Receive Deskew Command Port 3	See the description for bits 23:21.
8:6	HSS Receive Deskew Command Port 2	See the description for bits 23:21.

Bit(s)	Field Name	Description
5:3	HSS Receive Deskew Command Port 1	See the description for bits 23:21.
2:0	HSS Receive Deskew Command Port 0	See the description for bits 23:21.

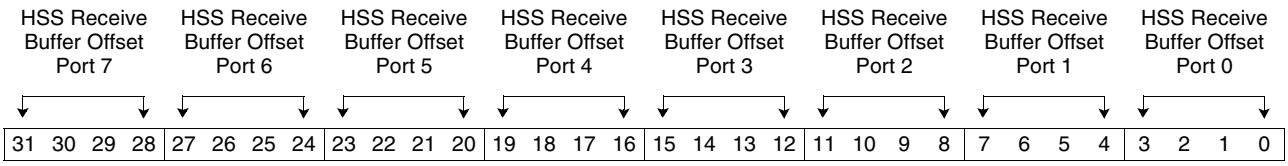
5.3.7 HSS Receive Buffer Offset Register

This register must be written before setting the HSS Receive Enable Port *N* fields in the *HSS Receive Command Register* (page 71).

Address x‘16’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:28	HSS Receive Buffer Offset Port 7	This field corresponds to the preset value of the read address counter used by the HSS receive clock deskew multiport register arrays (MPRAs). Valid field values range from x‘4’ to x‘C’; the recommended value is x‘8’.
27:24	HSS Receive Buffer Offset Port 6	See the description for bits 31:28.
23:20	HSS Receive Buffer Offset Port 5	See the description for bits 31:28.
19:16	HSS Receive Buffer Offset Port 4	See the description for bits 31:28.
15:12	HSS Receive Buffer Offset Port 3	See the description for bits 31:28.
11:8	HSS Receive Buffer Offset Port 2	See the description for bits 31:28.
7:4	HSS Receive Buffer Offset Port 1	See the description for bits 31:28.
3:0	HSS Receive Buffer Offset Port 0	See the description for bits 31:28.

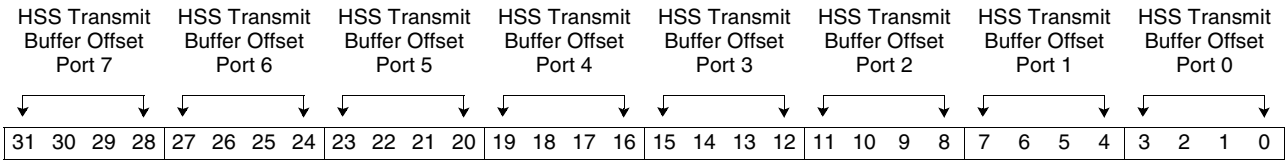
5.3.8 HSS Transmit Buffer Offset Register

This register must be written before setting the HSS Transmit Enable Port *N* fields in the *HSS Transmit Command Register* (page 73).

Address x‘17’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



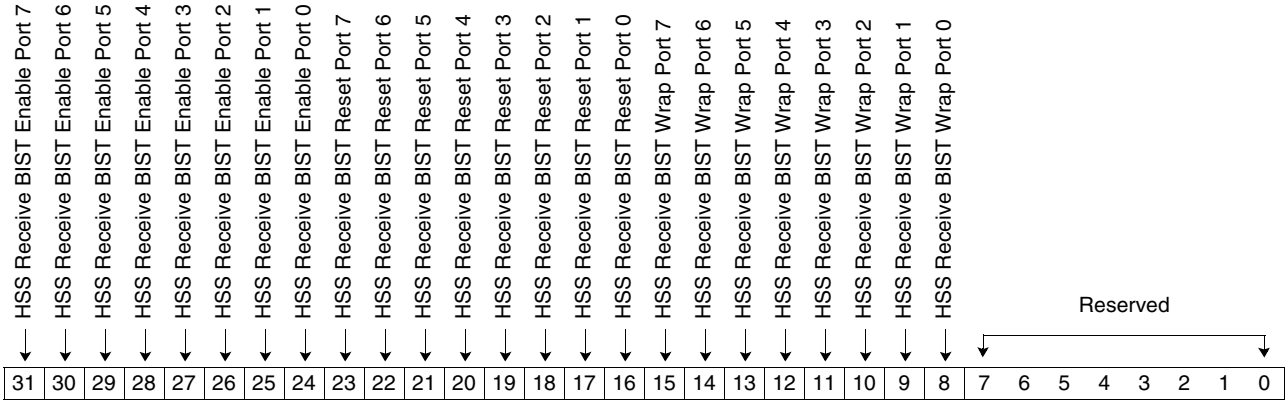
Bit(s)	Field Name	Description
31:28	HSS Transmit Buffer Offset Port 7	This field corresponds to the preset value of the write address counter used by the HSS transmit clock deskew MPRAs. Valid field values range from x‘4’ to x‘C’; the recommended value is x‘8’.
27:24	HSS Transmit Buffer Offset Port 6	See the description for bits 31:28.
23:20	HSS Transmit Buffer Offset Port 5	See the description for bits 31:28.
19:16	HSS Transmit Buffer Offset Port 4	See the description for bits 31:28.
15:12	HSS Transmit Buffer Offset Port 3	See the description for bits 31:28.
11:8	HSS Transmit Buffer Offset Port 2	See the description for bits 31:28.
7:4	HSS Transmit Buffer Offset Port 1	See the description for bits 31:28.
3:0	HSS Transmit Buffer Offset Port 0	See the description for bits 31:28.

5.3.9 HSS Receive BIST Command Register

Address x‘18’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	HSS Receive BIST Enable Port 7	When set to ‘1’, enables a logic BIST on the HSS receive port.
30	HSS Receive BIST Enable Port 6	See the description for bit 31.
29	HSS Receive BIST Enable Port 5	See the description for bit 31.
28	HSS Receive BIST Enable Port 4	See the description for bit 31.
27	HSS Receive BIST Enable Port 3	See the description for bit 31.
26	HSS Receive BIST Enable Port 2	See the description for bit 31.
25	HSS Receive BIST Enable Port 1	See the description for bit 31.
24	HSS Receive BIST Enable Port 0	See the description for bit 31.
23	HSS Receive BIST Reset Port 7	When set to ‘1’, resets the logic BIST controller on the HSS receive port.
22	HSS Receive BIST Reset Port 6	See the description for bit 23.
21	HSS Receive BIST Reset Port 5	See the description for bit 23.
20	HSS Receive BIST Reset Port 4	See the description for bit 23.
19	HSS Receive BIST Reset Port 3	See the description for bit 23.
18	HSS Receive BIST Reset Port 2	See the description for bit 23.

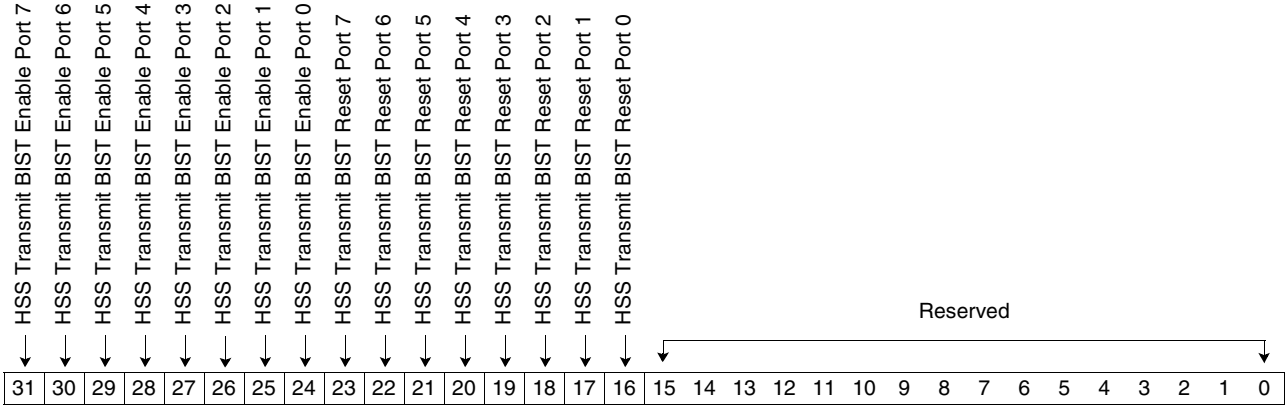
Bit(s)	Field Name	Description
17	HSS Receive BIST Reset Port 1	See the description for bit 23.
16	HSS Receive BIST Reset Port 0	See the description for bit 23.
15	HSS Receive BIST Wrap Port 7	Selects the HSS receive port data source during a logic BIST: 1 The logic BIST data source is internally generated. 0 The logic BIST data source is externally received.
14	HSS Receive BIST Wrap Port 6	See the description for bit 15.
13	HSS Receive BIST Wrap Port 5	See the description for bit 15.
12	HSS Receive BIST Wrap Port 4	See the description for bit 15.
11	HSS Receive BIST Wrap Port 3	See the description for bit 15.
10	HSS Receive BIST Wrap Port 2	See the description for bit 15.
9	HSS Receive BIST Wrap Port 1	See the description for bit 15.
8	HSS Receive BIST Wrap Port 0	See the description for bit 15.
7:0	Reserved	Reserved.

5.3.10 HSS Transmit BIST Command Register

Address x‘19’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	HSS Transmit BIST Enable Port 7	When set to ‘1’, enables a logic BIST on the HSS transmit port.
30	HSS Transmit BIST Enable Port 6	See the description for bit 31.
29	HSS Transmit BIST Enable Port 5	See the description for bit 31.
28	HSS Transmit BIST Enable Port 4	See the description for bit 31.
27	HSS Transmit BIST Enable Port 3	See the description for bit 31.
26	HSS Transmit BIST Enable Port 2	See the description for bit 31.
25	HSS Transmit BIST Enable Port 1	See the description for bit 31.
24	HSS Transmit BIST Enable Port 0	See the description for bit 31.
23	HSS Transmit BIST Reset Port 7	When set to ‘1’, resets the logic BIST controller on the HSS transmit port.
22	HSS Transmit BIST Reset Port 6	See the description for bit 23.
21	HSS Transmit BIST Reset Port 5	See the description for bit 23.
20	HSS Transmit BIST Reset Port 4	See the description for bit 23.
19	HSS Transmit BIST Reset Port 3	See the description for bit 23.
18	HSS Transmit BIST Reset Port 2	See the description for bit 23.

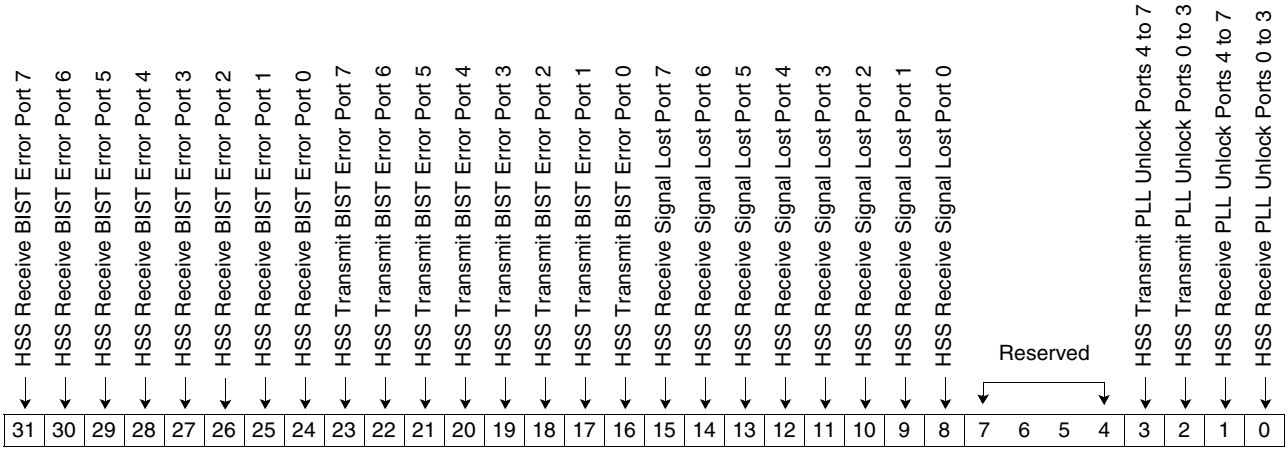
Bit(s)	Field Name	Description
17	HSS Transmit BIST Reset Port 1	See the description for bit 23.
16	HSS Transmit BIST Reset Port 0	See the description for bit 23.
15:0	Reserved	Reserved.

5.3.11 HSS Error 1 Register

Address x‘1A’

Access Type Read only

Reset Value Undefined



Bit(s)	Field Name	Description
31	HSS Receive BIST Error Port 7	When set to ‘1’, reports a logic BIST failure on the HSS receive port. This bit is reset when the corresponding HSS Receive BIST Reset Port bit is set to ‘1’ in the *HSS Receive BIST Command Register* (page 81).
30	HSS Receive BIST Error Port 6	See the description for bit 31.
29	HSS Receive BIST Error Port 5	See the description for bit 31.
28	HSS Receive BIST Error Port 4	See the description for bit 31.
27	HSS Receive BIST Error Port 3	See the description for bit 31.
26	HSS Receive BIST Error Port 2	See the description for bit 31.
25	HSS Receive BIST Error Port 1	See the description for bit 31.
24	HSS Receive BIST Error Port 0	See the description for bit 31.
23	HSS Transmit BIST Error Port 7	When set to ‘1’, reports a logic BIST failure on the HSS transmit port. This bit is reset when the corresponding HSS Transmit BIST Reset Port bit is set to ‘1’ in the *HSS Transmit BIST Command Register* (page 83).
22	HSS Transmit BIST Error Port 6	See the description for bit 23.
21	HSS Transmit BIST Error Port 5	See the description for bit 23.
20	HSS Transmit BIST Error Port 4	See the description for bit 23.

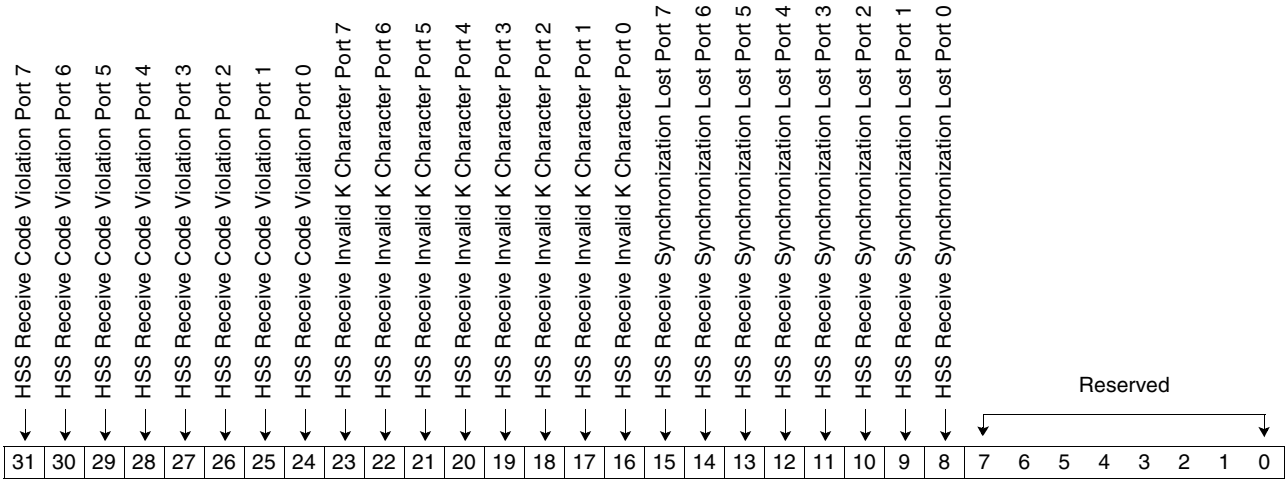
Bit(s)	Field Name	Description
19	HSS Transmit BIST Error Port 3	See the description for bit 23.
18	HSS Transmit BIST Error Port 2	See the description for bit 23.
17	HSS Transmit BIST Error Port 1	See the description for bit 23.
16	HSS Transmit BIST Error Port 0	See the description for bit 23.
15	HSS Receive Signal Lost Port 7	0 The HSS receiver detects the correct signal on the corresponding port. 1 The HSS receiver does not detect a signal. If the Hardware Auto Disable on Signal Lost bit in the *HSS Receive Command Register* (page 71) is set to '1', the corresponding HSS Receive Data Valid Port bit in the *HSS Synchronization Status 3 Register* (page 77) is automatically cleared and the port disabled.
14	HSS Receive Signal Lost Port 6	See the description for bit 15.
13	HSS Receive Signal Lost Port 5	See the description for bit 15.
12	HSS Receive Signal Lost Port 4	See the description for bit 15.
11	HSS Receive Signal Lost Port 3	See the description for bit 15.
10	HSS Receive Signal Lost Port 2	See the description for bit 15.
9	HSS Receive Signal Lost Port 1	See the description for bit 15.
8	HSS Receive Signal Lost Port 0	See the description for bit 15.
7:4	Reserved	Reserved.
3	HSS Transmit PLL Unlock Ports 4 to 7	When set to '1', unlocks the HSS transmit PLL for the indicated ports.
2	HSS Transmit PLL Unlock Ports 0 to 3	See the description for bit 3.
1	HSS Receive PLL Unlock Ports 4 to 7	When set to '1', unlocks the HSS receive PLL for the indicated ports.
0	HSS Receive PLL Unlock Ports 0 to 3	See the description for bit 1.

5.3.12 HSS Error 2 Register

Address x‘1B’

Access Type Read/Clear

Reset Value Undefined



Bit(s)	Field Name	Description
31	HSS Receive Code Violation Port 7	When set to ‘1’, the HSS supervision logic has detected an 8b/10b code violation during the receive port data mode.
30	HSS Receive Code Violation Port 6	See the description for bit 31.
29	HSS Receive Code Violation Port 5	See the description for bit 31.
28	HSS Receive Code Violation Port 4	See the description for bit 31.
27	HSS Receive Code Violation Port 3	See the description for bit 31.
26	HSS Receive Code Violation Port 2	See the description for bit 31.
25	HSS Receive Code Violation Port 1	See the description for bit 31.
24	HSS Receive Code Violation Port 0	See the description for bit 31.
23	HSS Receive Invalid K Character Port 7	When set to ‘1’, the HSS supervision logic has detected at least one invalid K character (either an unaligned K28.5 character or a K28.1/K28.5 character in the wrong position) during the receive port data mode.
22	HSS Receive Invalid K Character Port 6	See the description for bit 23.
21	HSS Receive Invalid K Character Port 5	See the description for bit 23.
20	HSS Receive Invalid K Character Port 4	See the description for bit 23.

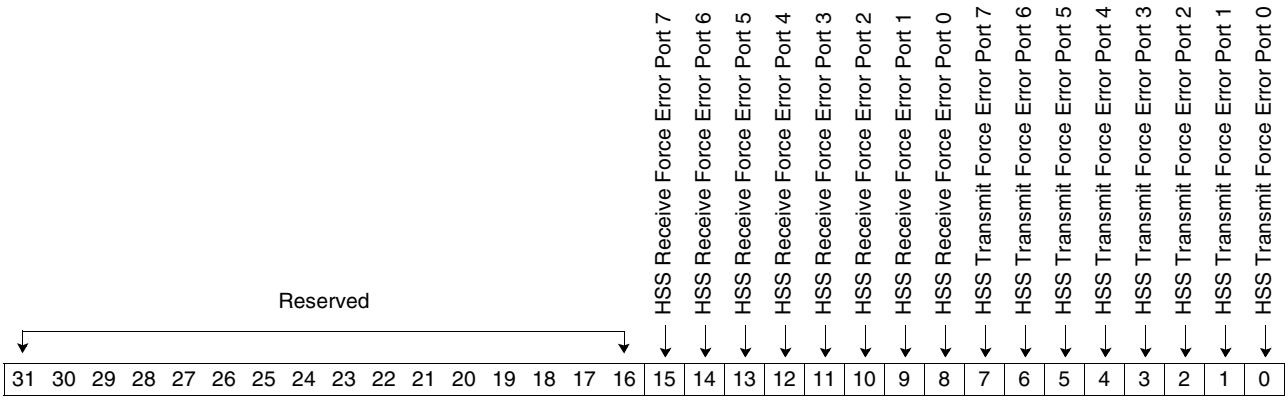
Bit(s)	Field Name	Description
19	HSS Receive Invalid K Character Port 3	See the description for bit 23.
18	HSS Receive Invalid K Character Port 2	See the description for bit 23.
17	HSS Receive Invalid K Character Port 1	See the description for bit 23.
16	HSS Receive Invalid K Character Port 0	See the description for bit 23.
15	HSS Receive Synchronization Lost Port 7	When set to ‘1’, the HSS supervision logic has detected a loss of synchronization condition (either three consecutive unaligned K28.5 characters or three consecutive K28.1/K28.5 characters in the wrong position) during the receive port data mode. If the Hardware Auto Disable on Synchronization Lost bit in the *HSS Receive Command Register* (page 71) is set to ‘1’, the corresponding HSS Receive Data Valid Port bit in the *HSS Synchronization Status 3 Register* (page 77) is automatically cleared and the port disabled.
14	HSS Receive Synchronization Lost Port 6	See the description for bit 15.
13	HSS Receive Synchronization Lost Port 5	See the description for bit 15.
12	HSS Receive Synchronization Lost Port 4	See the description for bit 15.
11	HSS Receive Synchronization Lost Port 3	See the description for bit 15.
10	HSS Receive Synchronization Lost Port 2	See the description for bit 15.
9	HSS Receive Synchronization Lost Port 1	See the description for bit 15.
8	HSS Receive Synchronization Lost Port 0	See the description for bit 15.
7:0	Reserved	Reserved.

5.3.13 HSS Force Error Register

Address x‘1C’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:16	Reserved	Reserved.
15	HSS Receive Force Error Port 7	When rising, forces an error in the HSS receive MPRA read address, which causes a code violation and loss of synchronization on the port.
14	HSS Receive Force Error Port 6	See the description for bit 15.
13	HSS Receive Force Error Port 5	See the description for bit 15.
12	HSS Receive Force Error Port 4	See the description for bit 15.
11	HSS Receive Force Error Port 3	See the description for bit 15.
10	HSS Receive Force Error Port 2	See the description for bit 15.
9	HSS Receive Force Error Port 1	See the description for bit 15.
8	HSS Receive Force Error Port 0	See the description for bit 15.
7	HSS Transmit Force Error Port 7	When rising, forces an error in the HSS transmit MPRA read address, which causes a code violation and loss of synchronization on the HSS port of the receiving device.
6	HSS Transmit Force Error Port 6	See the description for bit 7.
5	HSS Transmit Force Error Port 5	See the description for bit 7.
4	HSS Transmit Force Error Port 4	See the description for bit 7.
3	HSS Transmit Force Error Port 3	See the description for bit 7.

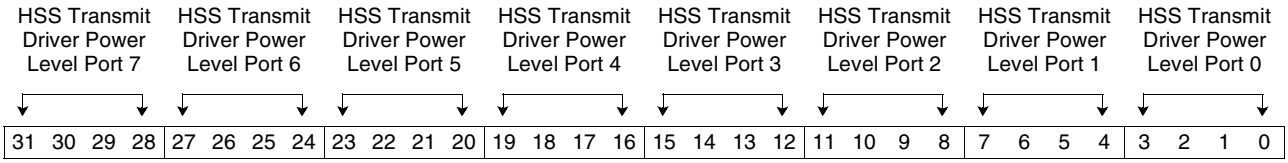
Bit(s)	Field Name	Description
2	HSS Transmit Force Error Port 2	See the description for bit 7.
1	HSS Transmit Force Error Port 1	See the description for bit 7.
0	HSS Transmit Force Error Port 0	See the description for bit 7.

5.3.14 HSS Power Level Register

Address x‘1D’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



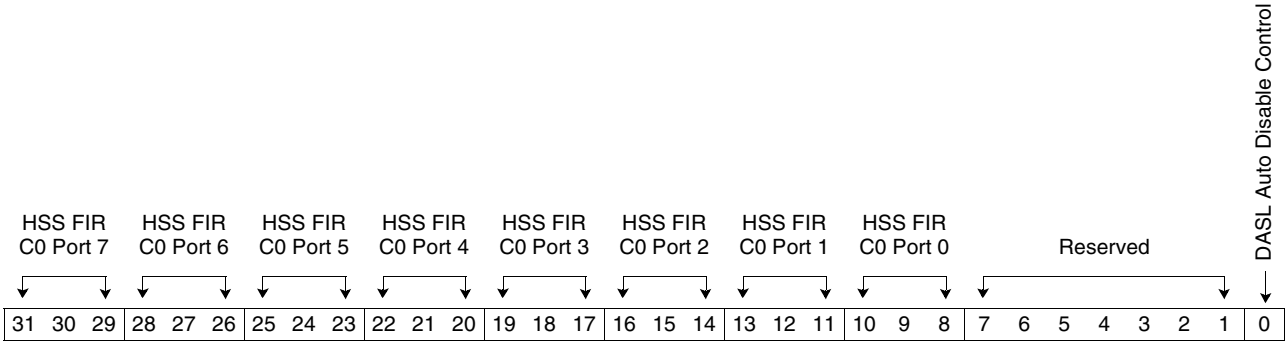
Bit(s)	Field Name	Description
31:28	HSS Transmit Driver Power Level Port 7	Adjusts the HSS transmit core driver output power.
27:24	HSS Transmit Driver Power Level Port 6	See the description for bits 31:28.
23:20	HSS Transmit Driver Power Level Port 5	See the description for bits 31:28.
19:16	HSS Transmit Drive Power Level Port 4	See the description for bits 31:28.
15:12	HSS Transmit Driver Power Level Port 3	See the description for bits 31:28.
11: 8	HSS Transmit Driver Power Level Port 2	See the description for bits 31:28.
7:4	HSS Transmit Drive Power Level Port 1	See the description for bits 31:28.
3:0	HSS Transmit Driver Power Level Port 0	See the description for bits 31:28.

5.3.15 HSS FIR C0 Register

Address x‘1E’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



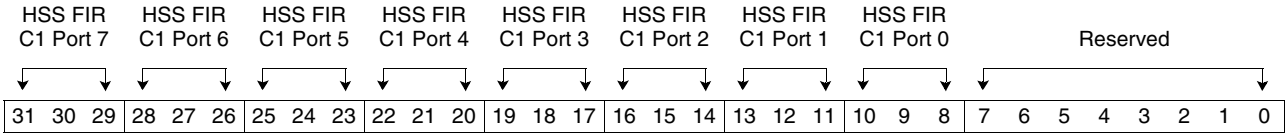
Bit(s)	Field Name	Description
31:29	HSS FIR C0 Port 7	Specifies the value of the pre-emphasis finite impulse response (FIR) filter coefficient, C0.
28:26	HSS FIR C0 Port 6	See the description for bits 31:29.
25:23	HSS FIR C0 Port 5	See the description for bits 31:29.
22:20	HSS FIR C0 Port 4	See the description for bits 31:29.
19:17	HSS FIR C0 Port 3	See the description for bits 31:29.
16:14	HSS FIR C0 Port 2	See the description for bits 31:29.
13:11	HSS FIR C0 Port 1	See the description for bits 31:29.
10:8	HSS FIR C0 Port 0	See the description for bits 31:29.
7:1	Reserved	Reserved.
0	DASL Auto Disable Control	0 Allows the DASL transmit macro to disable itself (by forcing its outputs to ‘0’) when the i_data_valid signal is at ‘0’. 1 Does not allow the DASL transmit macro to disable itself when the i_data_valid signal is at ‘0’. This bit must be set to ‘0’.

5.3.16 HSS FIR C1 Register

Address x‘1F’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



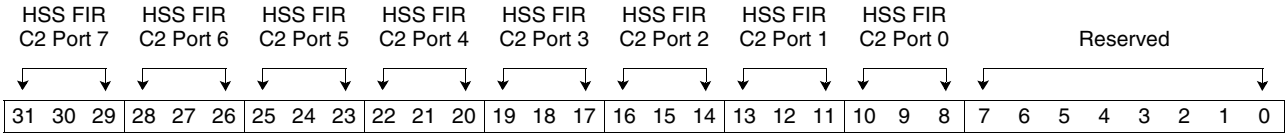
Bit(s)	Field Name	Description
31:29	HSS FIR C1 Port 7	Specifies the value of the pre-emphasis FIR filter coefficient, C1.
28:26	HSS FIR C1 Port 6	See the description for bits 31:29.
25:23	HSS FIR C1 Port 5	See the description for bits 31:29.
22:20	HSS FIR C1 Port 4	See the description for bits 31:29.
19:17	HSS FIR C1 Port 3	See the description for bits 31:29.
16:14	HSS FIR C1 Port 2	See the description for bits 31:29.
13:11	HSS FIR C1 Port 1	See the description for bits 31:29.
10:8	HSS FIR C1 Port 0	See the description for bits 31:29.
7:0	Reserved	Reserved.

5.3.17 HSS FIR C2 Register

Address x‘20’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



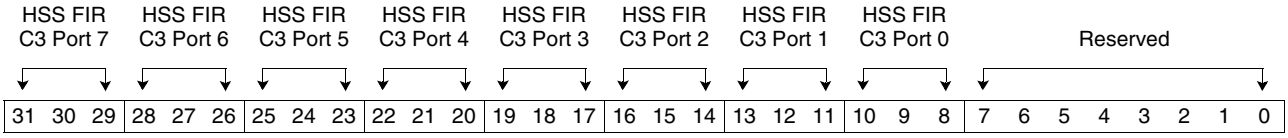
Bit(s)	Field Name	Description
31:29	HSS FIR C2 Port 7	Specifies the value of the pre-emphasis FIR filter coefficient, C2.
28:26	HSS FIR C2 Port 6	See the description for bits 31:29.
25:23	HSS FIR C2 Port 5	See the description for bits 31:29.
22:20	HSS FIR C2 Port 4	See the description for bits 31:29.
19:17	HSS FIR C2 Port 3	See the description for bits 31:29.
16:14	HSS FIR C2 Port 2	See the description for bits 31:29.
13:11	HSS FIR C2 Port 1	See the description for bits 31:29.
10:8	HSS FIR C2 Port 0	See the description for bits 31:29.
7:0	Reserved	Reserved.

5.3.18 HSS FIR C3 Register

Address x‘21’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:29	HSS FIR C3 Port 7	Specifies the value of the pre-emphasis FIR filter coefficient, C3.
28:26	HSS FIR C3 Port 6	See the description for bits 31:29.
25:23	HSS FIR C3 Port 5	See the description for bits 31:29.
22:20	HSS FIR C3 Port 4	See the description for bits 31:29.
19:17	HSS FIR C3 Port 3	See the description for bits 31:29.
16:14	HSS FIR C3 Port 2	See the description for bits 31:29.
13:11	HSS FIR C3 Port 1	See the description for bits 31:29.
10:8	HSS FIR C3 Port 0	See the description for bits 31:29.
7:0	Reserved	Reserved.

5.3.19 HSS Phase Rotator/Sample Registers

The PowerPRS SCIC implements the register shown below for each of the eight HSS ports at the respective address, x‘22’ to x‘29’.

Address

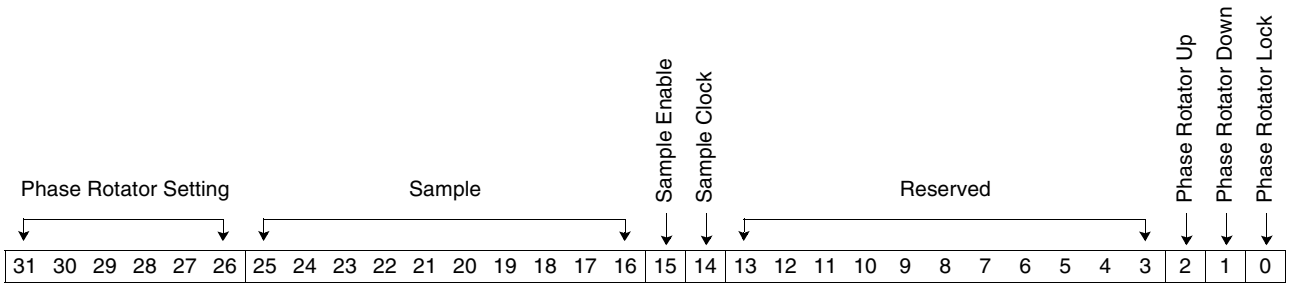
x‘22’	Port 0	x‘26’	Port 4
x‘23’	Port 1	x‘27’	Port 5
x‘24’	Port 2	x‘28’	Port 6
x‘25’	Port 3	x‘29’	Port 7

Access Type

Read Only for bits 31:16
Read/Write for bits 15:0

Reset Value

‘uuuu uuuu uuuu uuuu 0000 0000 0000 0000’, where ‘u’ = undefined



Bit(s)	Field Name	Description
31:26	Phase Rotator Setting	Indicates the current phase rotator setting on the HSS port.
25:16	Sample	Indicates the value of an instantaneous sample on the HSS port.
15	Sample Enable	When set to ‘1’, enables the observation latch on the HSS port.
14	Sample Clock	When rising, observation latch clock. If the Sample Enable bit is already set to ‘1’, latches a new sample in bits 25:16.
13:3	Reserved	Reserved.
2	Phase Rotator Up	When set to ‘1’, advances the HSS port sample clock phase by one step.
1	Phase Rotator Down	When set to ‘1’, retards the HSS port sample clock phase by one step.
0	Phase Rotator Lock	When set to ‘1’, allows external control of the Phase Rotator Setting field by manipulating bits 2:1.

5.4 DASL Programming Registers

These registers provide data-aligned synchronous link (DASL) logic access and control. DASL logic is comprised of four DASL receivers, four DASL transmitters, and one shared DASL controller (SDC). The SDC is comprised of:

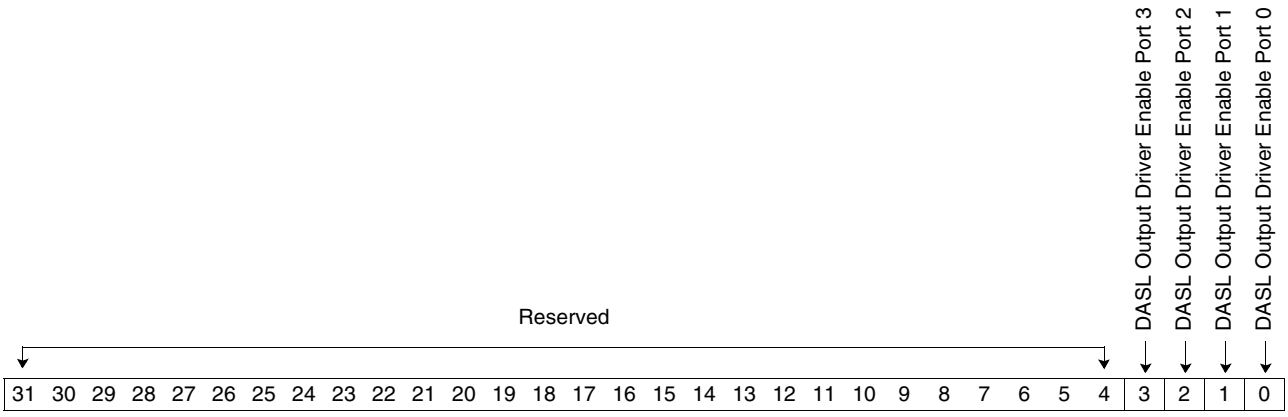
- A picoprocessor with instruction memory and local memory
- A set of I/O registers and hardware for DASL receiver control assistance

5.4.1 DASL Output Driver Enable Register

Address x‘30’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



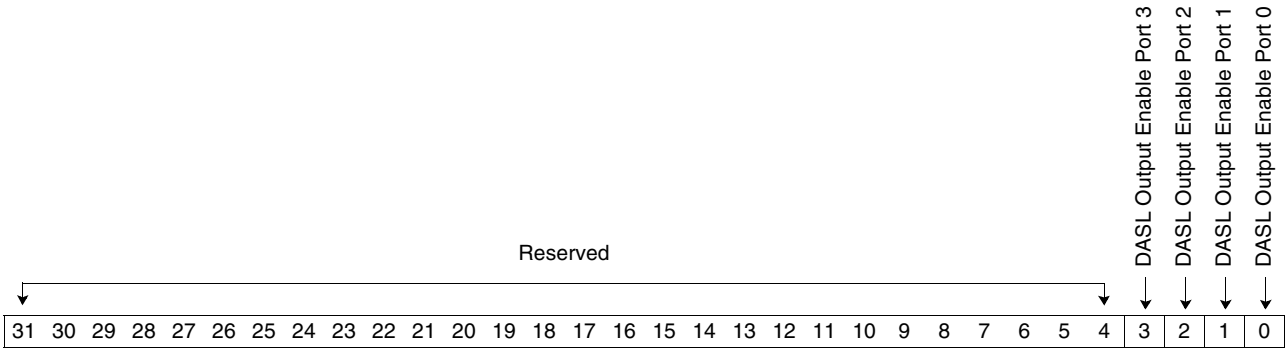
Bit(s)	Field Name	Description
31:4	Reserved	Reserved.
3	DASL Output Driver Enable Port 3	1 Enables the DASL output driver for the port when the Off-Chip Driver Enable bit is set in the *Reset Register* (page 58) and the FullyInsertedIn# signal is active (low level). 0 Disables (tristates) the DASL output driver.
2	DASL Output Driver Enable Port 2	See the description for bit 3.
1	DASL Output Driver Enable Port 1	See the description for bit 3.
0	DASL Output Driver Enable Port 0	See the description for bit 3.

5.4.2 Output Port Enable Register

Address x‘31’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



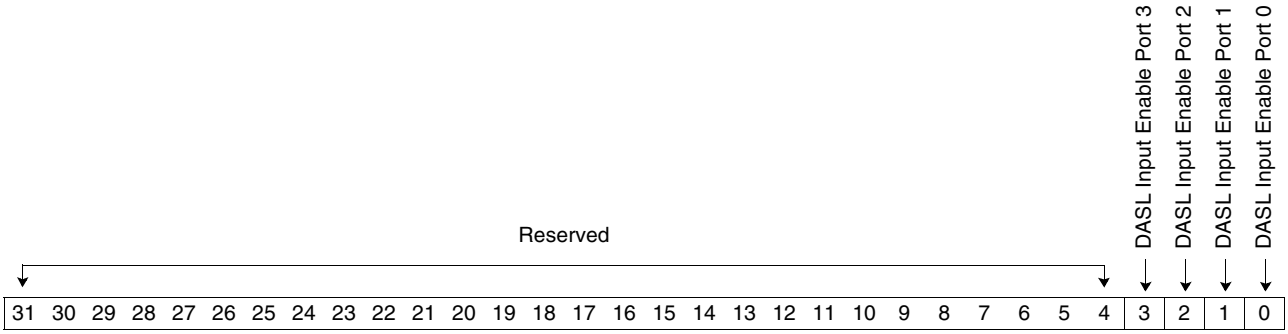
Bit(s)	Field Name	Description
31:4	Reserved	Reserved.
3	DASL Output Enable Port 3	1 Enables normal data transmission on the output port. 0 Forces the data sent by the port to ‘0’.
2	DASL Output Enable Port 2	See the description for bit 3.
1	DASL Output Enable Port 1	See the description for bit 3.
0	DASL Output Enable Port 0	See the description for bit 3.

5.4.3 Input Port Enable Register

Address x‘33’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



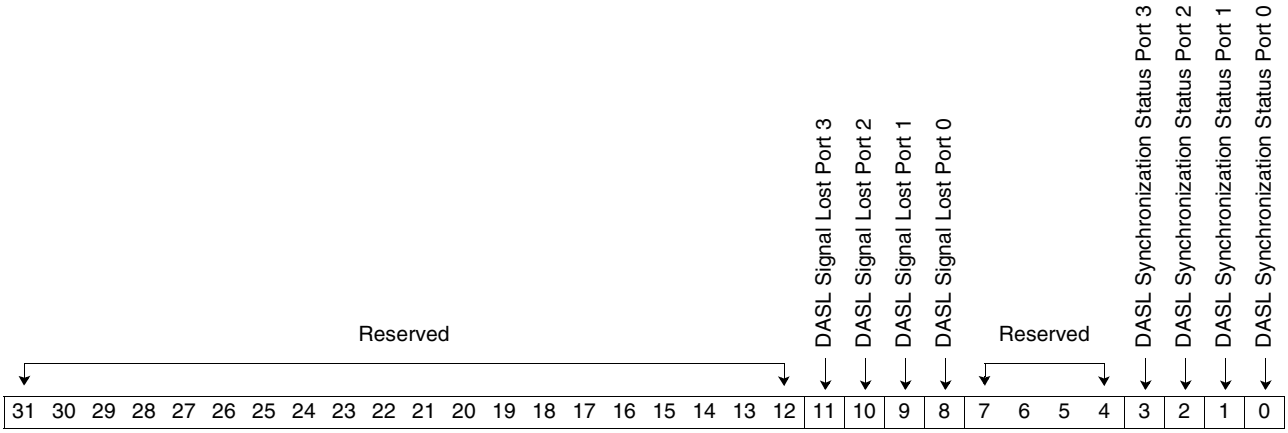
Bit(s)	Field Name	Description
31:-4	Reserved	Reserved.
3	DASL Input Enable Port 3	1 Enables the input port. The picoprocessor can align and synchronize the data stream. 0 Disables the input port. The picoprocessor cannot align and synchronize the data stream, and packets cannot be received.
2	DASL Input Enable Port 2	See the description for bit 3.
1	DASL Input Enable Port 1	See the description for bit 3.
0	DASL Input Enable Port 0	See the description for bit 3.

5.4.4 DASL Status Register

Address x‘34’

Access Type Read Only

Reset Value Undefined



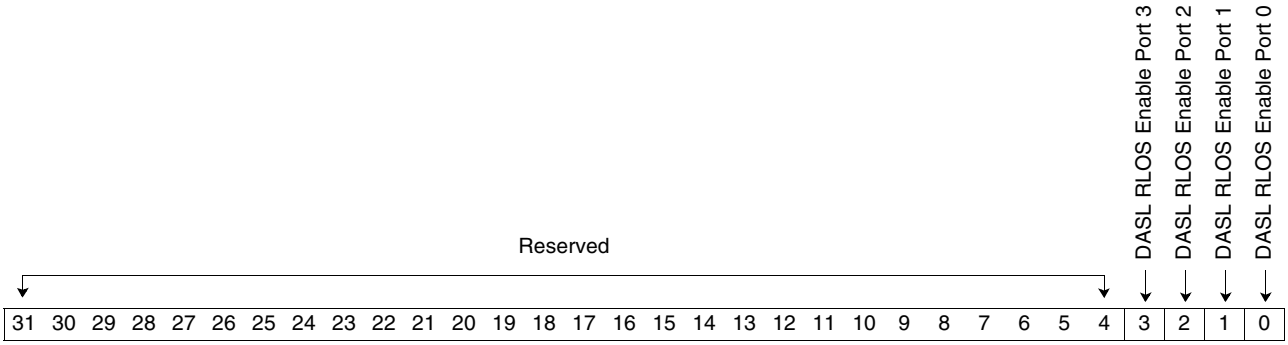
Bit(s)	Field Name	Description
31:12	Reserved	Reserved.
11	DASL Signal Lost Port 3	1 Does not detect a signal on at least one port link. 0 Detects a correct signal on each port link. If not masked, a change in a DASL Signal Lost bit sets the DASL Signal Interrupt bit in the *Status Register* (page 53) to ‘1’.
10	DASL Signal Lost Port 2	See the description for bit 11.
9	DASL Signal Lost Port 1	See the description for bit 11.
8	DASL Signal Lost Port 0	See the description for bit 11.
7:4	Reserved	Reserved.
3	DASL Synchronization Status Port 3	Indicates the status of the link synchronization sequence (including bit phase alignment and packet delineation) initiated by a synchronization hunt command issued through the *DASL Synchronization Hunt Register* (page 101): 1 The port synchronization sequence is complete and normal packet reception is enabled. 0 Either the synchronization sequence is incomplete or the port is disabled. **Note:** Bits 3:0 correspond to the four rx_data_indicator signals.
2	DASL Synchronization Status Port 2	See the description for bit 3.
1	DASL Synchronization Status Port 1	See the description for bit 3.
0	DASL Synchronization Status Port 0	See the description for bit 3.

5.4.5 SDC RLOS Enable Register

Address x‘35’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



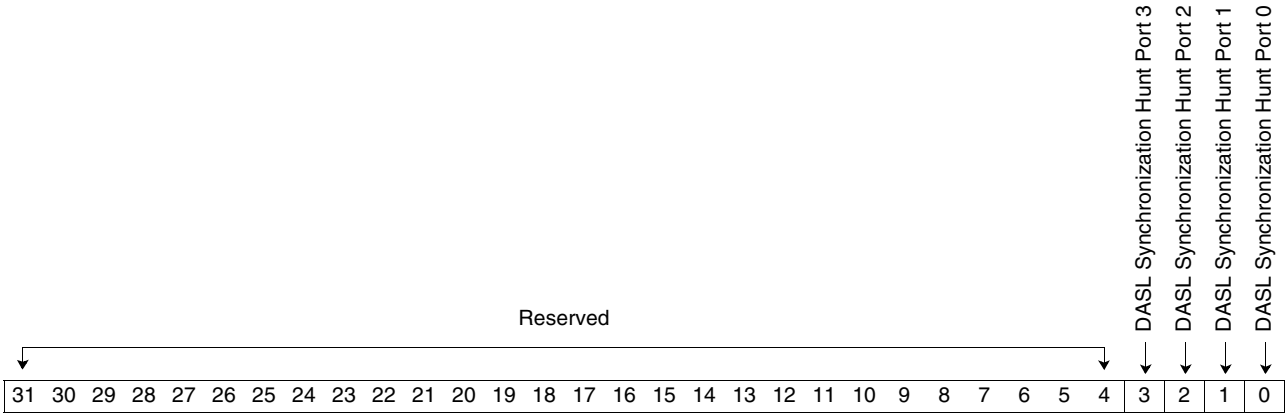
Bit(s)	Field Name	Description
31:4	Reserved	Reserved.
3	DASL RLOS Enable Port 3	1 Enables the SDC to react to a receiver loss of signal (RLOS) assertion on the port receiver by resetting the port phase-alignment state machine. The port receivers must be resynchronized. 0 Disables the SDC from reacting to an RLOS condition on the port receiver. The *DASL Status Register* (page 99) reports the RLOS condition.
2	DASL RLOS Enable Port 2	See the description for bit 3.
1	DASL RLOS Enable Port 1	See the description for bit 3.
0	DASL RLOS Enable Port 0	See the description for bit 3.

5.4.6 DASL Synchronization Hunt Register

Address x‘36’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



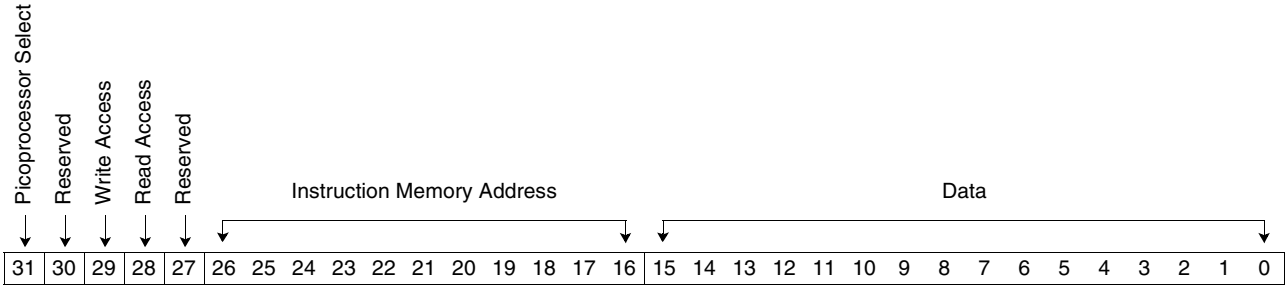
Bit(s)	Field Name	Description
31:4	Reserved	Reserved.
3	DASL Synchronization Hunt Port 3	When set to ‘1’, enables the picoprocessor to start the data stream synchronization sequence (including bit phase alignment and packet delineation) for the corresponding input port. When completed, the picoprocessor sets the corresponding DASL Synchronization Status Port bit in the *DASL Status Register* (page 99) and clears this bit.
2	DASL Synchronization Hunt Port 2	See the description for bit 3.
1	DASL Synchronization Hunt Port 1	See the description for bit 3.
0	DASL Synchronization Hunt Port 0	See the description for bit 3.

5.4.7 Picoprocessor Instruction Memory Access Register

Address x‘37’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	Picoprocessor Select	Set to ‘1’ for access requests to and from the picoprocessor instruction memory.
30	Reserved	Reserved.
29	Write Access	Set to ‘1’ for write access.
28	Read Access	Set to ‘1’ for read access. Read access is performed in two steps: 1. Sets bit 31 to ‘1’ and specifies the instruction memory address in bits 26:16. The data field is ignored. 2. Reads the register to return the data field value.
27	Reserved	Reserved.
26:16	Instruction Memory Address	Specifies the instruction memory address (up to 2048).
15:0	Data	Specifies the data for a write operation and holds the returned data for a read operation.

5.4.8 DASL Configuration Register

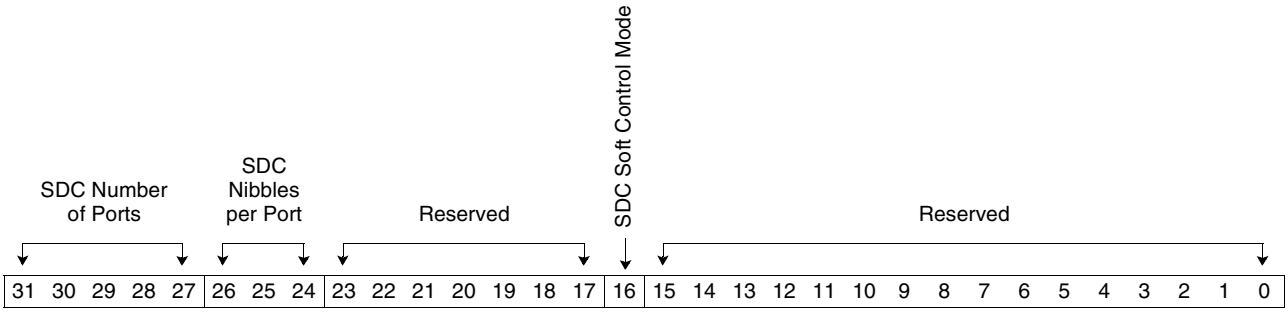
This register must be loaded before the Shared DASL Controller Reset bit in the *Reset Register* (page 58) is released and before the *Picoprocessor Instruction Memory Access Register* (page 102) is loaded. The required loading process is:

1. Set the Shared DASL Controller Reset bit and the Picoprocessor Reset bit in the *Reset Register*.
2. Load this register.
3. Release the Shared DASL Controller Reset bit in the *Reset Register*.
4. Load the *Picoprocessor Instruction Memory Access Register*.
5. Release the Picoprocessor Reset bit in the *Reset Register*.

Address x‘38’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



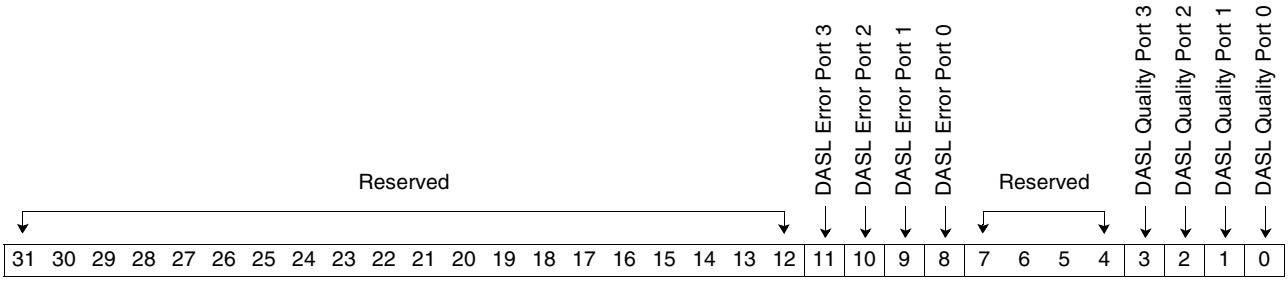
Bit(s)	Field Name	Description
31:27	SDC Number of Ports	The number of physical ports handled by the picoprocessor minus one. Must be set to ‘00011‘.
26:24	SDC Nibbles per Port	The number of physical DASLs per port minus one. Must be set to ‘111’.
23:17	Reserved	Reserved.
16	SDC Soft Control Mode	SDC software control mode. Must be set to ‘1’.
15:0	Reserved	Reserved.

5.4.9 DASL Port Error/Quality Register

Address x‘39’

Access Type Read Only

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



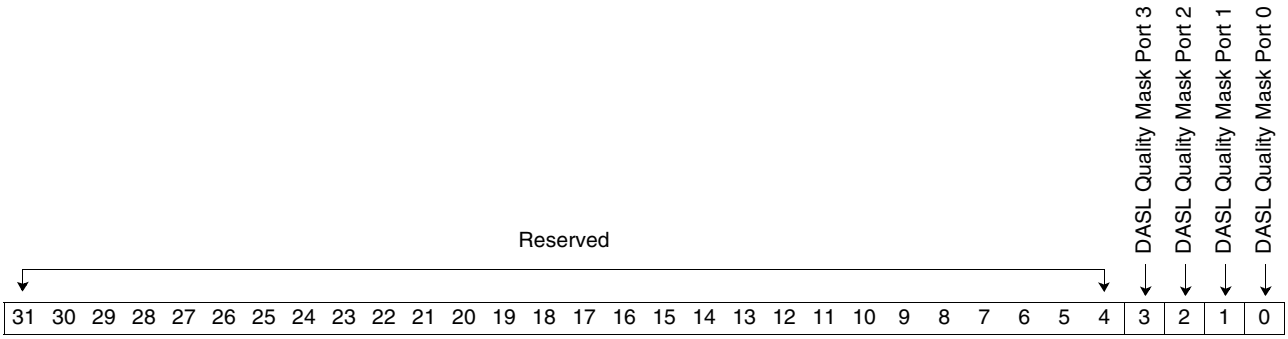
Bit(s)	Field Name	Description
31:12	Reserved	Reserved.
11	DASL Error Port 3	When set to ‘1’, the DASL receiver state machine has detected an error on the receive port.
10	DASL Error Port 2	See the description for bit 11.
9	DASL Error Port 1	See the description for bit 11.
8	DASL Error Port 0	See the description for bit 11.
7:4	Reserved	Reserved.
3	DASL Quality Port 3	When set to ‘1’, the picoprocessor has detected a minimum-eye violation on the receive port. A minimum eye violation indicates that one or more of the port links are operating outside of device specifications (see the *Glossary* on page 145).
2	DASL Quality Port 2	See the description for bit 3.
1	DASL Quality Port 1	See the description for bit 3.
0	DASL Quality Port 0	See the description for bit 3.

5.4.10 DASL Port Quality Mask Register

Address x‘3A’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:4	Reserved	Reserved.
3	DASL Quality Mask Port 3	When set to ‘1’, resets the corresponding DASL Quality Port bit in the *DASL Port Error/Quality Register* (page 104).
2	DASL Quality Mask Port 2	See the description for bit 3.
1	DASL Quality Mask Port 1	See the description for bit 3.
0	DASL Quality Mask Port 0	See the description for bit 3.

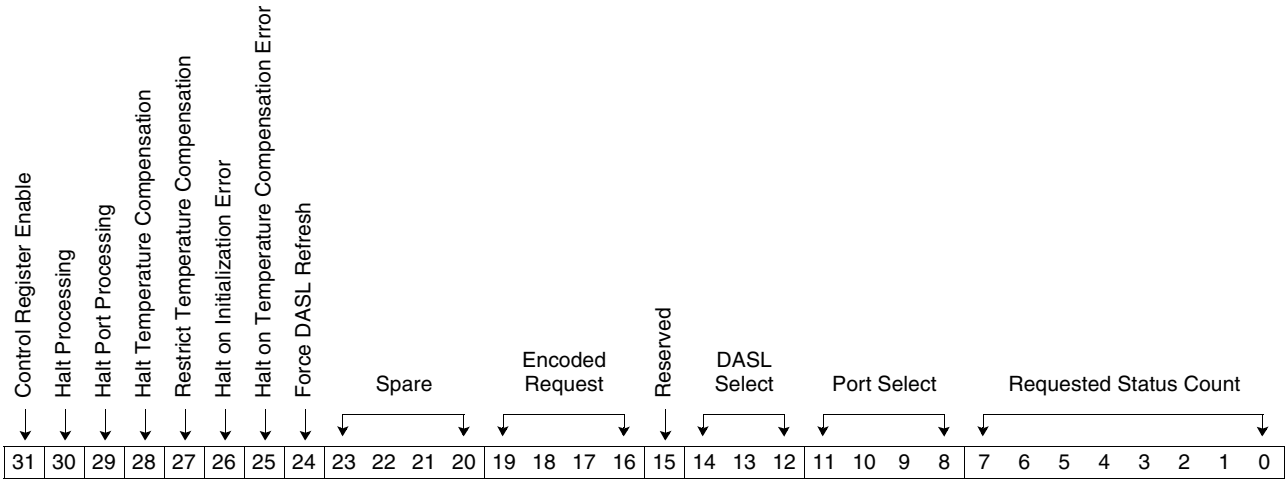
5.4.11 SDC Resource Control Register

This register is not used in normal operating mode.

Address x‘3B’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31	Control Register Enable	1 Enables the register content. 0 Ignores all the other register fields except the Requested Status Count field.
30	Halt Processing	When set to ‘1’, the picoprocessor stops all processing.
29	Halt Port Processing	When set to ‘1’, the picoprocessor stops all processing but continues to update the status and respond to debug requests.
28	Halt Temperature Compensation	When set to ‘1’, the picoprocessor does not perform any port-processing functions beyond initialization.
27	Restrict Temperature Compensation	When set to ‘1’, the picoprocessor performs all port-processing functions but does not adjust the multiplexer setting beyond initialization.
26	Halt on Initialization Error	When set to ‘1’, the picoprocessor stops all processing after the next initialization error.
25	Halt on Temperature Compensation Error	When set to ‘1’, the picoprocessor stops all processing after the next data mode.
24	Force DASL Refresh	When set to ‘1’, the picoprocessor writes the current DASL receiver settings to all ports that have completed initialization but does not perform data mode compensation.
23:20	Spare	Spare.

Bit(s)	Field Name	Description
19:16	Encoded Request	Specifies which services the picocode should perform: 0000 No operation. 0001 Request a read to the address in the *SDC Resource Address Register* (page 108). 0010 Request a write to the address in the *SDC Resource Address Register*. 0101 Load sample memory. 1000 Request a delay line sample from the DASL specified by the Port Select and DASL Select fields. 1001 Update the DASL data structure with the *SDC Resource Data Register* (page 108) input for the DASL receiver specified by the Port Select and DASL Select fields. Others Reserved.
15	Reserved	Reserved.
14:12	DASL Select	Specifies the DASL of the selected port (bits 11:8) for a given action: 000 Link 0 100 Link 4 001 Link 1 101 Link 5 010 Link 2 110 Link 6 011 Link 3 111 Link 7
11:8	Port Select	Specifies the port for a given action. A request that uses this field is processed at the next port service opportunity. If the specified port is outside the port range, the request is processed for port 0. 0000 DASL port 0 0001 DASL port 1 0010 DASL port 2 0011 DASL port 3
7:0	Requested Status Count	The picoprocessor reads, increments, and returns the contents of this field from the Updated Status Count field in the *SDC Status Register* (page 109). This field verifies that the picoprocessor is operating correctly.

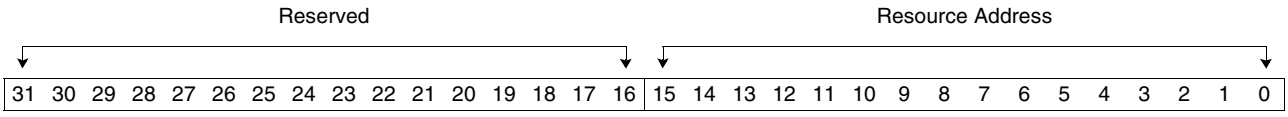
5.4.12 SDC Resource Address Register

This register is not used in normal operating mode.

Address x‘3C’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:16	Reserved	Reserved.
15:0	Resource Address	Specifies the resource address for a read or write operation, enabling indirect access to the local store and picoprocessor I/O registers.

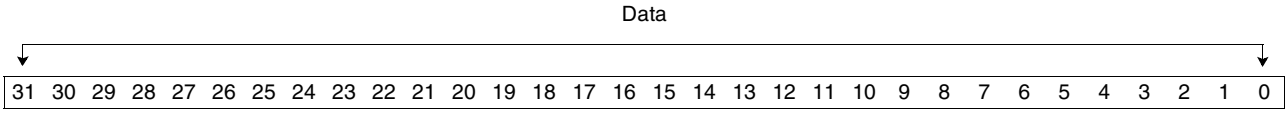
5.4.13 SDC Resource Data Register

This register is not used in normal operating mode.

Address x‘3D’

Access Type Read/Write

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:0	Data	Contains the SDC resource data for read and write operations.

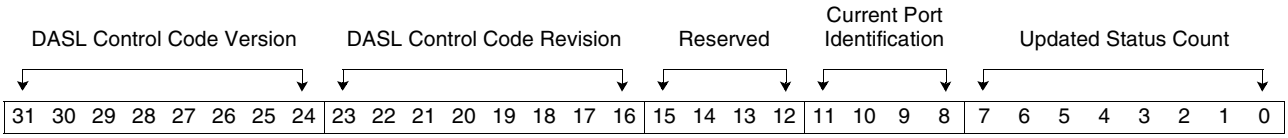
5.4.14 SDC Status Register

This register is loaded by the functional picocode when the Picoprocessor Reset bit in the *Reset Register* (page 58) is released.

Address x‘3E’

Access Type Read Only

Reset Value ‘0000 0000 0000 0000 0000 0000 0000 0000’



Bit(s)	Field Name	Description
31:24	DASL Control Code Version	The DASL control version that is running.
23:16	DASL Control Code Revision	The DASL control revision that is running.
15:12	Reserved	Reserved.
11:8	Current Port Identification	The port number currently being processed by the SDC: 0000 DASL port 0 0001 DASL port 1 0010 DASL port 2 0011 DASL port 3
7:0	Updated Status Count	Written by the picoprocessor to be one count higher than the value of the Requested Status Count field in the *SDC Resource Control Register* (page 106). This field verifies that the picoprocessor is operating correctly.

6. Reset, Initialization, and Operation

6.1 Reset Sequence

This sequence must be executed after card power-up.

1. Activate the PowerOnResetIn# input pin and start the ProcessorClkIn.
2. Deactivate the PowerOnResetIn# input pin after at least three ProcessorClkIn cycles.
3. Write the *Internal/DASL PLL Programming Register* (page 55) and the *HSS PLL Programming Register* (page 56) with the correct values and release the PLL reset bits.
4. Wait 500 µs.
5. Set the Off-Chip Driver Enable bit in the *Reset Register* (page 58).
6. Release the Flush bit in the *Reset Register*.
7. Write the *DASL Configuration Register* (page 103) with the appropriate value.
8. Release the Shared DASL Controller Reset bit in the *Reset Register*.
9. Load the functional picocode into the picoprocessor instruction memory.
10. Release the Picoprocessor Reset bit in the *Reset Register*.
11. Read the *Status Register* (page 53) to clear all interrupt signals.
12. If needed, release the Global Interrupt Mask bit in the *Reset Register*.
13. Enable the two HSS receive macros in the *HSS Receive Command Register* (page 71) and the two HSS transmit macros in the *HSS Transmit Command Register* (page 73).
14. Pool the *HSS Error 1 Register* (page 85) until the four HSS Transmit/Receive PLL Unlock Port bits are reset.
15. Define the configuration bits by writing the *General Configuration Register* (page 62), *HSS Receive Command Register, HSS Transmit Command Register, HSS Receive Buffer Offset Register* (page 79), *HSS Transmit Buffer Offset Register* (page 80), *HSS Power Level Register* (page 90), and four *HSS FIR Registers* (pages 91–94).

6.2 Logic BIST Execution Sequence

This sequence must be executed after a card power-up.

1. Activate the PowerOnResetIn# input pin and start the ProcessorClkIn.
2. Deactivate the PowerOnResetIn# input pin after at least three ProcessorClkIn cycles.
3. Write the *Internal/DASL PLL Programming Register* and the *HSS PLL Programming Register* with the correct values and release the PLL reset bits.
4. Wait 500 µs.
5. Set the Logic BIST Requested bit in the *Reset Register*.
6. Set the PRPG/MISR Data field in the *BIST Data Register* (page 60) with a defined value.
7. Load the *BIST Counter Register* (page 60).

8. Set the Shift Speed and Scan Chain Length fields in the *BIST Select Register* (page 61).
9. Set the Off-Chip Driver Enable bit in the *Reset Register* (page 58).
10. Release the Flush bit in the *Reset Register*.
11. Pool the *Status Register* (page 53) until the Logic BIST Done bit is set.
12. Read the MISR result in the PRPG/MISR Data field of the *BIST Data Register* (page 60).
13. Set the Flush bit and reset the Logic BIST Requested bit in the *Reset Register*.

6.3 Memory BIST Execution Sequence

This sequence must be executed after a card power-up.

1. Activate the PowerOnResetIn# input pin and start the ProcessorClkIn.
2. Deactivate the PowerOnResetIn# input pin after at least three ProcessorClkIn cycles.
3. Write the *Internal/DASL PLL Programming Register* (page 55) and the *HSS PLL Programming Register* (page 56) with the correct values and release the PLL reset bits.
4. Wait 500 µs.
5. Set the Memory BIST Requested bit in the *Reset Register*.
6. Release the Flush bit in the *Reset Register*.
7. Pool the *Status Register* until the Memory BIST Done bit is set.
8. Confirm that the Memory BIST Fail bit is released in the *Status Register*.
9. Set the Flush bit and reset the Memory BIST Requested bit in the *Reset Register*.

6.4 HSS BIST Sequences

High-speed SerDes (HSS) receive and transmit built-in self-test (BIST) sequences can run simultaneously on all HSS ports.

6.4.1 HSS Receive BIST Sequence in Wrap Mode

This test sequence validates an HSS receive port and must be executed after the reset sequence (see *Section 6.1* on page 111).

1. Set the HSS Receive BIST Wrap Port *N* bit in the *HSS Receive BIST Command Register* (page 81).
2. Set the HSS Receive BIST Enable Port *N* bit in the *HSS Receive BIST Command Register*.
3. Set the HSS Receive BIST Reset Port *N* bit in the *HSS Receive BIST Command Register* to clear the HSS Receive BIST Error Port *N* bit in the *HSS Error 1 Register* (page 85).
4. Release the HSS Receive BIST Reset Port *N* bit in the *HSS Receive BIST Command Register*.
5. Monitor the HSS Receive BIST Error Port *N* bit in the *HSS Error 1 Register*.

Note: Once started, the HSS receive BIST runs until the HSS Receive BIST Enable Port *N* bit in the *HSS Receive BIST Command Register* is released.

6.4.2 HSS Receive BIST Sequence in Link Verification Mode

This test sequence validates HSS receive and transmit ports on the same transmission path and must be executed after the reset sequence (see *Section 6.1* on page 111).

1. Confirm that the HSS Receive BIST Wrap Port *N* bit in the *HSS Receive BIST Command Register* (page 81) is set to '0' (normal setting following a reset sequence).
2. Start the HSS transmit BIST sequence on port *n* (see *Section 6.4.3)*.
3. Set the HSS Receive BIST Enable Port *N* bit in the *HSS Receive BIST Command Register*.
4. Set the HSS Receive BIST Reset Port *N* bit in the *HSS Receive BIST Command Register* to clear the HSS Receive BIST Error Port *N* bit in the *HSS Error 1 Register* (page 85).
5. Release the HSS Receive BIST Reset Port *N* bit in the *HSS Receive BIST Command Register*.
6. Monitor the HSS Receive BIST Error Port *N* bit in the *HSS Error 1 Register*.

Note: Once started, the HSS receive BIST runs until the HSS Receive BIST Enable Port *N* bit in the *HSS Receive BIST Command Register* is released.

6.4.3 HSS Transmit BIST Sequence

This test sequence must be executed after the reset sequence (see *Section 6.1* on page 111).

1. Set the HSS Transmit BIST Enable Port *N* bit in the *HSS Transmit BIST Command Register* (page 83).
2. Set the HSS Transmit BIST Reset Port *N* bit in the *HSS Transmit BIST Command Register* to clear the HSS Transmit BIST Error Port *N* bit in the *HSS Error 1 Register*.
3. Release the HSS Transmit BIST Reset Port *N* bit in the *HSS Transmit BIST Command Register*.
4. Monitor the HSS Transmit BIST Error Port *N* bit in the *HSS Error 1 Register*.

Note: Once started, the HSS transmit BIST runs until the HSS Transmit BIST Enable Port *N* bit in the *HSS Transmit BIST Command Register* is released.

6.5 Port Activation Sequences

The PowerPRS 64G, SCIC, and C192 all require a port activation procedure. The following procedures describe the port activation sequence executed by the PowerPRS SCIC local processor. For the port activation sequence executed on the other PowerPRS devices, refer to the corresponding datasheet (see *Related Documents* on page 153).

Note: The PowerPRS SCIC data-aligned synchronous link (DASL) interface is attached to eight PowerPRS 64G ports configured for speed expansion and port paralleling. Port activation must be performed on all four PowerPRS SCIC ports simultaneously.

6.5.1 Ingress Port Activation

The following procedure activates a port on the ingress path.

After a reset sequence:

1. Wait until all eight HSS Receive Signal Lost Port bits in the *HSS Error 1 Register* are cleared.

2. Set the eight HSS Receive Enable Port bits in the *HSS Receive Command Register* (page 71).
3. Wait until all eight HSS RX Synchronization Status Port bits in the *HSS Synchronization Status 1 Register* (page 75) and *HSS Synchronization Status 2 Register* (page 76) report '11'.
4. Perform the following logical unit (LU) deskew process:
   a. Read the eight HSS Receive K Position Port bits in the *HSS Synchronization Status 1 Register* and *HSS Synchronization Status 2 Register*.
   b. Calculate the correction (number of delay cycles) to apply to the LUs on each HSS port.
   c. Write the eight HSS Receive Deskew Command Port bits in the *HSS Ingress Deskew Command Register* (page 78).
   d. Read the eight HSS Receive K Position Port bits in the *HSS Synchronization Status Registers* again to verify that the LU deskew process is complete (this step is optional).
5. Set the Receive Data Mode bit in the *HSS Ingress Deskew Command Register.*
6. Wait until all eight HSS Receive Data Valid Port bits in the *HSS Synchronization Status 3 Register* (page 77) are set to '1'.
7. Set the four DASL Output Enable Port bits in the *Output Port Enable Register* (page 97).
8. Set the four DASL Output Driver Enable Port bits in the *DASL Output Driver Enable Register* (page 96).
9. When PowerPRS 64G synchronization is complete, set the Idle Mode bit in the *HSS Ingress Deskew Command Register* and read the *Yellow Packet Register* (page 64), *Packet Error Register* (page 66), *HSS Error Registers* (pages 85–87), and *Status Register* (page 53) to clear any error indicators that may have been set during synchronization.

6.5.2 Egress Port Activation

The following procedure activates a port on the egress path.

After a reset sequence:

1. Wait until all four DASL Signal Lost Port bits in the *DASL Status Register* (page 99) are cleared.
2. Set the four DASL Input Enable Port bits in the *Input Port Enable Register* (page 98).
3. Start the DASL synchronization process by setting the four DASL Synchronization Hunt Port bits in the *DASL Synchronization Hunt Register* (page 101).
4. Wait until all four DASL Synchronization Status Port bits in the *DASL Status Register* are set to '1'.
5. Perform the following DASL deskew process:
   a. Read the four Start of Packet bits in the *Egress Deskew Status Register* (page 67).
   b. Calculate the correction (number of delay cycles) to apply to each DASL port.
   c. Write the four Egress Deskew Command bits in the *Egress Deskew Command Register* (page 68).
   d. Read the four Start of Packet bits in the *Egress Deskew Status Register* again to verify that the DASL deskew process is complete (this step is optional).
6. Set the Egress Data Mode bit in the *Egress Deskew Command Register*.
7. Read the *Yellow Packet Register, Packet Error Register,* and *Status Register* to clear any error indicators that may have been set during synchronization.

8. Set the eight HSS Transmit Enable Port bits in the *HSS Transmit Command Register* (page 73).
9. Set the eight HSS Transmit Driver Enable Port bits in the *HSS Transmit Command Register.*

6.5.3 Port Activation in PowerPRS C192 Loopback Mode

The following procedure activates a port in PowerPRS C192 loopback mode.

After a reset sequence:

1. Set the C192 Loopback bit in the *General Configuration Register* (page 62).
2. Execute the entire ingress port activation sequence in *Section 6.5.1* on page 113. Steps 7 and 8 are optional because the DASLs do not need to be synchronized.
3. Execute steps 6 through 9 of the egress port activation sequence in *Section 6.5.2* on page 114. Step 4 is optional.

6.5.4 Port Activation in PowerPRS 64G Loopback Mode

The following procedure activates a port in PowerPRS 64G loopback mode.

After a reset sequence:

1. Set the Switch Loopback bit in the *General Configuration Register.*
2. Release the Hardware Auto Disable on Signal Lost and Hardware Auto Disable on Synchronization Lost bits in the *HSS Receive Command Register* (page 71).
3. Execute steps 1 through 8 of the egress port activation sequence in *Section 6.5.2*.
4. Execute steps 2 through 9 of the ingress port activation sequence in *Section 6.5.1*. Step 4 is optional.

7. I/O Definitions and I/O Timing

7.1 I/O Definitions

All functional I/O signals are 3.3-V tolerant 2.5-V CMOS-compatible drivers and receivers except the following:

- High-speed SerDes (HSS) interface signals (common mode logic)
- Data-aligned synchronous link (DASL) interface signals (high-speed transceiver logic)
- HSS and DASL clock and phase-locked loop (PLL) signals (low-voltage pseudoemitter-coupled logic)
- Test signals (1.8-V CMOS-compatible drivers and receivers)

Note: Nondifferential signals are active high unless there is a # symbol at the end of the signal name, in which case the signal is active low. Differential pairs are designated by a _P for the positive signal and an _N for the negative signal at the end of the signal name.

7.1.1 Programming Interface

Figure 7-1. Parallel Processor Interface Signals

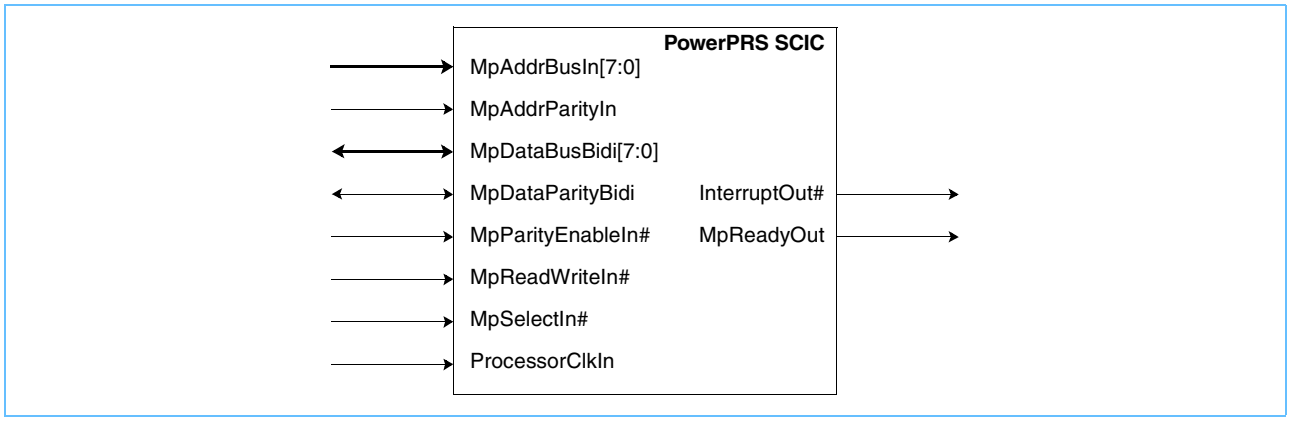


Table 7-1. Parallel Processor Interface Signal Definitions (Page 1 of 2)

Signal Name	Direction	I/O Type	Description
InterruptOut#	Output	2.5-V LVCMOS	Used to generate interrupt signals to the local processor. This signal remains asserted until an serial host interface (SHI) read status command is executed. To support a wired-OR configuration, InterruptOut# uses an open-drain driver and is in the high-impedance state when inactive.
MpAddrBusIn[7:0]	Input	2.5-V LVCMOS	Parallel processor address bus. MpAddrBusIn[0] is the least significant bit. MpAddrBusIn{7:6] are not used and can be left unconnected.
MpAddrParityIn	Input	2.5-V LVCMOS	Parallel processor address bus odd parity (verified by the PowerPRS SCIC). This signal is optional and can be set through an interface pin.
MpDataBusBidi[7:0]	Bidirec-tional	2.5-V LVCMOS	Parallel processor data bus. These signals are in a high-impedance state when no accesses are being processed. MpDataBusBidi[0] is the least sig-nificant bit.

Table 7-1. Parallel Processor Interface Signal Definitions (Page 2 of 2)

Signal Name	Direction	I/O Type	Description
MpDataParityBidi	Bidirec-tional	2.5-V LVCMOS	Parallel processor data bus odd parity. This signal is optional and can be set through an interface pin. It is in a high-impedance state when no accesses are being processed. The PowerPRS SCIC verifies data bus parity during a write operation and calculates it during a read operation.
MpParityEnableIn#	Input	2.5-V LVCMOS	Enables the calculation and verification of local parallel processor data and address parity.
MpReadWriteIn#	Input	2.5-V LVCMOS	Indicates read or write operations on the local parallel processor bus. Read/write line: read operation when low; write operation when high.
MpReadyOut	Output	2.5-V LVCMOS	Indicates when a transfer cycle is complete. The PowerPRS SCIC asserts this signal to end a transfer cycle.
MpSelectIn#	Input	2.5-V LVCMOS	Selects the device for local parallel processor access. The PowerPRS SCIC is selected when low.
ProcessorClkIn	Input	2.5-V LVCMOS	SHI and parallel processor interface clock. Minimum frequency is 25 MHz and maximum frequency is 66 MHz.

Table 7-2. Serial Host Interface Signal Definitions

Signal Name	Direction	I/O Type	Description
SelectSerialHostIn	Input	2.5-V LVCMOS	When high, enables the SHI. When low, enables the eight-bit parallel processor interface.
SHIDataIn	Input	2.5-V LVCMOS	Serial data line that shifts into the *SHI Instruction Register* (page 48).
SHIDataOut	Output	2.5-V LVCMOS	Serial data line that shifts out of the *SHI Instruction Register.* This signal is in a high-impedance state when the SHI is not in shift state. The SHI is in shift state one processor clock cycle after SHISelectIn# becomes inactive.
SHISelectIn#	Input	2.5-V LVCMOS	Enables SHI operation. An SHI instruction is serially shifted into the *SHI Instruction Register* one processor clock cycle after the SHISelectIn# signal becomes active.

7.1.2 HSS Interface

Table 7-3. High-Speed SerDes Interface Signal Definitions (Page 1 of 2)

Signal Name	Direction	I/O Type	Description
HssData[0:7]In_N HssData[0:7]In_P	Differential input		HssData[*n*]In_N and HssData[*n*]In_P form the 2.5-Gbps (2-Gbps payload) differential pairs that transfer PowerPRS SCIC input from the PowerPRS C192.
HssData[0:7]Out_N HssData[0:7]Out_P	Differential output		HssData[*n*]Out_N and HssData[*n*]Out_P form the 2.5-Gbps (2-Gbps payload) differential pairs that transfer PowerPRS SCIC output to the PowerPRS C192.
HssLtestIn	Input	1.8-V LVCMOS	HSS logic test mode input. At the card level, HssLtestIn must be directly connected to HssLtestOut.
HssLtestOut	Output	1.8-V LVCMOS	HSS logic test mode output.
HssMtestIn	Input	1.8-V LVCMOS	HSS macro test mode input. An internal pulldown resistor forces the inactive state.
RxAv25In[0:1]	Input		HSS receive macro 2.5-V analog power supply.
RxAvRegOut[0:1]	Output		HSS receive macro observation point for the internal voltage regulator.
RxAvTTIn[0:1]	Input		HSS receive macro 1.8-V analog termination voltage.

Table 7-3. High-Speed SerDes Interface Signal Definitions (Page 2 of 2)

Signal Name	Direction	I/O Type	Description
TxAv25In[0:1]	Input		HSS transmit macro 2.5-V analog power supply.
TxAvRegOut[0:1]	Output		HSS transmit macro observation point for the internal voltage regulator.
TxAvTTIn[0:1]	Input		HSS transmit macro 1.8-V analog termination voltage.

7.1.3 DASL Interface

The data-aligned synchronous link (DASL) interface supports high-speed transceiver logic (HSTL) serial links. HSTL is specified in the JEDEC Standard No. 8-6 (see *Related Documents* on page 153).

Table 7-4. DASL Interface Signal Definitions

Signal Name	Direction	I/O Type	Description
DaslData[0:3]In[0:7]_N DaslData[0:3]In[0:7]_P	Differential input	HSTL	DaslData[*p*]In[*n*]_N and DaslData[*p*]In[*n*]_P form one of the eight 500-Mbps differential pairs that transfer PowerPRS SCIC input from the PowerPRS 64G.
DaslData[0:3]Out[0:7]_N DaslData[0:3]Out[0:7]_P	Differential output	HSTL	DaslData[*p*]Out[*n*]_N and DaslData[*p*]Out[*n*]_P form one of the eight 500-Mbps differential pairs that transfer PowerPRS SCIC output to the PowerPRS 64G.
MemoryGrantIn[0:3]	Input	2.5-V LVCMOS	These four PowerPRS 64G-generated signals indicate if the switch shared memory is above or below its packet storage capacity for a specific priority. These signals are set to ‘0’ when the PowerPRS 64G *cannot* accept data packets from the PowerPRS SCIC because the shared memory is full and to ‘1’ when the PowerPRS 64G *can* accept data packets from the PowerPRS SCIC.
SendGrantOut	Output	2.5-V LVCMOS	This signal transmits the four send grant bits encoded according to the pattern defined in *Section 3.3.5 Send Grant Serializer* on page 36. In reset mode, this signal is forced to a high impedance state.

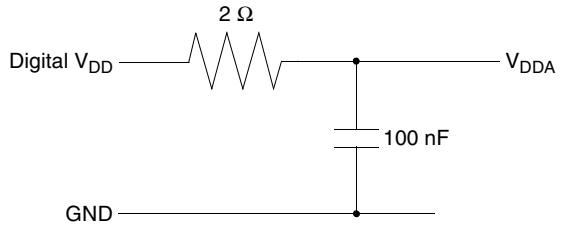
7.1.4 HSS and DASL Clocks and PLLs

Table 7-5. HSS and DASL Clock and PLL Signal Definitions

Signal Name	Direction	I/O Type	Description
DaslClockIn_N DaslClockIn_P	Differential input	HSTL (balanced)	The switch core system clock used for internal and DASL clock generation in the switch interface side. Clock frequency is 53.125 MHz to 62.5 MHz.
DaslPLLGndaIn	Input	DASL PLL Analog GND	Provides a dedicated filtered voltage to the DASL PLL. (DC test I/O)
DaslPLLVddaIn	Input	DASL PLL Analog V_{DD}	Provides a dedicated filtered voltage to the DASL PLL. This signal must be connected to 1.8 V. (DC test I/O)
HssClockIn_N HssClockIn_P	Differential input	PECL (balanced)	The clock used for HSS clock generation in the PowerPRS C192 interface side. Clock frequency is 106.25 MHz to 125 MHz.
HssPLLGndaIn	Input	HSS PLL Analog GND	Provides a dedicated filtered voltage to the HSS PLL. (DC test I/O)
HssPLLVddaIn	Input	HSS PLL Analog V_{DD}	Provides a dedicated filtered voltage to the HSS PLL. This signal must be connected to 2.5 V. (DC test I/O)

To isolate the PLL from the noisy internal digital V_{DD} signal, the analog V_{DD} signal is connected to a dedicated package pin. If limited noise is expected at the card level, the analog V_{DD} pin can be connected directly to the digital V_{DD} plane; however, it is often prudent to place a filter circuit on the analog V_{DD} pin (see *Figure 7-2).* All wire lengths should be as short as possible to minimize coupling from other signals.

Figure 7-2. Analog V_{DD} Filtering for Each PLL



7.1.5 External Debug

Table 7-6. External Debug Signal Definitions

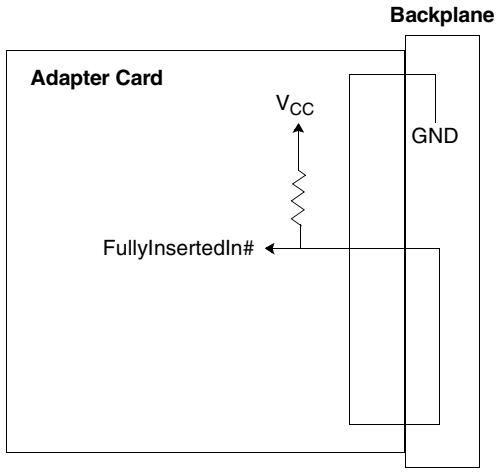
Signal Name	Direction	I/O Type	Description
ACTestIn	Input	2.5-V LVCMOS	Test I/O used to determine the DASL macro propagation delay. (AC test I/O)
ACTestOut	Output	2.5-V LVCMOS	50-ohm tristate common I/O. Test I/O used to determine the DASL macro propagation delay (based on 12 DASL delay lines). (AC test I/O)
DebugBusOut[17:0]	Output	2.5-V LVCMOS	50-ohm tristate common I/O. This 18-bit bus provides direct I/O access (logic analyzer) to the debug bus specified by the *Debug Bus Select Register* (page 69). These drivers are enabled by the Debug Bus Enable bit in the *Debug Bus Select Register*.
Osc625ProbeOut_N Osc625ProbeOut_P	Output	LVDS	Driver connected to the internal 625-MHz oscillator clock tree. This driver is enabled by the Debug Bus Enable bit in the *Debug Bus Select Register*.
Pad_A_In Pad_B_In	Input		Diodes used to measure the device junction temperature.

7.1.6 Miscellaneous

Table 7-7. Miscellaneous External Signal Definitions

Signal Name	Direction	I/O Type	Description
FullyInsertedIn#	Input	2.5-V LVCMOS	This signal forces the DASL and HSS drivers into a high impedance state until both ends of the adapter board housing the PowerPRS SCIC are fully inserted. An external pullup resistor is required to force the inactive state when the board is correctly inserted (see *Figure 7-3* on page 121).
PowerOnResetIn#	Input	2.5-V LVCMOS	50-ohm tristate common I/O. This signal forces a PowerPRS SCIC hardware reset. It resets the external JTAG logic but maintains internal logic after the flush.

Figure 7-3. Detection of a Fully Inserted Adapter Card



7.1.7 Test

Table 7-8. Dedicated Test I/O Signal Definitions (Page 1 of 2)

Signal Name	Direction	I/O Type	Description
DI1#	Input	2.5-V LVCMOS	The nontest driver inhibit for all device boundary outputs. Boundary outputs are device outputs or common I/Os that serve as primary outputs of the internal logic. They must be fed by boundary latches or special boundary logic cells that comprise the boundary logic. When set to '0', this signal disables (tristates) all device boundary outputs. When set to '1', this signal is in an inactive state and all boundary outputs are controlled by normal functions.This pin must be connected externally to logic that drives the appropriate value for system mode.
DI2#	Input	1.8-V LVCMOS	The test driver inhibit for all device nonboundary outputs. Nonboundary outputs are device outputs or common I/Os that transfer test function and level-sensitive scan design (LSSD) data to and from the internal logic. When set to '0', this signal disables (tristates) all device nonboundary outputs. An internal pullup resistor forces the inactive state. When set to '1', this signal is in an inactive state and all nonboundary outputs are controlled by normal functions.
IOTestIn	Input	1.8-V LVCMOS	Forces the use of JTAG EXTEST methodology. An internal pulldown resistor forces the inactive state.
LeakageTestIn	Input	1.8-V LVCMOS	Measures the input leakage current at dc voltage values. (DC test I/O)
Lssd_A_ClkIn	Input	1.8-V LVCMOS	An external source of the internal set/reset latch (SRL) scan A clock. This signal enables the tester to independently source the internal SRL clocks from the primary inputs during LSSD tests. An internal pullup resistor forces the inactive state.
Lssd_B_ClkIn	Input	1.8-V LVCMOS	An external source of the internal SRL scan B clock. This signal enables the tester to independently source the internal SRL clocks from the primary inputs during LSSD tests. An internal pullup resistor forces the inactive state.
Lssd_C1_ClkIn	Input	1.8-V LVCMOS	An external source of the internal SRL scan C clock. This signal enables the tester to independently source the internal SRL clocks from the primary inputs (used for logic) during an LSSD test. An internal pullup resistor forces the inactive state.

Table 7-8. Dedicated Test I/O Signal Definitions (Page 2 of 2)

Signal Name	Direction	I/O Type	Description
Lssd_C3_ClkIn	Input	1.8-V LVCMOS	An external source of the internal multiport register array (MPRA) scan C clock. This signal enables the tester to independently source the internal MPRA clocks from the primary inputs during LSSD tests. An internal pullup resistor forces the inactive state.
Lssd_C4_ClkIn	Input	1.8-V LVCMOS	An external source of the internal SRL scan C clock. This signal enables the tester to independently source the internal SRL clocks from the primary inputs during LSSD tests. An internal pullup resistor forces the inactive state.
LssdTestEnableIn	Input	1.8-V LVCMOS	When forced to a '1', this pin enables the LSSD test mode. When set to '0', this signal is in an inactive state and normal device operation is enabled. (DC test I/O)
RI#	Input	1.8-V LVCMOS	When pulled down ('0'), this signal places all boundary receivers in a known state independent of the receiver input to prevent unknown states from entering the internal logic and to reduce switching activities during internal test. The RI# pin must be pulled up externally for system mode.
ScanIn[0:13]	Input	1.8-V LVCMOS	LSSD scan chain inputs. An internal pulldown resistor is implemented for bits 0:9 and 11. An internal pullup resistor is implemented for bits 10, 12, and 13.
ScanOut[0:13]	Output	2.5-V LVCMOS	LSSD scan chain outputs.
TestM3In	Input	1.8-V LVCMOS	Controls the internal memory BIST controllers.

Table 7-9 presents the I/O test signals that are shared with the test signals defined in *Table 7-8* above.

Table 7-9. Shared Test I/O Signal Definitions

Signal Name	Direction	I/O Type	Description
DASL_PLL_LOCK	Output	1.8-V LVCMOS driver	50-ohm tristate common I/O. This test I/O determines the lock state of the DASL PLL. Shared with ScanOut[9].
DASL_PLL_TESTOUT	Output		During PLL test, the tester must monitor this signal to verify the PLL output frequency. Shared with ScanOut[12].
HSS_PLL_LOCK	Output		1.8-V LVCMOS driver 50-ohm tristate common I/O. This test I/O determines the lock state of the HSS PLL. Shared with ScanOut[8].
HSS_PLL_TESTOUT	Output		During PLL test, the tester must monitor this signal to verify the PLL output frequency. Shared with ScanOut[11].
LSSD_SCAN_GATE	Input	1.8-V LVCMOS	Shared with IOTestIn.
MEMORYBIST_DIAGOUT	Output	1.8-V LVCMOS	Each sram_diagout signal is multiplexed to this MEMORYBIST_DIAGOUT pin to observe the pass/fail flag of individual arrays during the memory BIST diagnostic mode. Shared with ScanOut[7].

Table 7-10. External JTAG Signal Definitions

Signal Name	Direction	I/O Type	Description
TCK	Input	1.8-V LVCMOS receiver tristate common I/O	Test clock input. An internal pullup resistor forces the inactive state. Shared with ScanIn[13].
TDI	Input	1.8-V LVCMOS receiver tristate common I/O	Test data input. An internal pullup resistor forces the inactive state. Shared with ScanIn[10].
TDO	Output	1.8-V LVCMOS 50-ohm tristate common I/O	Test data output. Shared with ScanOut[10].
TMS	Input	1.8-V LVCMOS receiver tristate common I/O	Test mode select input. An internal pullup resistor forces the inactive state. Shared with ScanIn[12].
TRST#	Input	1.8-V LVCMOS receiver tristate common I/O	JTAG test reset. This signal is automatically asserted when the PowerOn-ResetIn# signal (see *Table 7-7* on page 120) is asserted. An internal pullup resistor forces the inactive state.

Note: For a detailed description of these JTAG signals, refer to IEEE Standard 1149.1 listed under *Related Documents* on page 153.

7.2 I/O Timing

7.2.1 Parallel Processor Interface

Figure 7-4. Parallel Processor Read Access

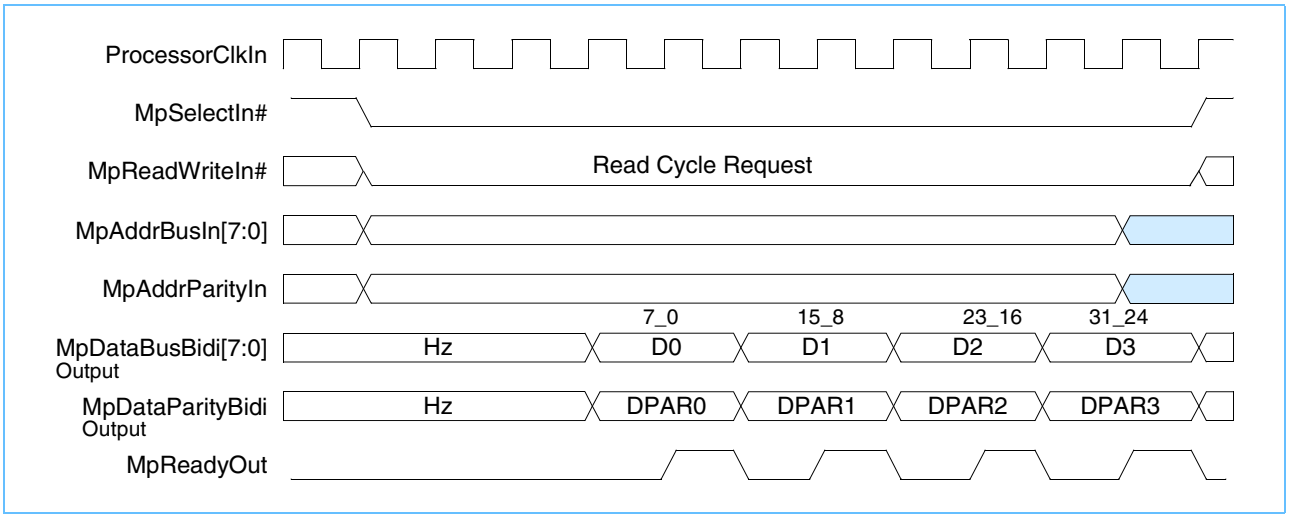


Figure 7-5. Parallel Processor Write Access

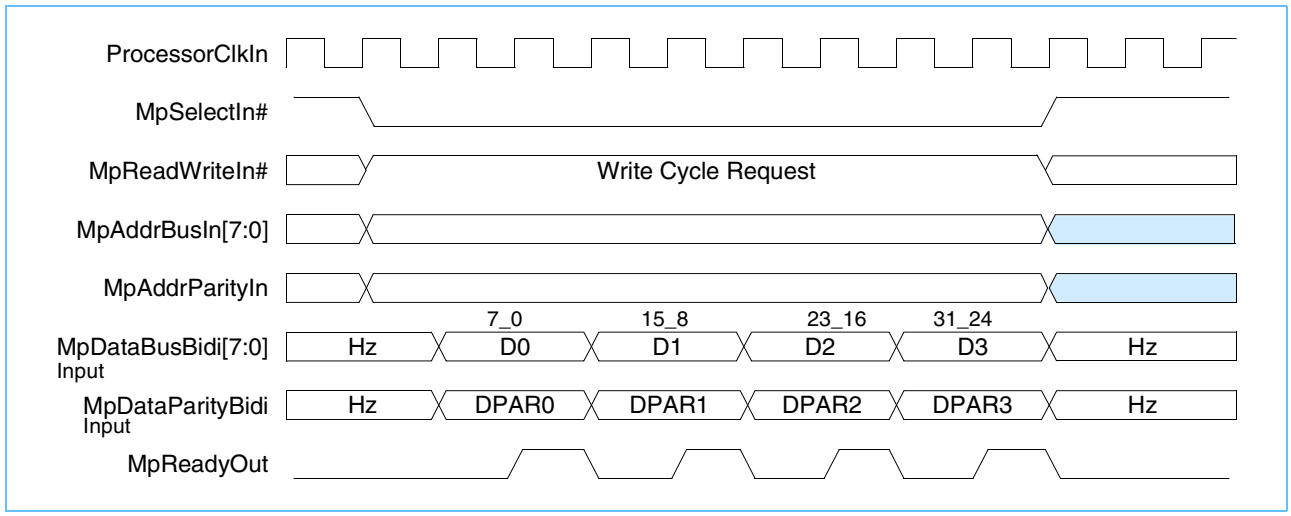


Figure 7-6. Parallel Processor Interface Signal Timing Diagram

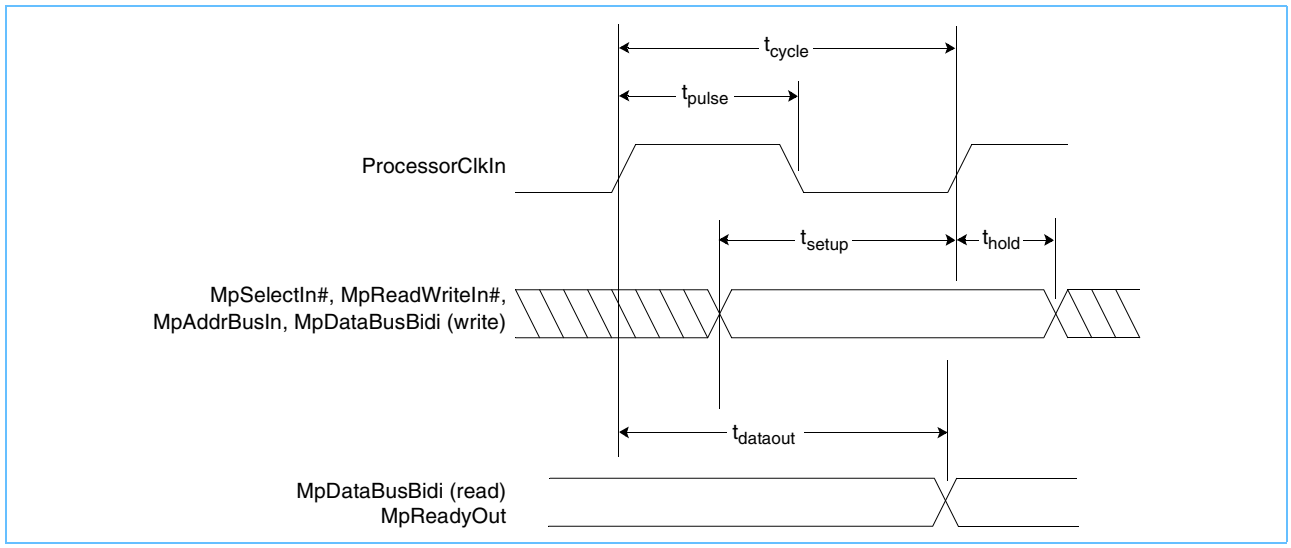


Table 7-11. Parallel Processor Interface Signal Timing Values

Symbol	Parameter	Rating		Units
		Minimum	Maximum	
t_{cycle}	Cycle time	16		ns
t_{pulse}	Pulse width	4		ns
t_{setup}	Setup time	4		ns
t_{hold}	Hold time	5		ns
$t_{dataout}$	ProcessorClkIn to MpDataBusBidi	3	8	ns

7.2.2 Serial Host Interface

Figure 7-7. SHI Signal Timing Diagram

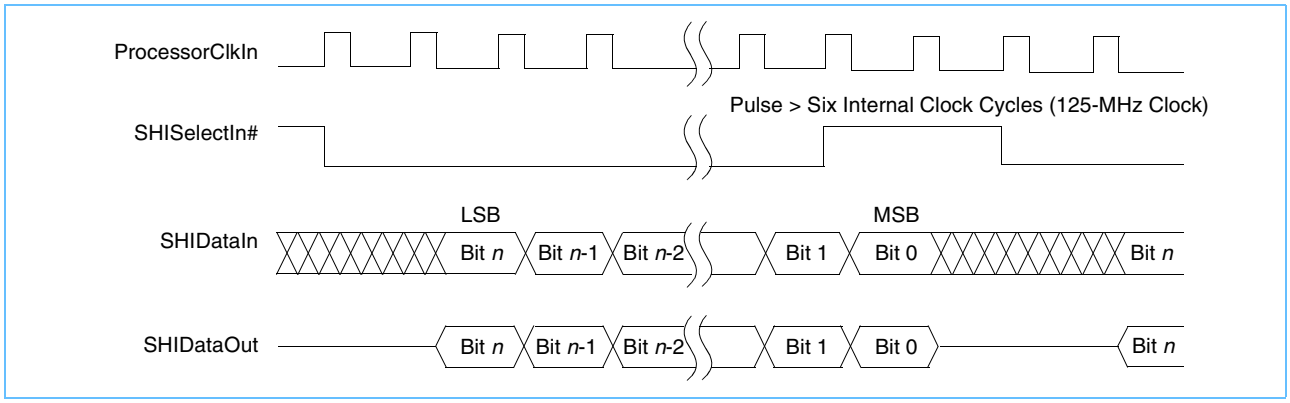


Figure 7-8. SHI Signal-to-Clock Timing Diagram

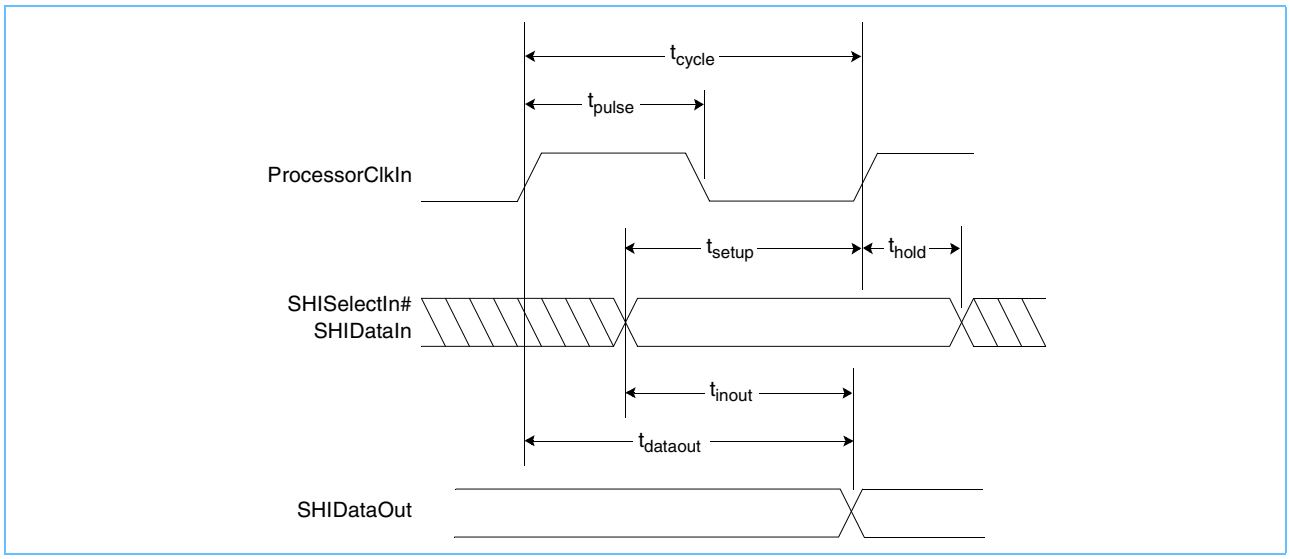


Table 7-12. SHI Signal Timing Values

Symbol	Parameter	Rating		Units
		Minimum	Maximum	
t_{cycle}	Cycle time	16		ns
t_{pulse}	Pulse width	4		ns
t_{setup}	Setup time	4		ns
t_{hold}	Hold time	5		ns
t_{inout}	SHISelectIn# to SHIDataOut	2	6	ns
$t_{dataout}$	ProcessorClkIn to SHIDataOut	3	8	ns

7.2.3 HSS Interface

Table 7-13. HSS Interface Signal Skew Requirements

Parameter	Rating	Units
Maximum skew between the two lines of a differential pair	±20	ps
Maximum skew between two 2.5-Gbps links to the same port	4	ns

7.2.4 DASL Interface

Table 7-14. DASL Interface Signal Skew Requirements

Parameter	Rating	Units	Notes
Maximum skew between the two lines of a differential pair	±130	ps	
Maximum skew between two 500-Mbps links to the same port or to any two ports configured for speed expansion	±2	clock cycles (8 to 10 ns)	1

1. Clock cycle = 8 ns (125-MHz operation) to 10 ns (100-MHz operation).

8. Pin Information

Figure 8-1. Pinout (399-ball HyperBGA package, bottom view)

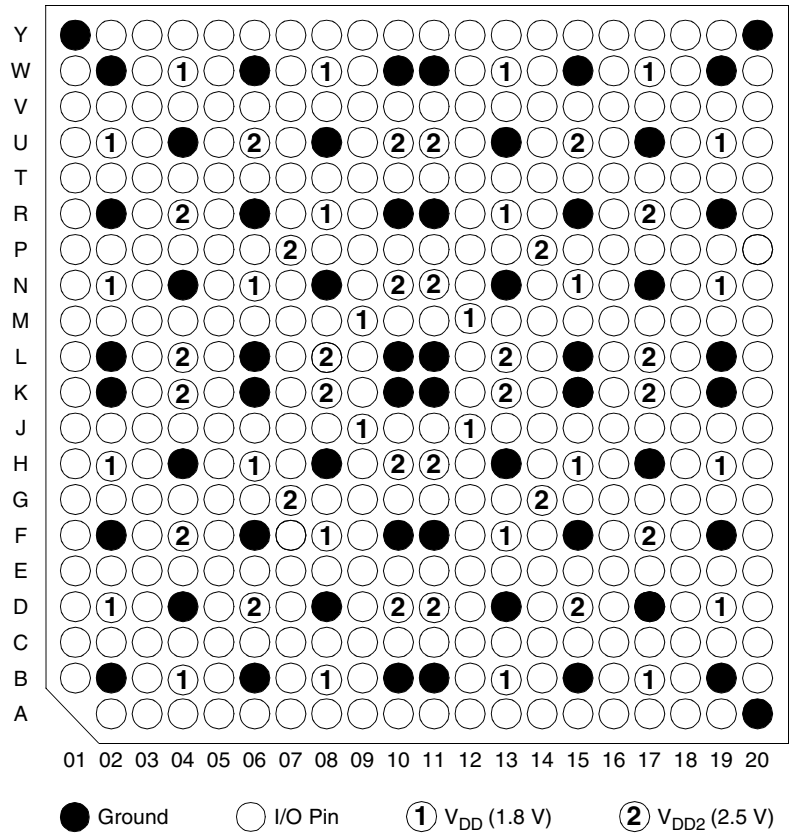


Table 8-1. Ground and V_{DD} Pin Locations

Pin Function	Pin Locations
Ground	A20, B02, B06, B10, B11, B15, B19, D04, D08, D13, D17, F02, F06, F10, F11, F15, F19, H04, H08, H13, H17, K02, K06, K10, K11, K15, K19, L02, L06, L10, L11, L15, L19, N04, N08, N13, N17, R02, R06, R10, R11, R15, R19, U04, U08, U13, U17, W02, W06, W10, W11, W15, W19, Y01, Y20
V_{DD} (1.8 V)	B04, B08, B13, B17, D02, D19, F08, F13, H02, H06, H15, H19, J09, J12, M09, M12, N02, N06, N15, N19, R08, R13, U02, U19, W04, W08, W13, W17
V_{DD2} (2.5 V)	D06, D10, D11, D15, F04, F17, G07, G14, H10, H11, K04, K08, K13, K17, L04, L08, L13, L17, N10, N11, P07, P14, R04, R17, U06, U10, U11, U15

Table 8-2: I/O Signal List Sorted by Signal Name (Continued)

Signal Name	Pin Location	Signal Name	Pin Location	Signal Name	Pin Location
ACTestIn	W09	DaslData[1]In[0]_N	H03	DaslData[2]In[2]_N	N01
ACTestOut	N07	DaslData[1]In[0]_P	G02	DaslData[2]In[2]_P	M02
DaslClockIn_N	A18	DaslData[1]In[1]_N	J02	DaslData[2]In[3]_N	P02
DaslClockIn_P	A19	DaslData[1]In[1]_P	H01	DaslData[2]In[3]_P	N03
DaslData[0]In[0]_N	E06	DaslData[1]In[2]_N	J04	DaslData[2]In[4]_N	L16
DaslData[0]In[0]_P	D05	DaslData[1]In[2]_P	J03	DaslData[2]In[4]_P	K16
DaslData[0]In[1]_N	G05	DaslData[1]In[3]_N	J05	DaslData[2]In[5]_N	M16
DaslData[0]In[1]_P	F05	DaslData[1]In[3]_P	J06	DaslData[2]In[5]_P	M15
DaslData[0]In[2]_N	G03	DaslData[1]In[4]_N	V13	DaslData[2]In[6]_N	P17
DaslData[0]In[2]_P	F03	DaslData[1]In[4]_P	V12	DaslData[2]In[6]_P	N16
DaslData[0]In[3]_N	H05	DaslData[1]In[5]_N	Y14	DaslData[2]In[7]_N	R16
DaslData[0]In[3]_P	G04	DaslData[1]In[5]_P	Y13	DaslData[2]In[7]_P	P16
DaslData[0]In[4]_N	Y08	DaslData[1]In[6]_N	V14	DaslData[2]Out[0]_N	T04
DaslData[0]In[4]_P	Y07	DaslData[1]In[6]_P	U14	DaslData[2]Out[0]_P	T05
DaslData[0]In[5]_N	Y10	DaslData[1]In[7]_N	W16	DaslData[2]Out[1]_N	T02
DaslData[0]In[5]_P	Y09	DaslData[1]In[7]_P	V15	DaslData[2]Out[1]_P	T03
DaslData[0]In[6]_N	Y12	DaslData[1]Out[0]_N	D03	DaslData[2]Out[2]_N	U01
DaslData[0]In[6]_P	Y11	DaslData[1]Out[0]_P	C02	DaslData[2]Out[2]_P	T01
DaslData[0]In[7]_N	W12	DaslData[1]Out[1]_N	E01	DaslData[2]Out[3]_N	V02
DaslData[0]In[7]_P	V11	DaslData[1]Out[1]_P	D01	DaslData[2]Out[3]_P	U03
DaslData[0]Out[0]_N	A04	DaslData[1]Out[2]_N	E04	DaslData[2]Out[4]_N	U16
DaslData[0]Out[0]_P	A05	DaslData[1]Out[2]_P	E05	DaslData[2]Out[4]_P	T15
DaslData[0]Out[1]_N	C03	DaslData[1]Out[3]_N	E03	DaslData[2]Out[5]_N	T17
DaslData[0]Out[1]_P	C04	DaslData[1]Out[3]_P	E02	DaslData[2]Out[5]_P	T16
DaslData[0]Out[2]_N	C06	DaslData[1]Out[4]_N	J18	DaslData[2]Out[6]_N	Y17
DaslData[0]Out[2]_P	B05	DaslData[1]Out[4]_P	J17	DaslData[2]Out[6]_P	Y16
DaslData[0]Out[3]_N	D07	DaslData[1]Out[5]_N	E19	DaslData[2]Out[7]_N	T19
DaslData[0]Out[3]_P	C07	DaslData[1]Out[5]_P	E18	DaslData[2]Out[7]_P	T18
DaslData[0]Out[4]_N	G18	DaslData[1]Out[6]_N	J16	DaslData[3]In[0]_N	R05
DaslData[0]Out[4]_P	F18	DaslData[1]Out[6]_P	J15	DaslData[3]In[0]_P	P05
DaslData[0]Out[5]_N	E17	DaslData[1]Out[7]_N	G19	DaslData[3]In[1]_N	P04
DaslData[0]Out[5]_P	E16	DaslData[1]Out[7]_P	H18	DaslData[3]In[1]_P	N05
DaslData[0]Out[6]_N	G16	DaslData[2]In[0]_N	M05	DaslData[3]In[2]_N	R03
DaslData[0]Out[6]_P	F16	DaslData[2]In[0]_P	M06	DaslData[3]In[2]_P	P03
DaslData[0]Out[7]_N	G17	DaslData[2]In[1]_N	M03	DaslData[3]In[3]_N	U05
DaslData[0]Out[7]_P	H16	DaslData[2]In[1]_P	M04	DaslData[3]In[3]_P	T06

Table 8-2: I/O Signal List Sorted by Signal Name (Continued)

Signal Name	Pin Location	Signal Name	Pin Location	Signal Name	Pin Location
DaslData[3]In[4]_N	L18	DebugBusOut[10]	D14	HssData[5]Out_P	G09
DaslData[3]In[4]_P	K18	DebugBusOut[11]	V05	HssData[6]In_N	G12
DaslData[3]In[5]_N	M18	DebugBusOut[12]	E14	HssData[6]In_P	G11
DaslData[3]In[5]_P	M17	DebugBusOut[13]	E08	HssData[6]Out_N	J10
DaslData[3]In[6]_N	P19	DebugBusOut[14]	T10	HssData[6]Out_P	K09
DaslData[3]In[6]_P	N18	DebugBusOut[15]	T11	HssData[7]In_N	G15
DaslData[3]In[7]_N	R18	DebugBusOut[16]	E10	HssData[7]In_P	F14
DaslData[3]In[7]_P	P18	DebugBusOut[17]	E13	HssData[7]Out_N	E09
DaslData[3]Out[0]_N	V07	DI1#	Y03	HssData[7]Out_P	F09
DaslData[3]Out[0]_P	U07	DI2#	C08	HssLtestIn	V08
DaslData[3]Out[1]_N	W05	FullyInsertedIn#	L05	HssLtestOut	H14
DaslData[3]Out[1]_P	V06	HssClockIn_N	Y18	HssMtestIn	B14
DaslData[3]Out[2]_N	V03	HssClockIn_P	Y19	HssPLLGndaIn	V20
DaslData[3]Out[2]_P	V04	HssData[0]In_N	L12	HssPLLVddaIn	W20
DaslData[3]Out[3]_N	Y04	HssData[0]In_P	M11	InterruptOut#	C01
DaslData[3]Out[3]_P	Y05	HssData[0]Out_N	R07	IOTestIn	K20
DaslData[3]Out[4]_N	V18	HssData[0]Out_P	P06	LeakageTestIn	E11
DaslData[3]Out[4]_P	V17	HssData[1]In_N	R12	Lssd_A_ClkIn	F20
DaslData[3]Out[5]_N	V19	HssData[1]In_P	T12	Lssd_B_ClkIn	G20
DaslData[3]Out[5]_P	U18	HssData[1]Out_N	P10	Lssd_C1_ClkIn	J20
DaslData[3]Out[6]_N	N20	HssData[1]Out_P	P09	Lssd_C3_ClkIn	M20
DaslData[3]Out[6]_P	M19	HssData[2]In_N	P12	Lssd_C4_ClkIn	P20
DaslData[3]Out[7]_N	U20	HssData[2]In_P	P11	LssdTestEnableIn	T13
DaslData[3]Out[7]_P	T20	HssData[2]Out_N	R09	MemoryGrantIn[0]	B01
DaslPLLGndaIn	C20	HssData[2]Out_P	T09	MemoryGrantIn[1]	C11
DaslPLLVddaIn	B20	HssData[3]In_N	P15	MemoryGrantIn[2]	K03
DebugBusOut[0]	B16	HssData[3]In_P	R14	MemoryGrantIn[3]	C10
DebugBusOut[1]	A17	HssData[3]Out_N	M10	MpAddrBusIn[0]	C09
DebugBusOut[2]	V16	HssData[3]Out_P	L09	MpAddrBusIn[1]	H20
DebugBusOut[3]	T14	HssData[4]In_N	K12	MpAddrBusIn[2]	E15
DebugBusOut[4]	C05	HssData[4]In_P	J11	MpAddrBusIn[3]	A16
DebugBusOut[5]	D16	HssData[4]Out_N	F07	MpAddrBusIn[4]	H12
DebugBusOut[6]	V01	HssData[4]Out_P	G06	MpAddrBusIn[5]	C16
DebugBusOut[7]	U12	HssData[5]In_N	E12	MpAddrBusIn[6]	F12
DebugBusOut[8]	T08	HssData[5]In_P	D12	MpAddrBusIn[7]	J19
DebugBusOut[9]	E07	HssData[5]Out_N	G10	MpAddrParityIn	C14

Table 8-2: I/O Signal List Sorted by Signal Name (Continued)

Signal Name	Pin Location	Signal Name	Pin Location	Signal Name	Pin Location
MpDataBusBidi[0]	L03	RxAv25In[0]	M13	ScanOut[4]	B18
MpDataBusBidi[1]	A12	RxAv25In[1]	J14	ScanOut[5]	A13
MpDataBusBidi[2]	U09	RxAvRegOut[0]	L14	ScanOut[6]	C18
MpDataBusBidi[3]	V10	RxAvRegOut[1]	J13	ScanOut[7]	B12
MpDataBusBidi[4]	N09	RxAvTTIn[0]	M14	ScanOut[8]	A11
MpDataBusBidi[5]	C19	RxAvTTIn[1]	K14	ScanOut[9]	A10
MpDataBusBidi[6]	K05	ScanIn[0]	A03	ScanOut[10]	A08
MpDataBusBidi[7]	A14	ScanIn[1]	B03	ScanOut[11]	A06
MpDataParityBidi	C15	ScanIn[2]	A02	ScanOut[12]	Y02
MpParityEnableIn#	V09	ScanIn[3]	F01	ScanOut[13]	B07
MpReadWriteIn#	A07	ScanIn[4]	P01	SelectSerialHostIn	H09
MpReadyOut	A09	ScanIn[5]	G01	SendGrantOut	W01
MpSelectIn#	D18	ScanIn[6]	J01	SHIDataIn	C12
Osc625ProbeOut_N	E20	ScanIn[7]	W07	SHIDataOut	D09
Osc625ProbeOut_P	D20	ScanIn[8]	K01	SHISelectIn#	T07
Pad_A_In	W14	ScanIn[9]	L01	Spare	H07
Pad_B_In	N14	ScanIn[10]	M01	TestM3In	B09
PowerOnResetIn#	N12	ScanIn[11]	Y15	TRST#	W03
ProcessorClkIn	C17	ScanIn[12]	R20	TxAv25In[0]	M07
Reserved	P13	ScanIn[13]	W18	TxAv25In[1]	J08
Reserved	G13	ScanOut[0]	L20	TxAvRegOut[0]	M08
Reserved	P08	ScanOut[1]	A15	TxAvRegOut[1]	K07
Reserved	G08	ScanOut[2]	Y06	TxAvTTIn[0]	L07
RI#	R01	ScanOut[3]	C13	TxAvTTIn[1]	J07

Table 8-3: I/O Signal List Sorted by Pin Location (Continued)

Pin Location	Signal Name	Pin Location	Signal Name	Pin Location	Signal Name
A02	ScanIn[2]	C09	MpAddrBusIn[0]	E15	MpAddrBusIn[2]
A03	ScanIn[0]	C10	MemoryGrantIn[3]	E16	DaslData[0]Out[5]_P
A04	DaslData[0]Out[0]_N	C11	MemoryGrantIn[1]	E17	DaslData[0]Out[5]_N
A05	DaslData[0]Out[0]_P	C12	SHIDataIn	E18	DaslData[1]Out[5]_P
A06	ScanOut[11]	C13	ScanOut[3]	E19	DaslData[1]Out[5]_N
A07	MpReadWriteIn#	C14	MpAddrParityIn	E20	Osc625ProbeOut_N
A08	ScanOut[10]	C15	MpDataParityBidi	F01	ScanIn[3]
A09	MpReadyOut	C16	MpAddrBusIn[5]	F03	DaslData[0]In[2]_P
A10	ScanOut[9]	C17	ProcessorClkIn	F05	DaslData[0]In[1]_P
A11	ScanOut[8]	C18	ScanOut[6]	F07	HssData[4]Out_N
A12	MpDataBusBidi[1]	C19	MpDataBusBidi[5]	F09	HssData[7]Out_P
A13	ScanOut[5]	C20	DaslPLLGndaIn	F12	MpAddrBusIn[6]
A14	MpDataBusBidi[7]	D01	DaslData[1]Out[1]_P	F14	HssData[7]In_P
A15	ScanOut[1]	D03	DaslData[1]Out[0]_N	F16	DaslData[0]Out[6]_P
A16	MpAddrBusIn[3]	D05	DaslData[0]In[0]_P	F18	DaslData[0]Out[4]_P
A17	DebugBusOut[1]	D07	DaslData[0]Out[3]_N	F20	Lssd_A_ClkIn
A18	DaslClockIn_N	D09	SHIDataOut	G01	ScanIn[5]
A19	DaslClockIn_P	D12	HssData[5]In_P	G02	DaslData[1]In[0]_P
B01	MemoryGrantIn[0]	D14	DebugBusOut[10]	G03	DaslData[0]In[2]_N
B03	ScanIn[1]	D16	DebugBusOut[5]	G04	DaslData[0]In[3]_P
B05	DaslData[0]Out[2]_P	D18	MpSelectIn#	G05	DaslData[0]In[1]_N
B07	ScanOut[13]	D20	Osc625ProbeOut_P	G06	HssData[4]Out_P
B09	TestM3In	E01	DaslData[1]Out[1]_N	G08	Reserved
B12	ScanOut[7]	E02	DaslData[1]Out[3]_P	G09	HssData[5]Out_P
B14	HssMtestIn	E03	DaslData[1]Out[3]_N	G10	HssData[5]Out_N
B16	DebugBusOut[0]	E04	DaslData[1]Out[2]_N	G11	HssData[6]In_P
B18	ScanOut[4]	E05	DaslData[1]Out[2]_P	G12	HssData[6]In_N
B20	DaslPLLVddaIn	E06	DaslData[0]In[0]_N	G13	Reserved
C01	InterruptOut#	E07	DebugBusOut[9]	G15	HssData[7]In_N
C02	DaslData[1]Out[0]_P	E08	DebugBusOut[13]	G16	DaslData[0]Out[6]_N
C03	DaslData[0]Out[1]_N	E09	HssData[7]Out_N	G17	DaslData[0]Out[7]_N
C04	DaslData[0]Out[1]_P	E10	DebugBusOut[16]	G18	DaslData[0]Out[4]_N
C05	DebugBusOut[4]	E11	LeakageTestIn	G19	DaslData[1]Out[7]_N
C06	DaslData[0]Out[2]_N	E12	HssData[5]In_N	G20	Lssd_B_ClkIn
C07	DaslData[0]Out[3]_P	E13	DebugBusOut[17]	H01	DaslData[1]In[1]_P
C08	DI2#	E14	DebugBusOut[12]	H03	DaslData[1]In[0]_N

Table 8-3: I/O Signal List Sorted by Pin Location (Continued)

Pin Location	Signal Name	Pin Location	Signal Name	Pin Location	Signal Name
H05	DaslData[0]In[3]_N	L01	ScanIn[9]	N18	DaslData[3]In[6]_P
H07	Spare	L03	MpDataBusBidi[0]	N20	DaslData[3]Out[6]_N
H09	SelectSerialHostIn	L05	FullyInsertedIn#	P01	ScanIn[4]
H12	MpAddrBusIn[4]	L07	TxAvTTIn[0]	P02	DaslData[2]In[3]_N
H14	HssLtestOut	L09	HssData[3]Out_P	P03	DaslData[3]In[2]_P
H16	DaslData[0]Out[7]_P	L12	HssData[0]In_N	P04	DaslData[3]In[1]_N
H18	DaslData[1]Out[7]_P	L14	RxAvRegOut[0]	P05	DaslData[3]In[0]_P
H20	MpAddrBusIn[1]	L16	DaslData[2]In[4]_N	P06	HssData[0]Out_P
J01	ScanIn[6]	L18	DaslData[3]In[4]_N	P08	Reserved
J02	DaslData[1]In[1]_N	L20	ScanOut[0]	P09	HssData[1]Out_P
J03	DaslData[1]In[2]_P	M01	ScanIn[10]	P10	HssData[1]Out_N
J04	DaslData[1]In[2]_N	M02	DaslData[2]In[2]_P	P11	HssData[2]In_P
J05	DaslData[1]In[3]_N	M03	DaslData[2]In[1]_N	P12	HssData[2]In_N
J06	DaslData[1]In[3]_P	M04	DaslData[2]In[1]_P	P13	Reserved
J07	TxAvTTIn[1]	M05	DaslData[2]In[0]_N	P15	HssData[3]In_N
J08	TxAv25In[1]	M06	DaslData[2]In[0]_P	P16	DaslData[2]In[7]_P
J10	HssData[6]Out_N	M07	TxAv25In[0]	P17	DaslData[2]In[6]_N
J11	HssData[4]In_P	M08	TxAvRegOut[0]	P18	DaslData[3]In[7]_P
J13	RxAvRegOut[1]	M10	HssData[3]Out_N	P19	DaslData[3]In[6]_N
J14	RxAv25In[1]	M11	HssData[0]In_P	P20	Lssd_C4_ClkIn
J15	DaslData[1]Out[6]_P	M13	RxAv25In[0]	R01	RI#
J16	DaslData[1]Out[6]_N	M14	RxAvTTIn[0]	R03	DaslData[3]In[2]_N
J17	DaslData[1]Out[4]_P	M15	DaslData[2]In[5]_P	R05	DaslData[3]In[0]_N
J18	DaslData[1]Out[4]_N	M16	DaslData[2]In[5]_N	R07	HssData[0]Out_N
J19	MpAddrBusIn[7]	M17	DaslData[3]In[5]_P	R09	HssData[2]Out_N
J20	Lssd_C1_ClkIn	M18	DaslData[3]In[5]_N	R12	HssData[1]In_N
K01	ScanIn[8]	M19	DaslData[3]Out[6]_P	R14	HssData[3]In_P
K03	MemoryGrantIn[2]	M20	Lssd_C3_ClkIn	R16	DaslData[2]In[7]_N
K05	MpDataBusBidi[6]	N01	DaslData[2]In[2]_N	R18	DaslData[3]In[7]_N
K07	TxAvRegOut[1]	N03	DaslData[2]In[3]_P	R20	ScanIn[12]
K09	HssData[6]Out_P	N05	DaslData[3]In[1]_P	T01	DaslData[2]Out[2]_P
K12	HssData[4]In_N	N07	ACTestOut	T02	DaslData[2]Out[1]_N
K14	RxAvTTIn[1]	N09	MpDataBusBidi[4]	T03	DaslData[2]Out[1]_P
K16	DaslData[2]In[4]_P	N12	PowerOnResetIn#	T04	DaslData[2]Out[0]_N
K18	DaslData[3]In[4]_P	N14	Pad_B_In	T05	DaslData[2]Out[0]_P
K20	IOTestIn	N16	DaslData[2]In[6]_P	T06	DaslData[3]In[3]_P

Table 8-3: I/O Signal List Sorted by Pin Location (Continued)

Pin Location	Signal Name	Pin Location	Signal Name	Pin Location	Signal Name
T07	SHISelectIn#	V01	DebugBusOut[6]	W09	ACTestIn
T08	DebugBusOut[8]	V02	DaslData[2]Out[3]_N	W12	DaslData[0]In[7]_N
T09	HssData[2]Out_P	V03	DaslData[3]Out[2]_N	W14	Pad_A_In
T10	DebugBusOut[14]	V04	DaslData[3]Out[2]_P	W16	DaslData[1]In[7]_N
T11	DebugBusOut[15]	V05	DebugBusOut[11]	W18	ScanIn[13]
T12	HssData[1]In_P	V06	DaslData[3]Out[1]_P	W20	HssPLLVddaIn
T13	Lssd_TestEnableIn	V07	DaslData[3]Out[0]_N	Y02	ScanOut[12]
T14	DebugBusOut[3]	V08	HssLtestIn	Y03	DI1#
T15	DaslData[2]Out[4]_P	V09	MpParityEnableIn#	Y04	DaslData[3]Out[3]_N
T16	DaslData[2]Out[5]_P	V10	MpDataBusBidi[3]	Y05	DaslData[3]Out[3]_P
T17	DaslData[2]Out[5]_N	V11	DaslData[0]In[7]_P	Y06	ScanOut[2]
T18	DaslData[2]Out[7]_P	V12	DaslData[1]In[4]_P	Y07	DaslData[0]In[4]_P
T19	DaslData[2]Out[7]_N	V13	DaslData[1]In[4]_N	Y08	DaslData[0]In[4]_N
T20	DaslData[3]Out[7]_P	V14	DaslData[1]In[6]_N	Y09	DaslData[0]In[5]_P
U01	DaslData[2]Out[2]_N	V15	DaslData[1]In[7]_P	Y10	DaslData[0]In[5]_N
U03	DaslData[2]Out[3]_P	V16	DebugBusOut[2]	Y11	DaslData[0]In[6]_P
U05	DaslData[3]In[3]_N	V17	DaslData[3]Out[4]_P	Y12	DaslData[0]In[6]_N
U07	DaslData[3]Out[0]_P	V18	DaslData[3]Out[4]_N	Y13	DaslData[1]In[5]_P
U09	MpDataBusBidi[2]	V19	DaslData[3]Out[5]_N	Y14	DaslData[1]In[5]_N
U12	DebugBusOut[7]	V20	HssPLLGndaIn	Y15	ScanIn[11]
U14	DaslData[1]In[6]_P	W01	SendGrantOut	Y16	DaslData[2]Out[6]_P
U16	DaslData[2]Out[4]_N	W03	TRST#	Y17	DaslData[2]Out[6]_N
U18	DaslData[3]Out[5]_P	W05	DaslData[3]Out[1]_N	Y18	HssClockIn_N
U20	DaslData[3]Out[7]_N	W07	ScanIn[7]	Y19	HssClockIn_P

9. Electrical Characteristics

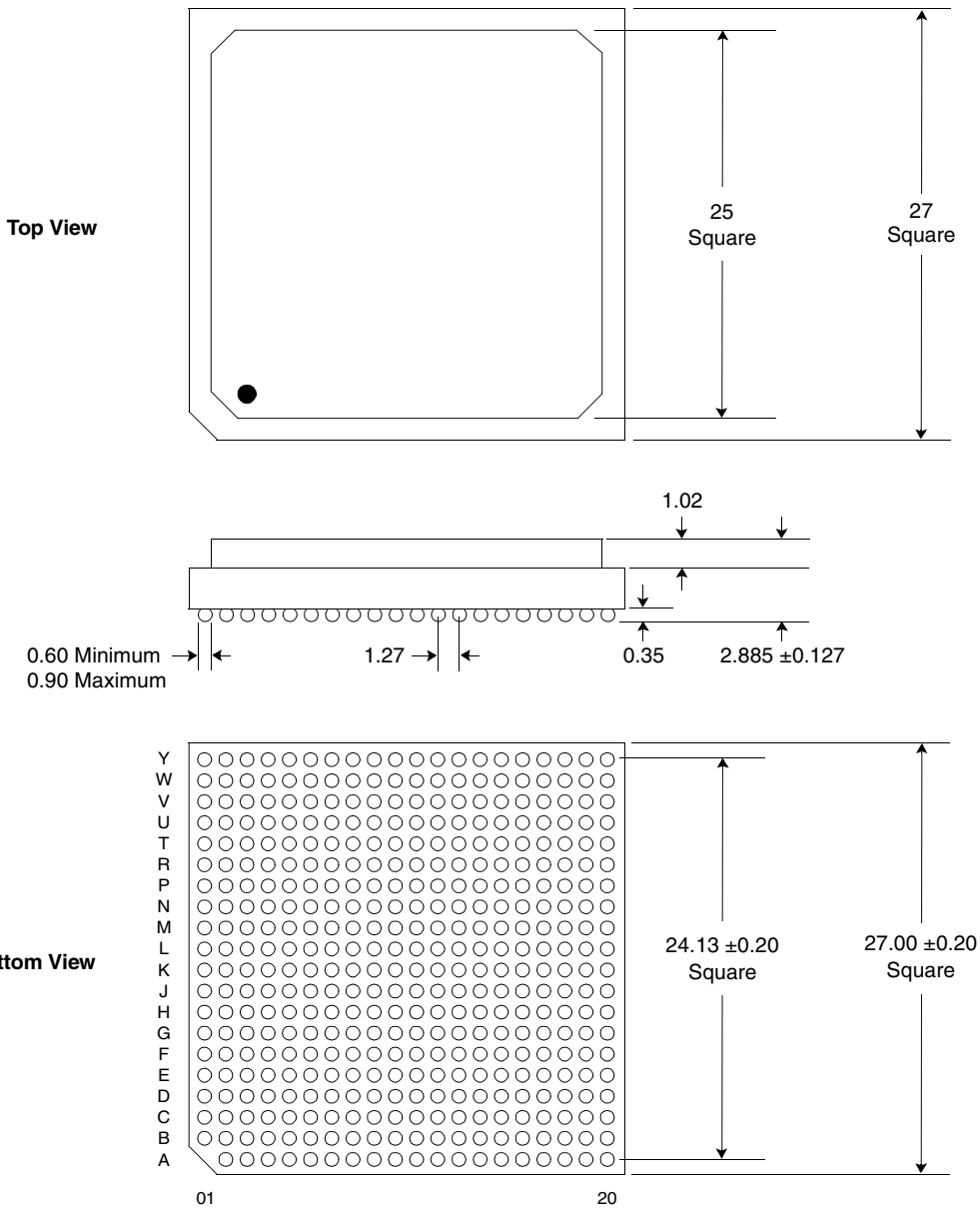
Table 9-1. Recommended Operating Conditions

Symbol	Parameter	Rating			Units
		Minimum	Typical	Maximum	
P_{Max}	Power (activity factor = ~0.1)	3.8	4.5	5.2	W
V_{DD} (1.8 V)	Power supply voltage	1.65	1.8	1.95	V
V_{DD} (2.5 V)		2.3	2.5	2.7	V
V_{IH}	Input up level (HSTL); $V_{REF} = V_{DD} \div 2$	V_{REF} + 0.1		V_{DD} + 0.3	V
V_{IL}	Input down level (HSTL); $V_{REF} = V_{DD} \div 2$	-0.3		V_{REF} - 0.1	V
V_{OH}	High-level output voltage (I_{OH} = -8 mA)	V_{DD} - 0.4			V
V_{OL}	Low-level output voltage (I_{OL} = 8 mA)			0.4	V
V_{CM}	PECL receiver common-mode voltage-level range (or voltage crosspoint)	0.55		2.35	V
V_{IS}	PECL receiver input differential voltage swing minimum	0.25			V
I_{DD} (1.8 V)	Power supply current	2.0	2.3	2.7	A
I_{DD} (2.5 V)		95	110	125	mA
T_J	Operating junction temperature	0		125	°C
T_S	Storage temperature	-65		150	°C

Note: Permanent device damage may occur if the maximum ratings are exceeded. Extended exposure to maximum rating conditions may affect device reliability.

10. Mechanical Information

Figure 10-1. Package Mechanical



Package type is 399-ball HyperBGA, package size is 27 × 27 mm, and array size is 20 × 20. All dimensions are in millimeters.

11. 8b/10b Codes

Table 11-1. 8b/10b Codes (Page 1 of 5)

Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001

Table 11-1. 8b/10b Codes (Page 2 of 5)

Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100

Table 11-1. 8b/10b Codes (Page 3 of 5)

Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010

Table 11-1. 8b/10b Codes (Page 4 of 5)

Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110

Table 11-1. 8b/10b Codes (Page 5 of 5)

Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD-abcdei fghj	Current RD+abcdei fghj
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 11-2. Special Codes

Special Code Name	Tn(7:0)	Current RD-abcdei fghj	Current RD+abcdei fghj	Special Code Name	Tn(7:0)	Current RD-abcdei fghj	Current RD+abcdei fghj
K28.0	000 11100	001111 0100	110000 1011	K28.6	110 11100	001111 0110	110000 1001
K28.1	001 11100	001111 1001	110000 0110	K28.7	111 11100	001111 1000	110000 0111
K28.2	010 11100	001111 0101	110000 1010	K23.7	111 10111	111010 1000	000101 0111
K28.3	011 11100	001111 0011	110000 1100	K27.7	111 11011	110110 1000	001001 0111
K28.4	100 11100	001111 0010	110000 1101	K29.7	111 11101	101110 1000	010001 0111
K28.5	101 11100	001111 1010	110000 0101	K30.7	111 11110	011110 1000	100001 0111

12. Glossary

8b/10b A coding scheme that converts every byte (8 bits) of data into 10 bits to improve transmission characteristics and clock recovery and reduce transmission errors. The PowerPRS SCIC HSS interface uses this coding scheme.

absolute maximum rating The highest value a quantity can have before malfunction or damage occurs.

ac alternating current

address A number designating a particular data location.

APA adaptor port available

array An ordered arrangement of data elements.

ASIC application-specific integrated circuit

ATM asynchronous transfer mode

b bit

B byte

bandwidth The transmission capacity (speed) of a data link or bus.

best-effort delivery The delivery of packets with no bandwidth guarantee and an unspecified quality of service. Packets can be discarded during traffic congestion.

bidirectional The ability to transmit in both directions.

BIST built-in self-test

bitmap A binary representation in which a bit or set of bits in the packet header corresponds to a packet routing switch output port or group of ports (destination). For example, a ‘1’ in the bitmap field indicates that the following data is destined for the corresponding PowerPRS 64G output port.

boundary scan A test methodology used to verify input/output hardware drivers and their interconnections on a printed circuit board.

buffer A memory bank used for temporary data storage.

bus A common pathway over which input and output signals are routed.

clock A signal that provides a continuous, steady, periodic, two-state waveform.

clock cycle One “tick” of the clock. For example, a 100-MHz clock has 100 million ticks per second.

clock frequency The reciprocal of the time period of a single clock cycle.

CMOS complementary metal-oxide semiconductor

configuration	The arrangement of speed expansion, port expansion, and port-paralleling options that create a custom switching device, or the act of programming a device register for a desired state of readiness.
control packet	Packets that carry the communications between the switch local processor and the protocol engine. A control packet bitmap is set to all zeros. The PowerPRS SCIC regards control packets as data packets.
counter	A circuit that counts pulses and generates an output at a specified time.
CPU	central processing unit
CRC	cyclic redundancy check. A code used to validate a block of data. The PowerPRS SCIC features CRC calculation and verification on the DASL interface.
CSIX	common switch interface. A physical interface for transferring data between the protocol engine (network processor) and the switch fabric.
DASL	data-aligned synchronous link. The physical link that performs nibble-to-serial serialization and serial-to-nibble deserialization in addition to bit, byte, and packet alignment. The PowerPRS SCIC DASL interface transfers data to and from the PowerPRS 64G.
data packet	The user data element that the PowerPRS SCIC processes in four equal lengths (see “LU”). The value of the packet qualifier byte protection field is either ‘01’, ‘10’, or ‘11’. Data packets are prioritized from zero to three, with zero being the highest priority (see “packet priority”). Data packets are inserted and extracted outside the switch fabric.
dc	direct current
DFF	data flip-flop
differential pair	Two wires of opposite polarity configured as a pair to reduce signal noise and crosstalk.
driver	Also called a “device driver.” A routine that links a peripheral device to the operating system and performs internal functions, or a functional unit that increases the output current, power, or voltage of another functional unit.
egress flow	Data flow from the switch core to the attached devices; corresponds to data transmitted by the switch.
Fibre Channel Standard	A standard definition for the high-speed data transfer interface used to build storage area networks as well as general-purpose networks such as those used in PowerPRS applications.
filter	A pattern or mask through which only selected data is passed (for example, finite impulse response filter).
FIR	finite impulse response
FPA	(switch) fabric port available

frame	A stream of packaged data that is a multiple of packet length divided by four (equal to LU length). For example, if two priorities are in use on the back-pressure bus, then the frame length of the framing signal is equal to either two LUs or two data packets (where the packet length is expressed in words [4 bytes or 32 bits].
FSM	finite state machine
Gbps	gigabits per second
HSS	high-speed serializer/deserializer. The HSS interface provides point-to-point data transmission (2.125 to 2.6 Gbps) over media with a characteristic impedance of approximately 50 Ω. Each HSS is comprised of two differential pairs; one differential pair carries ingress flow and the other carries egress flow. The PowerPRS SCIC HSS interface transfers data to and from the PowerPRS C192.
HSTL	high-speed transceiver logic
HyperBGA	IBM's organic laminate flip-chip attach, ball grid array chip package that enables complex high-performance devices.
I/O	input/output
idle packet	The packet transmitted to maintain the integrity (synchronization) of the bus when the other packet types are either unavailable for transmission or prevented from transmission due to a flow control situation. Idle packets carry SCC bytes in the sixth byte position.
IEEE	Institute of Electrical and Electronics Engineers
ingress flow	Data flow from the attached device to the switch core; corresponds to data received by the switch.
interrupt	A signal that gains the attention of the CPU and is usually generated when input or output is required.
jitter	A flicker or fluctuation in a transmission signal caused by a bit arriving either ahead or behind the standard clock cycle or, more generally, the variable arrival of packets.
JTAG	Joint Test Action Group. IEEE Standard 1149.1 (regarding boundary-scan architecture) is also referred to as the JTAG standard, after the group that developed it.
junction	The region of contact between opposite types of semiconductor materials.
K character	An 8b/10b code control character used for link synchronization and supervision.
line	An electronic communications channel such as a wire.

local processor The external microprocessor connected to the PowerPRS SCIC through either the serial host interface or the parallel processor interface and used to control device configuration.

loopback The path used to wrap an outgoing data stream back to the input (receive) side for testing purposes.

LSB least significant bit

LSSD level-sensitive scan design

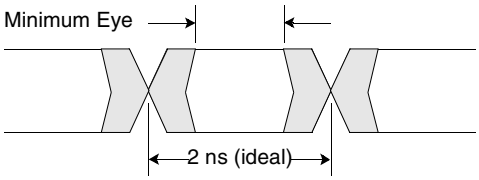
LU logical unit. An equal length (8 to 10 bytes) of data processed by a single shared memory within the PowerPRS 64G. The PowerPRS SCIC processes 16- to 20-byte LUs that correspond to 64- to 80-byte packets.

LVCMOS low-voltage complementary metal-oxide semiconductor

mask A bit pattern used to change (reject) or extract (accept) bit positions in another bit pattern. For example, when the Boolean AND operation is used to match a mask of ‘0’s and ‘1’s with a string of data bits and a ‘1’ occurs in both the mask and the data, the resulting bit will contain a ‘1’ in that position. Hardware interrupts are enabled and disabled in this manner, with each interrupt assigned a bit position in the *Interrupt Mask Register* (page 59).

Mbps megabits per second

minimum eye The part of the DASL receiver error-detection function used to detect bit synchronization errors caused by excessive transient noise (that is, electro-static discharge). These errors are characterized by eye closures detected by an edge-sampling circuit. An error exists when an edge is detected within the minimum-eye region of the data sample.



MISR multiple-input signature register

mode An operational state of at least two possible conditions to which a system can be switched.

MPRA multiport register array

MSB most significant bit

multiplexer A device that merges several low-speed transmissions into one high-speed transmission and vice versa (demultiplexer).

network processor A programmable CPU chip optimized to perform the packet processing supported by the PowerPRS 64G.

NP4GS3	The IBM-approved product nickname for the PowerNP NP4GS3 Network Processor.
OC-48	The synchronous optical network (SONET) transmission rate of 2488.32 Mbps.
OC-192	The SONET transmission rate of 9953.28 Mbps.
off-chip driver	An input/output logic cell that provides a buffered interface between internal and external device signals.
OQG	output queue grant
packet	See “data packet.”
packet header	The first two to five bytes in a packet that contain destination bitmap, packet priority, and switch redundancy support information, all protected by a parity bit.
packet priority	Four levels of data packet priority provide quality-of-service support. Data packets are prioritized from zero to three, with zero being the highest priority.
packet qualifier byte	The first byte (H0) of a PowerPRS 64G packet header. This byte contains important information about the packet, such as packet type, packet priority, and so forth.
Packet Routing Switch Serial Interface Converter	An IBM product that performs Utopia-3-like parallel interface to PowerPRS 64G DASL interface conversion.
parity	The number of bits (or the number of similar bits) that are even or odd, as intended.
payload	The part of the packet that carries the message data (contrast with packet header).
PECL	pseudoemitter-coupled logic
pin	An external connection facility that enables device attachment to a higher level of assembly.
pinout	A diagram of the integrated circuit that shows the locations of the pins for various functions.
PLL	phase-locked loop
port paralleling	An optional PowerPRS 64G configuration for reducing the number of device ports. Four ports are grouped to form one link, up to a maximum of eight links (or groups).
PowerPRS 64G	The IBM-approved product nickname for the PowerPRS 64G Packet Routing Switch.
PowerPRS C192	The IBM-approved product nickname for the PowerPRS C192 Common Switch Interface.

PowerPRS Q-64G	The IBM-approved product nickname for the PowerPRS Q-64G Packet Routing Switch.
PowerPRS SCIC	The IBM-approved product nickname for the PowerPRS SCIC Switch Core Interface Chip (SCIC).
protocol engine	The device, such as the protocol processor, network processor, traffic manager, ATM layer, and so forth, attached to the network side of the PowerPRS C192 that runs the higher layer protocols.
PRPG	pseudorandom pattern generator
pulldown	A resistor that lowers the pin voltage.
pullup	A resistor that raises the pin voltage.
pulse	A transient signal of short duration, constant amplitude, and one polarity.
quality of service	The network performance level.
queue	A temporary holding place for egress data.
RAM	random access memory
read/clear	A register field in which the value is cleared immediately after a read.
receiver	An electronic device that accepts signals, and processes or converts them for internal use.
register	A small, high-speed circuit that stores internal operation values, such as the address of the instruction being executed and the data being processed.
resistor	An electronic component that resists the flow of current in a device.
RLOS	receiver loss of signal
routing index	A packet header field used to route an egress packet (Cframe) on the PowerPRS C192 CSIX interface to its proper destination. The routing index field is ignored by PowerPRS devices.
RX	Abbreviation for “receive.”
SCC	side communication channel. The four-bit SCC field carries communications between the PowerPRS C192 and the PowerPRS 64G. SCC bits are equivalent to sampled hardware lines between the two devices. SCC information is transferred in band in the idle packet master LU (byte 6, bits 0:3 and 4:7) in two redundant nibbles.
SDC	shared DASL controller
service packet	Also referred to as a “yellow packet.” The PowerPRS SCIC transfers three types of service packets between the PowerPRS 64G and the PowerPRS C192: *event-1 service packets* to test link liveness, *event-2 service packets* to communicate events, and *command service packets* to request actions.

SHI	serial host interface
skew	A timing change in a transmission signal.
SRAM	static random access memory
SRL	set/reset latch
stream	A contiguous flow of bits, bytes, or data from one place to another.
subport	One half the logical bandwidth of each DASL port on the PowerPRS SCIC DASL interface.
switch core access layer	Open System Interconnection (OSI) layer 2, data link. This layer validates the integrity of the transmission. Transmitted bits are divided into frames (or packets).
switch fabric	The PowerPRS 64G internal interconnect architecture that redirects the ingress and egress data flow.
switchover	The process of redirecting the data flow between redundant switch planes.
sync	Abbreviation for “synchronization.”
synchronization packet	The packet that provides the bit transition and packet delineation necessary for DASL synchronization.
throughput	The amount of data processed through a device in a given time period. Device throughput is usually less than the aggregate port speed due to packet header, routing, and data integrity information (overhead).
traffic	Data crossing the network.
trailer	The last byte of each LU.
transceiver	A bidirectional input/output off-chip driver.
transmitter	An electronic device that generates signals.
TX	Abbreviation for “transmit.”
Utopia-3-like	An interface similar to the universal test and operations physical layer interface used in ATM network technology.
VCO	voltage-controlled oscillator
yellow packet	See “service packet.”

13. Related Documents

ASIC SA-27E Databook, Part I: Base Library and I/Os, IBM Corporation, January 2002 (contact your IBM representative for access to this document).

ASIC SA-27E Databook, Part II: Macros, IBM Corporation, January 2002 (contact your IBM representative for access to this document).

High-Speed Transceiver Logic (HSTL): A 1.5-V Output Buffer Supply Voltage-Based Interface Standard for Digital Integrated Circuits, Electronic Industries Association/JEDEC Standard No. 8-6, August 1995.

IBM Packet Routing Switch PRS64G Datasheet, IBM Corporation, July 2001 (see http://www-3.ibm.com/chips/techlib/techlib.nsf/products/Packet_Routing_Switch_PRS64G).

IBM Packet Routing Switch Serial Interface Converter Datasheet, Preliminary, IBM Corporation, January 2002 (see http://www-3.ibm.com/chips/techlib/techlib.nsf/products/Packet_Routing_Switch_Serial_Interface_Converter).

IBM PowerNP NP4GS3 Network Processor Datasheet, Preliminary, IBM Corporation, February 2002 (see http://www-3.ibm.com/chips/techlib/techlib.nsf/products/IBM_PowerNP_NP4GS3).

IBM PowerPRS C192 Common Switch Interface Summary Datasheet, Preliminary, IBM Corporation, September 2001 (see http://www-3.ibm.com/chips/techlib/techlib.nsf/products/PowerPRS_C192_Common_Switch_Interface).

IBM PowerPRS Q-64G Packet Routing Switch, Preliminary, IBM Corporation, December 2001 (see http://www-3.ibm.com/chips/techlib/techlib.nsf/products/PowerPRS_Q-64G_Packet_Routing_Switch).

IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE Standard 1596.3-1996, IEEE Standards Association, 1996.

IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Standard 1149.1-1990, IEEE Standards Association, 1990.

InfiniBand Architecture Specification, Volume 2: Physical Specifications, Release 1.0.a, InfiniBand Trade Association, June 2001 (see http://www.infinibandta.org/specs).

Revision Log

Revision Date	Contents of Modification
May 6, 2002	Initial release (00).