HARRIS SEMICONDUCTOR

HCS195MS

Radiation Hardened Inverting 8-Bit Parallel-Input/Serial Output Shift Register

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

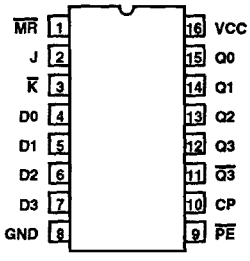
The Harris HCS195MS is a Radiation Hardened 8-Bit Parallel-In/Serial-Out Shift Register with complementary serial outputs and an asynchronous parallel load input.

The HCS195MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

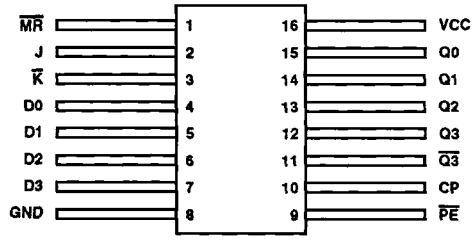
The HCS195MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

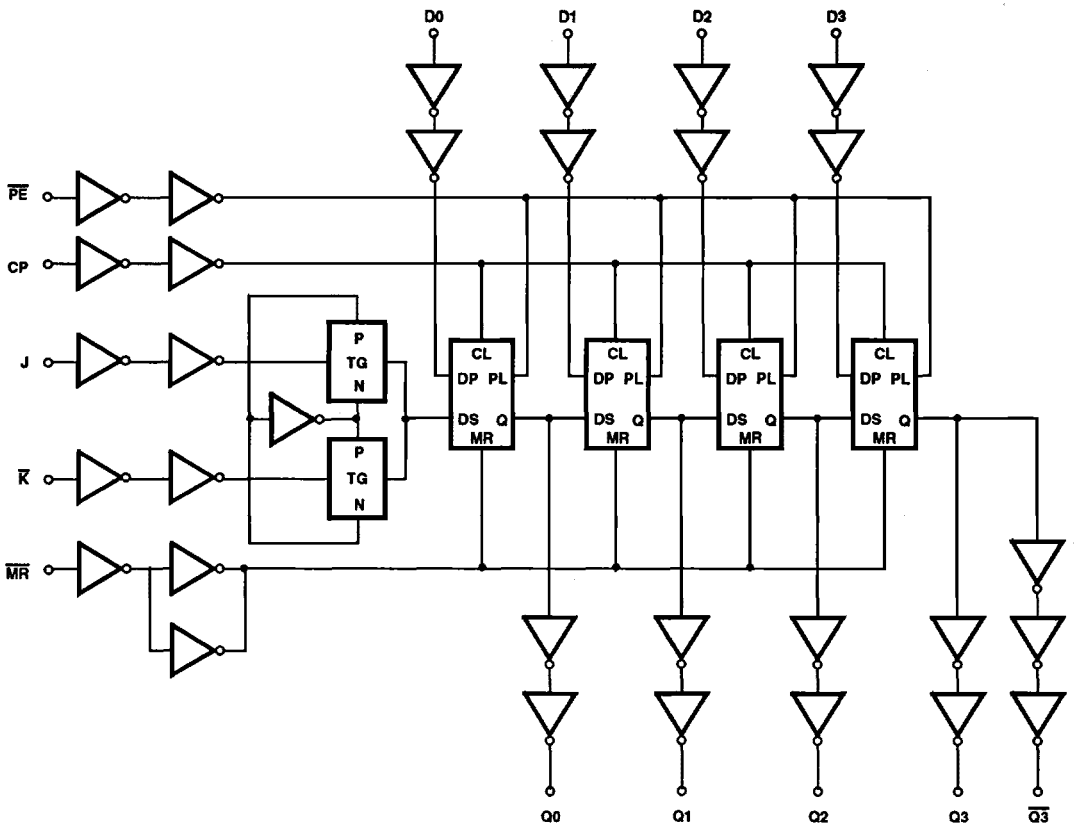
INPUTS						OUTPUTS				
$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q0	Q1	Q2	Q3	$\overline{Q3}$
L	X	X	X	X	X	L	L	L	L	H
H	⎍	h	h	h	X	H	q0	ql	q2	q3
H	⎍	h	l	l	X	L	q0	ql	q2	q3
H	⎍	h	h	l	X	$\overline{q0}$	q0	ql	q2	q3
H	⎍	h	l	h	X	q0	q0	ql	q2	q3
H	⎍	l	X	X	dn	d0	dl	d2	d3	$\overline{d3}$

Dn or Qn = referenced input (or output) one set-up time prior to clock
l or h = level one set-up time prior to clock
⎍ = positive clock

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3385

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1
(All voltage reference to VSS)

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 10ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to 30% of VCC
Input High Voltage (VIH) ..... VCC to 70% of VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. Force/measure functions may be interchanged.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (CP - Qn)	TPHL1	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
Propagation Delay (CP - Qn)	TPLH1	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	42	ns
Propagation Delay (MR - Q0-3)	TPHL2	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
Propagation Delay (MR - $\overline{Q3}$)	TPLH2	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	Typical 60		pF
			1	+125°C	Typical 80		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	20	pF
			1	+125°C	-	20	pF
Pulse Width Time (CP or MR)	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Setup Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	20	-	ns
			1	+125°C	20	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
MR to CP Removal Time	TREM	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Recovery Time $\overline{PL}$ to CP	TREC	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	20	-	ns
			1	+125°C	30	-	ns
Maximum Clock Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	30	-	MHz
			1	+125°C	20	-	MHz
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	1	15	ns
			1	+125°C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay (CP - Qn)	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	37	2	46.3	ns
Propagation Delay (CP - Qn)	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	42	2	52.5	ns
Propagation Delay (MR - Q0-3)	TPHL2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	39	2	48.8	ns
Propagation Delay (MR - $\overline{Q3}$)	TPLH2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	39	2	48.8	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1,9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 10, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8, 9	1 - 3, 16	11 - 15	10	4 - 7

NOTES:

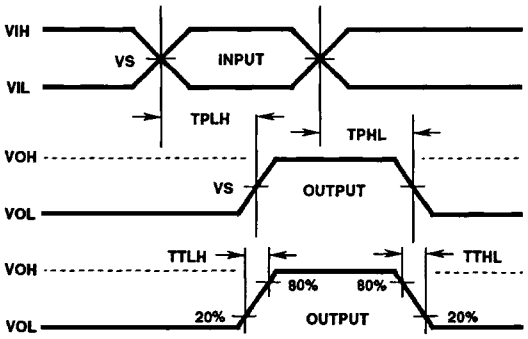
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

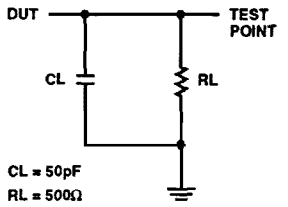
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit

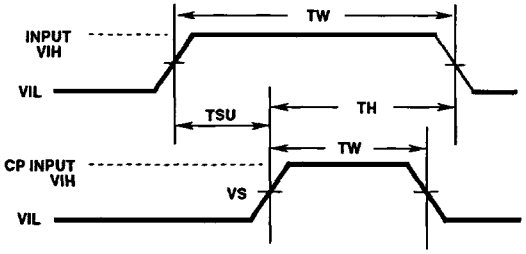




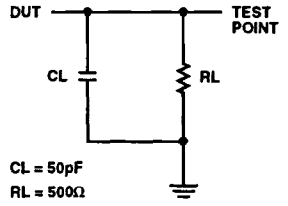
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



TH = Hold Time
TSU = Setup Time
TW = Pulse Width



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
95 x 94 mils
2.380 x 2.410mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout