VITELIC

# V53C866 FAMILY
# HIGH PERFORMANCE, LOW POWER
# 64K X 8 BIT STATIC COLUMN
# CMOS DYNAMIC RAM

| HIGH PERFORMANCE V53C866 | 70/70L | 80/80L | 10/10L | 12/12L |
|---|---|---|---|---|
| Max. $\overline{RAS}$ Access Time, ($t_{RAC}$) | 70 ns | 80 ns | 100 ns | 120 ns |
| Max. Column Address Access Time, ($t_{CAA}$) | 35 ns | 40 ns | 45 ns | 55 ns |
| Min. Static Column Cycle Time, ($t_{SWC}$, $t_{SRC}$) | 45 ns | 50 ns | 55 ns | 60 ns |
| Min. Read/Write Cycle Time, ($t_{RC}$) | 130 ns | 145 ns | 175 ns | 205 ns |

| LOW POWER V53C866L | 70L | 80L | 10L | 12L |
|---|---|---|---|---|
| Max. CMOS Standby Current, ($I_{DD6}$) | 1.0 mA | 1.0 mA | 1.0 mA | 1.0 mA |

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## Features

- Low power dissipation for V53C866-12
  - Operating Current—60 mA max.
  - TTL Standby Current—3.5 mA max.
- Low CMOS Standby Current
  - V53C866—3.0 mA max.
  - V53C866L—1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Static Column Mode operation for a sustained data rate greater than 22 MHz
- 256 Refresh cycles/4 ms
- Standard packages are 24 pin Plastic DIP and 24/26 pin SOJ.

## Description

The Vitelic V53C866 is a high speed 65,536 x 8 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS III technology, the V53C866 offers a combination of size and features unattainable with NMOS technology: Static Column decode for high data bandwidth and clock-free page operation, fast usable speed, CMOS standby current, inherently high CMOS reliability, and upon request, extended refresh for very low data retention power (V53C866L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Static Column operation allows random access of up to 256 (x8) bits within a row with cycle times as short as 45 ns. Because of static circuitry, $\overline{CAS}$ is not required either to clock or gate column addresses. Because $\overline{CAS}$ is not in the critical access time path, system design is easier, and inherent device speed is more usable. These unique features make the V53C866 ideally suited for computer peripherals, control systems and graphic systems.

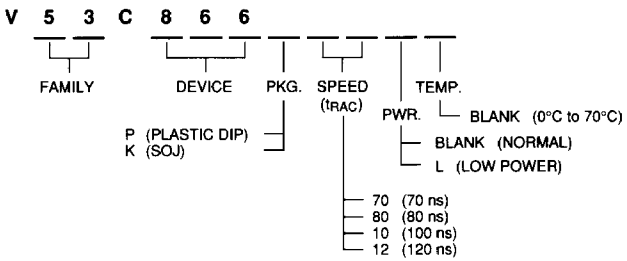
The V53C866L-12 offers a maximum data retention power of 5.5 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. For selected V53C866L devices with Refresh Interval longer than 4 ms, consult the factory.

## Device Usage Chart

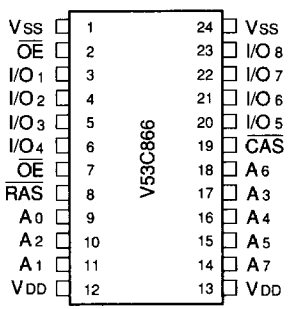
| Operating Temperature Range | Package Outline | | Access Time (ns) | | | | Power | | Temperature Mark |
|---|---|---|---|---|---|---|---|---|---|
| | P | K | 70 | 80 | 100 | 120 | Low | Std. | |
| 0°C to 70°C | • | • | • | • | • | • | • | • | Blank |

V53C866 Rev. 02 June 1990

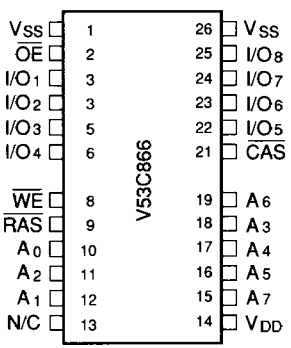
| Description | Pkg. | Pin Count |
|---|---|---|
| Plastic DIP | P | 24 |
| SOJ | K | 26/24 |




### 24 Lead Plastic DIP PIN CONFIGURATION Top View




### 26/24 Lead SOJ PIN CONFIGURATION Top View




### Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any Pin Except $V_{DD}$
Relative to $V_{SS}$ ..... −1.0 V to +7.0 V
Voltage on $V_{DD}$ relative to $V_{SS}$ ..... −1.0 V to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

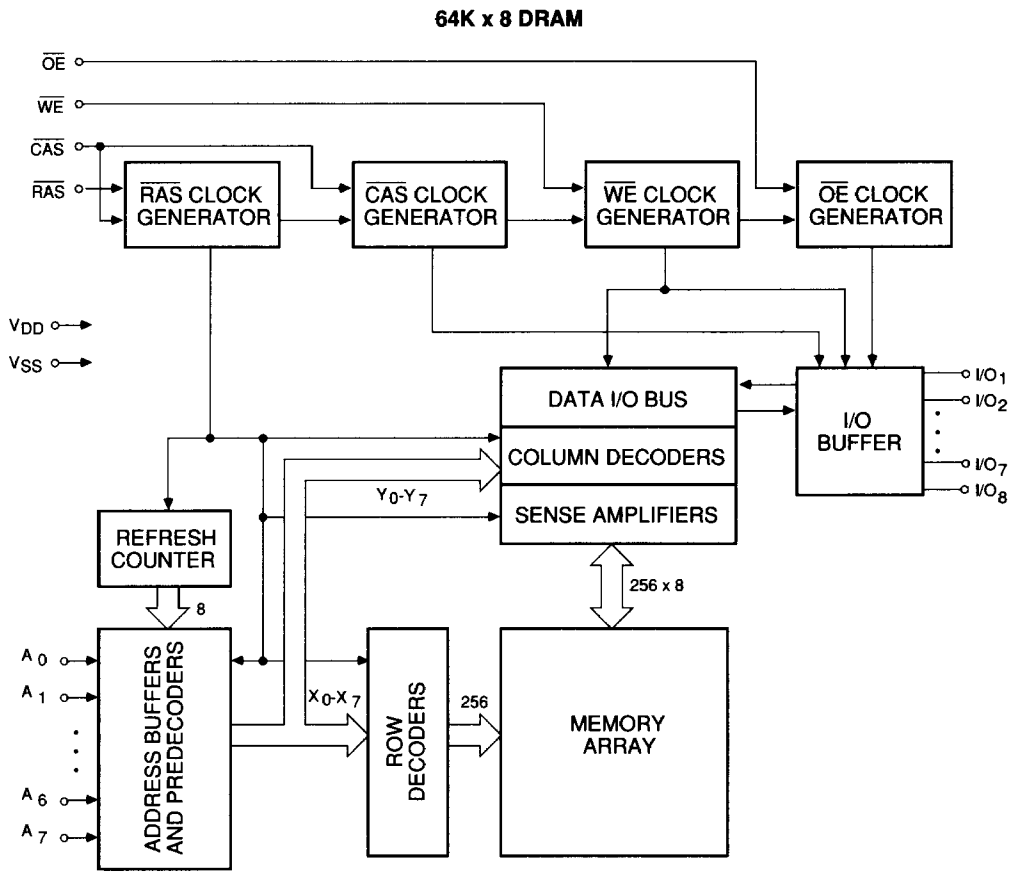
### Capacitance*

$T_A$ = 25°C, $V_{DD}$ = 5 V ±10%, $V_{SS}$ = 0 V

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN1}$ | Address Input | 3 | 4 | pF |
| $C_{IN2}$ | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | 4 | 5 | pF |
| $C_{OUT}$ | I/O | 5 | 7 | pF |

*Note: Capacitance is sampled and not 100% tested

## Block Diagram



## DC and Operating Characteristics (1-2)

$T_A$ = 0°C to 70°C, $V_{DD}$ = 5 V ±10%, $V_{SS}$ = 0 V, unless otherwise specified.

| Symbol | Parameter | Access Time | V53C866 | | V53C866L | | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | | |
| $I_{LI}$ | Input Leakage Current (any input pin) | | −10 | 10 | −10 | 10 | µA | $V_{SS} \le V_{IN} \le V_{DD}$ | |
| $I_{LO}$ | Output Leakage Current (for High-Z State) | | −10 | 10 | −10 | 10 | µA | $V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ | |
| $I_{DD1}$ | $V_{DD}$ Supply Current, Operating | 70 | | 85 | | 85 | mA | $t_{RC} = t_{RC}$ (min.) | 1,2 |
| | | 80 | | 75 | | 75 | | | |
| | | 100 | | 65 | | 65 | | | |
| | | 120 | | 60 | | 60 | | | |
| $I_{DD2}$ | $V_{DD}$ Supply Current, TTL Standby | | | 3.5 | | 2.0 | mA | $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ other inputs ≥ $V_{SS}$ | |
| $I_{DD3}$ | $V_{DD}$ Supply Current, $\overline{RAS}$-Only Refresh | 70 | | 85 | | 85 | mA | $t_{RC} = t_{RC}$ (min.) | 2 |
| | | 80 | | 75 | | 75 | | | |
| | | 100 | | 65 | | 65 | | | |
| | | 120 | | 60 | | 60 | | | |
| $I_{DD4}$ | $V_{DD}$ Supply Current, Static Column Mode Operation | 70 | | 60 | | 60 | mA | Minimum Cycle | 1,2 |
| | | 80 | | 55 | | 55 | | | |
| | | 100 | | 50 | | 50 | | | |
| | | 120 | | 45 | | 45 | | | |
| $I_{DD5}$ | $V_{DD}$ Supply Current, Standby, Output Enabled | | | 4 | | 2.5 | mA | $\overline{RAS}$=$V_{IH}$, $\overline{CAS}$=$V_{IL}$ other inputs ≥ $V_{SS}$ | 1 |
| $I_{DD6}$ | $V_{DD}$ Supply Current, CMOS Standby | | | 3 | | 1.0 | mA | $\overline{RAS} \ge V_{DD}$ −0.2 V, $\overline{CAS}$ at $V_{IH}$, other inputs ≥ $V_{SS}$ | |
| $V_{IL}$ | Input Low Voltage | | −1 | 0.8 | −1 | 0.8 | V | | 3 |
| $V_{IH}$ | Input High Voltage | | 2.4 | $V_{DD}$ +1 | 2.4 | $V_{DD}$ +1 | V | | 3 |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | | 0.4 | V | $I_{OL}$ = 4.2 mA | |
| $V_{OH}$ | Output High Voltage | | 2.4 | | 2.4 | | V | $I_{OH}$ = −5 mA | |

## AC Characteristics

$T_A$ = 0°C to 70°C, $V_{DD}$ = 5 V ±10%, $V_{SS}$ = 0 V, unless otherwise noted
AC Test conditions, input pulse levels 0 to 3 V

| # | JEDEC Symbol | Symbol | Parameter | 70/70L | | 80/80L | | 10/10L | | 12/12L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 1 | $t_{RL1RH1}$ | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 70 | 75K | 80 | 75K | 100 | 75K | 120 | 75K | ns | |
| 2 | $t_{RL2RL2}$ | $t_{RC}$ | Read or Write Cycle Time | 130 | | 145 | | 175 | | 205 | | ns | |
| 3 | $t_{RH2RL2}$ | $t_{RP}$ | $\overline{RAS}$ Precharge Time | 50 | | 55 | | 65 | | 75 | | ns | |
| 4 | $t_{RL1CH1}$ | $t_{CSH}$ | $\overline{CAS}$ Hold Time | 70 | | 80 | | 100 | | 120 | | ns | |
| 5 | $t_{CL1CH1}$ | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 25 | | 30 | | 35 | | 40 | | ns | |
| 6 | $t_{RL1CL1}$ | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay | 25 | 45 | 25 | 50 | 25 | 65 | 30 | 80 | ns | 4 |
| 7 | $t_{WH2CL2}$ | $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 8 | $t_{AVRL2}$ | $t_{ASR}$ | Row Address Setup Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 9 | $t_{RL1AX}$ | $t_{RAH}$ | Row Address Hold Time | 15 | | 15 | | 15 | | 20 | | ns | |
| 10 | $t_{CH2QZ}$ | $t_{HZ}$ | $\overline{OE}$ or $\overline{CAS}$ to High-Z Dout | 0 | 15 | 0 | 20 | 0 | 25 | 0 | 30 | ns | 5, 6 |
| 11 | $t_{CL2QZ}$ | $t_{LZ}$ | $\overline{OE}$ or $\overline{CAS}$ to Low-Z Dout | 0 | | 0 | | 0 | | 0 | | ns | 5, 6 |
| 12 | $t_{RL1QV}$ | $t_{RAC}$ | Access Time from $\overline{RAS}$ | | 70 | | 80 | | 100 | | 120 | ns | 7,8,9 |
| 13 | $t_{CL1QV}$ | $t_{CAC}$ | Access Time from $\overline{CAS}$ | | 25 | | 30 | | 35 | | 40 | ns | 9 |
| 14 | $t_{GL1QV}$ | $t_{OAC}$ | Access Time from $\overline{OE}$ | | 15 | | 20 | | 25 | | 30 | ns | 9 |
| 15 | $t_{AVQV}$ | $t_{CAA}$ | Access Time from Column Address | | 35 | | 40 | | 45 | | 55 | ns | 9,10,16 |
| 16 | $t_{CL1RH1(R)}$ | $t_{RSH(R)}$ | $\overline{RAS}$ Hold Time (Read Cycle) | 25 | | 30 | | 35 | | 40 | | ns | |
| 17 | $t_{WH2CL2}$ | $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 18 | $t_{AVRH1}$ | $t_{CAR}$ | Column Address to $\overline{RAS}$ Setup Time | 35 | | 40 | | 45 | | 55 | | ns | |
| 19 | $t_{RL1AX}$ | $t_{ARR}$ | Column Address Hold Time from $\overline{RAS}$ (Read) | 70 | | 80 | | 100 | | 120 | | ns | |
| 20 | $t_{CH2WX}$ | $t_{RCH}$ | Read Command Hold Time Referenced to $\overline{CAS}$ | 5 | | 5 | | 5 | | 5 | | ns | 11 |

## AC Characteristics (Cont'd.)

| # | JEDEC Symbol | Symbol | Parameter | 70/70L | | 80/80L | | 10/10L | | 12/12L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 21 | $t_{RH2WX}$ | $t_{RRH}$ | Read Command Hold Time Referenced to $\overline{RAS}$ | 5 | | 5 | | 5 | | 5 | | ns | 11 |
| 22 | $t_{RH2AX}$ | $t_{ARH}$ | Column Address Hold Time from $\overline{RAS}$ | 5 | | 5 | | 5 | | 5 | | ns | |
| 23 | $t_{RL1AV}$ | $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 20 | 35 | 20 | 40 | 20 | 55 | 25 | 65 | ns | 12 |
| 24 | $t_{AXQX}$ | $t_{OHA}$ | Output Hold Time from Address Change | 0 | | 0 | | 0 | | 0 | | ns | |
| 25 | $t_{GH2QX}$ | $t_{OH}$ | Data Hold Time from $\overline{OE}$ from $\overline{CAS}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| 26 | $t_{CL1RH1(W)}$ | $t_{RSH(W)}$ | $\overline{RAS}$ Hold Time (Write) | 25 | | 30 | | 35 | | 40 | | ns | |
| 27 | $t_{RL1WL1}$ | $t_{WDR}$ | $\overline{RAS}$ to Write Command Lead Time | | 40 | | 45 | | 60 | | 75 | ns | |
| 28 | $t_{WL1RH1}$ | $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 25 | | 30 | | 35 | | 40 | | ns | |
| 29 | $t_{WL1CH1}$ | $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 25 | | 30 | | 35 | | 40 | | ns | |
| 30 | $t_{WL1WH1}$ | $t_{WP}$ | Write Pulse Width | 15 | | 15 | | 20 | | 25 | | ns | |
| 31 | $t_{WH2WL2}$ | $t_{WCP}$ | Write Command Precharge Time | 15 | | 15 | | 20 | | 25 | | ns | |
| 32 | $t_{WL1CL2}$ | $t_{WCS}$ | Write Command Setup Time | 0 | | 0 | | 0 | | 0 | | ns | 13,14 |
| 33 | $t_{CL1WH1}$ | $t_{WCH}$ | Write Command Hold Time | 15 | | 15 | | 20 | | 25 | | ns | |
| 34 | $t_{RL1WH1}$ | $t_{WCR}$ | Write Command Hold Time from $\overline{RAS}$ | 55 | | 60 | | 70 | | 80 | | ns | |
| 35 | $t_{AVWL2}$ | $t_{AWS}$ | Column Address to Write Command Setup Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 36 | $t_{WL1AX}$ | $t_{AWH}$ | Column Address to Write Command Hold Time | 15 | | 15 | | 20 | | 25 | | ns | |
| 37 | $t_{RL1AX}$ | $t_{ARW}$ | Column Address Hold Time from $\overline{RAS}$ (Write) | 55 | | 60 | | 70 | | 80 | | ns | |

## AC Characteristics (Cont'd.)

| # | JEDEC Symbol | Symbol | Parameter | 70/70L | | 80/80L | | 10/10L | | 12/12L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 38 | $t_{DVWL2}$ | $t_{DS}$ | Data In Setup Time | 0 | | 0 | | 0 | | 0 | | ns | 15 |
| 39 | $t_{WL1DX}$ | $t_{DH}$ | Data In Hold Time | 15 | | 15 | | 20 | | 25 | | ns | 15 |
| 40 | $t_{GH2WH1}$ | $t_{OWS}$ | $\overline{OE}$ Setup Time from End of Write | 15 | | 20 | | 25 | | 30 | | ns | |
| 41 | $t_{CH1GL2}$ | $t_{COH}$ | $\overline{OE}$ Hold Time from $\overline{CAS}$ | 15 | | 20 | | 25 | | 30 | | ns | |
| 42 | $t_{RL2RL2}$ (RMW) | $t_{RWC}$ | Read/Modify/Write Cycle Time | 185 | | 210 | | 250 | | 290 | | ns | |
| 43 | $t_{RL1RH1}$ (RMW) | $t_{RRW}$ | RMW Cycle $\overline{RAS}$ Pulse Width | 125 | | 145 | | 175 | | 205 | | ns | |
| 44 | $t_{CL1CH1}$ (RMW) | $t_{CRW}$ | RMW Cycle $\overline{CAS}$ Pulse Width | 80 | | 95 | | 110 | | 125 | | ns | |
| 45 | $t_{RL1AX}$ (RMW) | $t_{AR}$ | Column Address Hold Time from $\overline{RAS}$ (RMW Cycle) | 120 | | 135 | | 165 | | 195 | | ns | |
| 46 | $t_{RL1WL2}$ | $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay | 95 | | 110 | | 135 | | 160 | | ns | 13 |
| 47 | $t_{AVWL2}$ | $t_{AWD}$ | Column Address to $\overline{WE}$ Delay | 60 | | 70 | | 80 | | 85 | | ns | 13 |
| 48 | $t_{CL1WL2}$ | $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay | 50 | | 60 | | 70 | | 80 | | ns | 13 |
| 49 | $t_{GH2WL2}$ | $t_{OWD}$ | $\overline{OE}$ to $\overline{WE}$ Delay | 20 | | 25 | | 30 | | 35 | | ns | |
| 50 | $t_{WL2WL2}$ | $t_{SWC}$ | Static Column Mode Write Cycle Time | 45 | | 50 | | 55 | | 60 | | ns | |
| 51 | $t_{WH2QV}$ | $t_{WPA}$ | Write Precharge Access Time | | 20 | | 25 | | 30 | | 35 | ns | 9,16 |
| 52 | $t_{WL1QV}$ | $t_{WRA}$ | Write-Read Access Time | | 85 | | 95 | | 105 | | 115 | ns | 9,16 |
| 53 | $t_{WL1GL2}$ | $t_{WOH}$ | Write to $\overline{OE}$ Hold Time | 20 | | 20 | | 25 | | 30 | | ns | |
| 54 | $t_{RL1WL2}$ | $t_{SWH}$ | Delay from $\overline{RAS}$ to Second Write Command | 70 | | 80 | | 100 | | 120 | | ns | |
| 55 | $t_{RL1DX}$ | $t_{DHR}$ | Data In Hold Time Referenced to $\overline{RAS}$ | 55 | | 60 | | 70 | | 80 | | ns | |
| 56 | $t_{AVAV(R)}$ | $t_{SRC}$ | Static Column Mode Read Cycle | 45 | | 50 | | 55 | | 60 | | ns | |

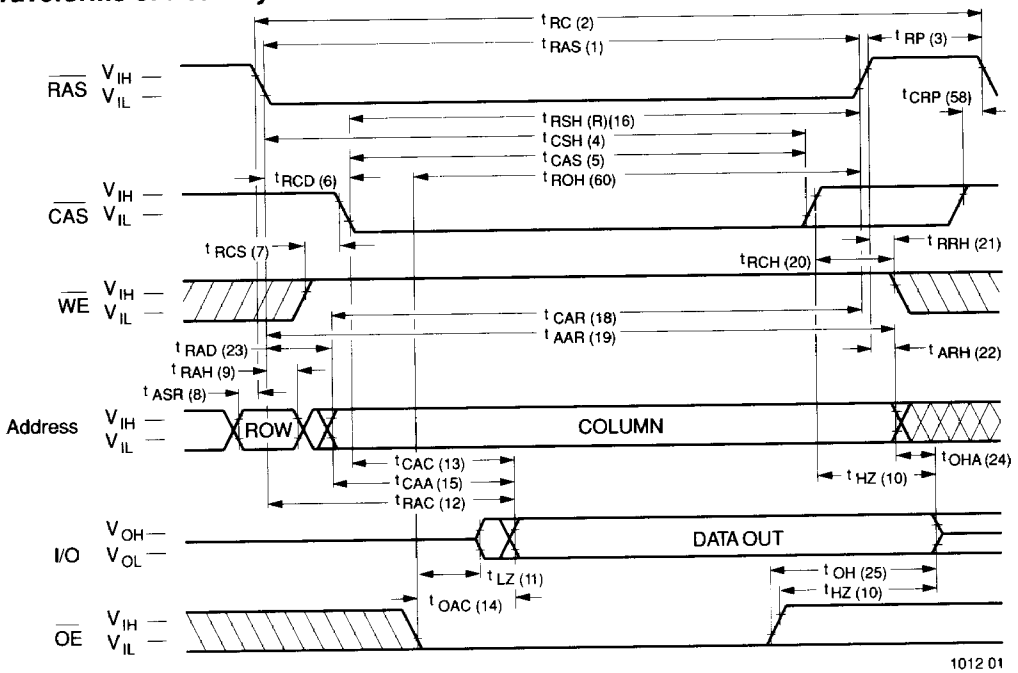
## AC Characteristics (Cont'd.)

| # | JEDEC Symbol | Symbol | Parameter | 70/70L | | 80/80L | | 10/10L | | 12/12L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 57 | $t_{CH2WH1}$ | $t_{WHC}$ | Write Command Hold Time Referenced to $\overline{CAS}$ | 0 | | 0 | | 0 | | 0 | | ns | 13 |
| 58 | $t_{CH2RL2}$ | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 15 | | 15 | | 15 | | 20 | | ns | |
| 59 | $t_{OEL1RH1}$ | $t_{ROH}$ | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| 60 | $t_{RL1CH1}$ | $t_{CHR}$ | $\overline{CAS}$ Hold Time $\overline{CAS}$-Before-$\overline{RAS}$ Cycle | 20 | | 25 | | 30 | | 40 | | ns | |
| 61 | $t_{RH2CL2}$ | $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 62 | $t_{CL1RL1}$ | $t_{CSR}$ | $\overline{CAS}$ Setup Time $\overline{CAS}$-Before-$\overline{RAS}$ Cycle | 10 | | 10 | | 10 | | 10 | | ns | |
| 63 | $t_{CH2CL2}$ | $t_{CP}$ | $\overline{CAS}$ Precharge Time | 15 | | 15 | | 20 | | 25 | | ns | |
| | $t_T$ | $t_T$ | Transition Time (Rise and Fall Time) | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | 17 |
| | | $t_{RI}$ | Refresh Interval (256 Cycles) | | 4 | | 4 | | 4 | | 4 | ms | 18 |

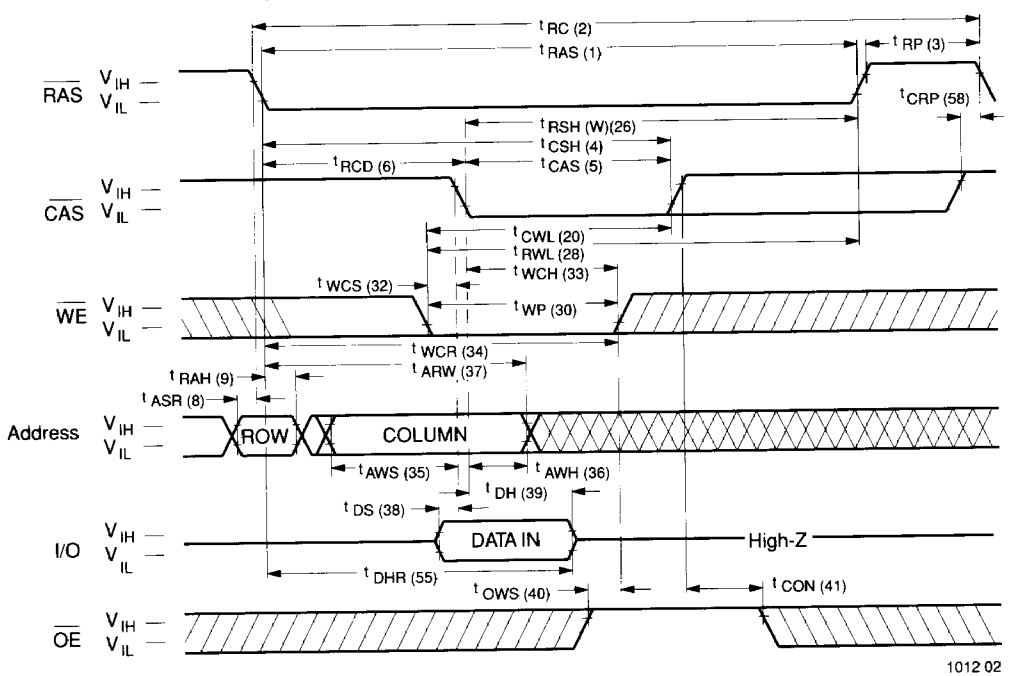
Notes:

1. $I_{DD}$ is dependent on output loading when the device output is selected. Specified $I_{DD}$ (max.) is measured with the output open.
2. $I_{DD}$ is dependent upon the number of address transitions. Specified $I_{DD}$ (max.) is measured with a maximum of two transitions per address cycle in Static Column Mode.
3. Specified $V_{IL}$ (min.) is steady state operating. During transitions, $V_{IL}$ (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with $V_{IL}$ (min.) ≥ $V_{SS}$ and $V_{IH}$ (max.) ≤ $V_{DD}$.
4. $t_{RCD}$ (max.) is specified for reference only. Operation within $t_{RCD}$ (max.) and $t_{RAD}$ (max.) limits ensure that $t_{RAC}$ (max.) and $t_{CAA}$ (max.) can be met. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max.), the access time is controlled by $t_{CAA}$ and $t_{CAC}$.
5. Assumes three state test load of 5 pF and a 380 Ohm Thevenin equivalent.
6. At any given temperature and voltage combination, coincident deselection/selection is permissible for "wire ORed" devices.
7. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If $t_{RAD}$ is greater than $t_{RAD}$ (max.), $t_{RAC}$ will increase by the amount that $t_{RAD}$ exceeds $t_{RAD}$ (max.).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If $t_{RCD}$ is greater than $t_{RCD}$ (max.), $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds $t_{RCD}$ (max.).
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a Read Cycle to occur.
12. Operation within the $t_{RAD}$ (max.) limit ensures that $t_{RAC}$ (max.) can be met. $t_{RAD}$ (max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max.) limit, the access time is controlled by $t_{CAA}$ and $t_{CAC}$.
13. $t_{WCS}$, $t_{WHC}$, $t_{RWD}$, $t_{AWD}$ and $t_{CWD}$ are not restrictive operating parameters.
14. $t_{WCS}$ (min.) must be satisfied in an Early Write Cycle.
15. $t_{DS}$ and $t_{DH}$ are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
16. Access time is determined by the longest of $t_{CAA}$, $t_{WPA}$ and $t_{WRA}$.
17. $t_T$ is measured between $V_{IH}$ (min.) and $V_{IL}$ (max.). AC measurements assume $t_T$ = 5 ns.
18. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

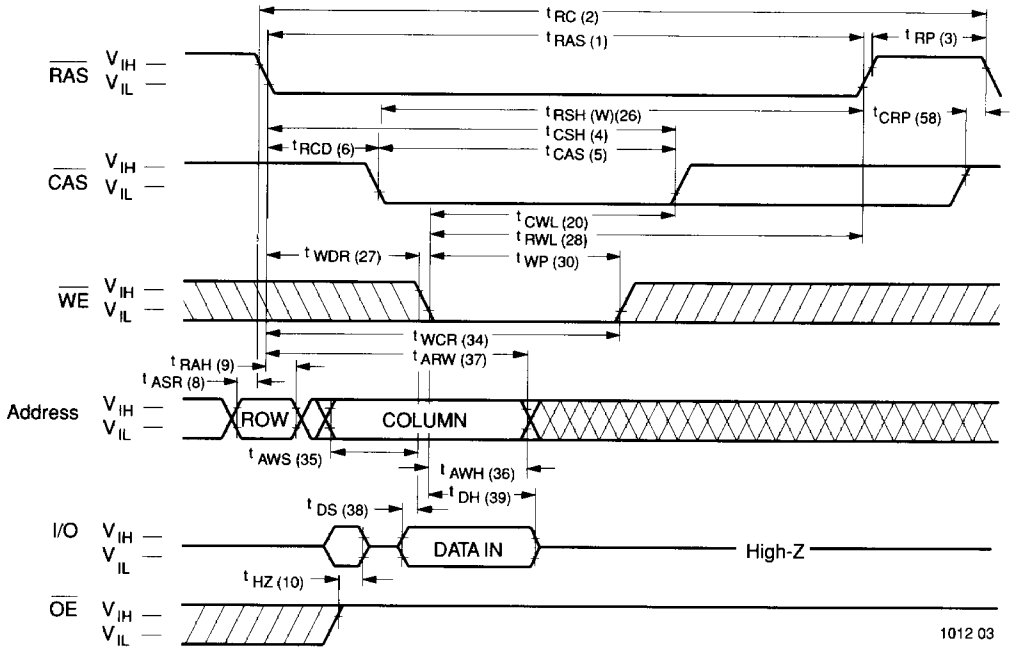
## Waveforms of Read Cycle



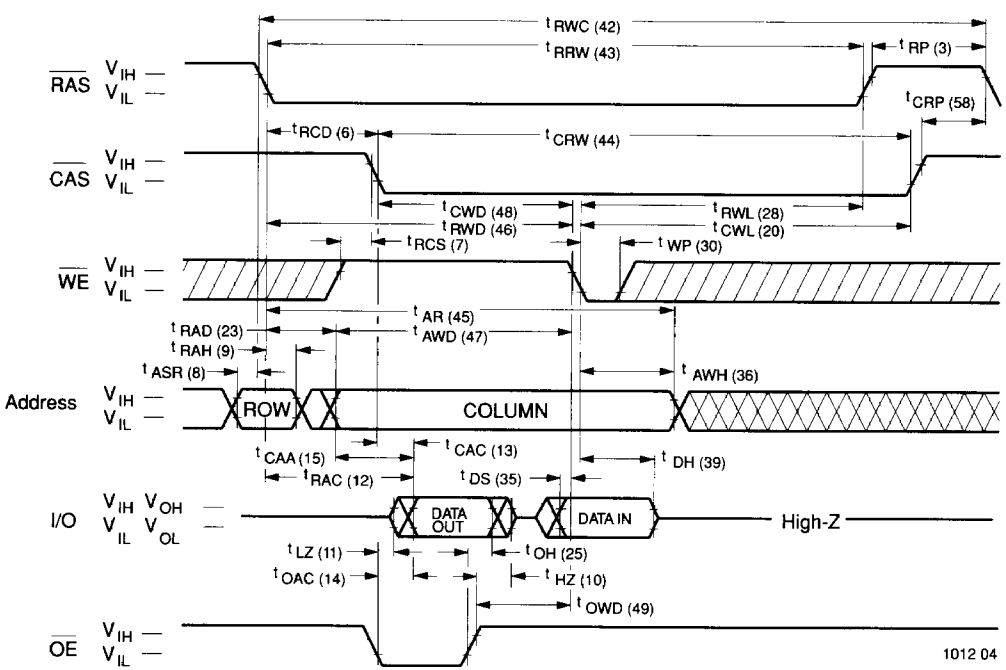

## Waveforms of Write Cycle ($\overline{CAS}$-Controlled)



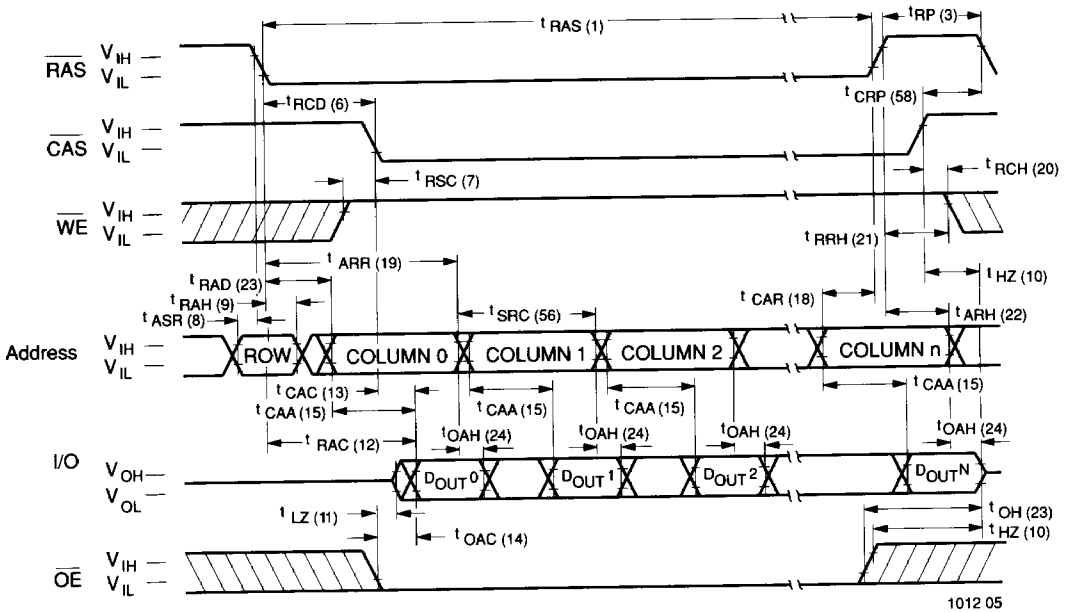
## Waveforms of Write Cycle ($\overline{WE}$-Controlled)



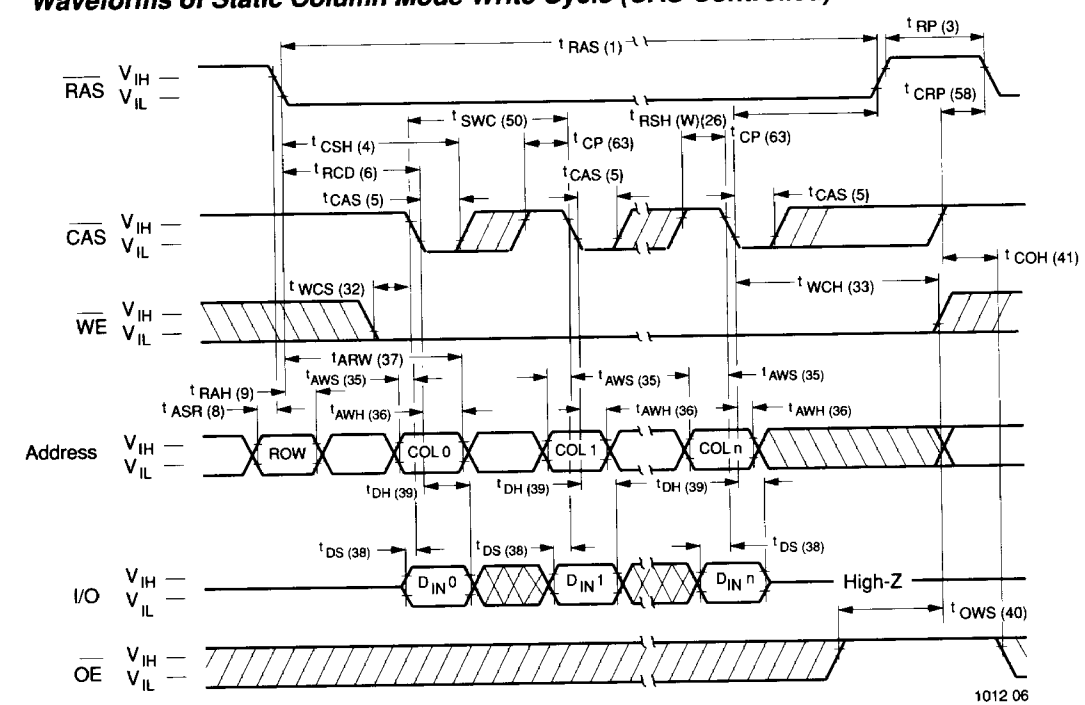

## Waveforms of Read-Modify-Write Cycle



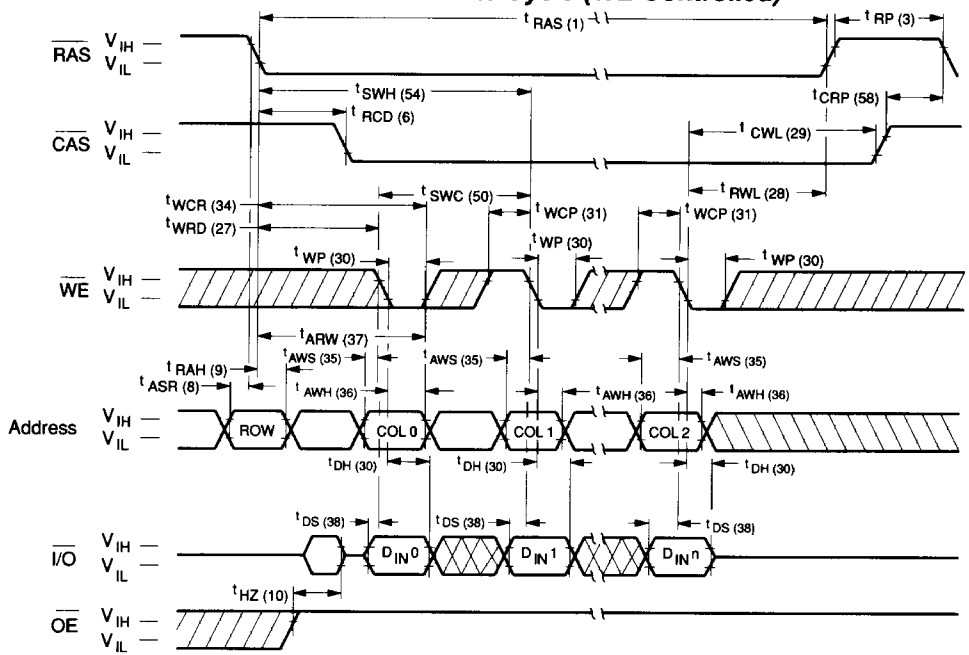
## Waveforms of Static Column Mode Read Cycle




## Waveforms of Static Column Mode Write Cycle (CAS-Controlled)



## Waveforms of Static Column Mode Write Cycle ($\overline{WE}$-Controlled)

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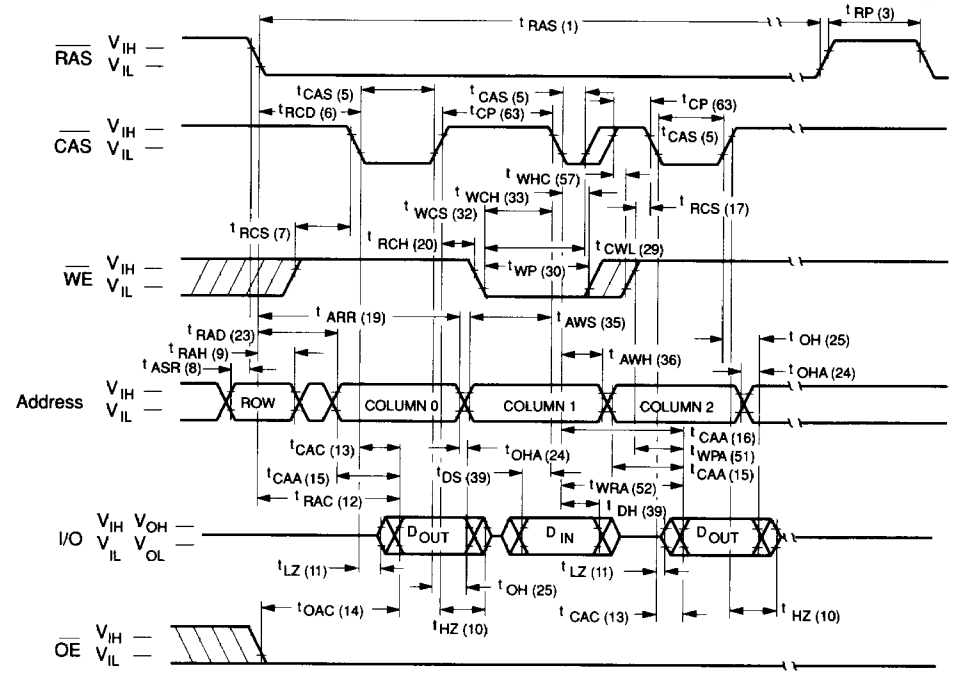
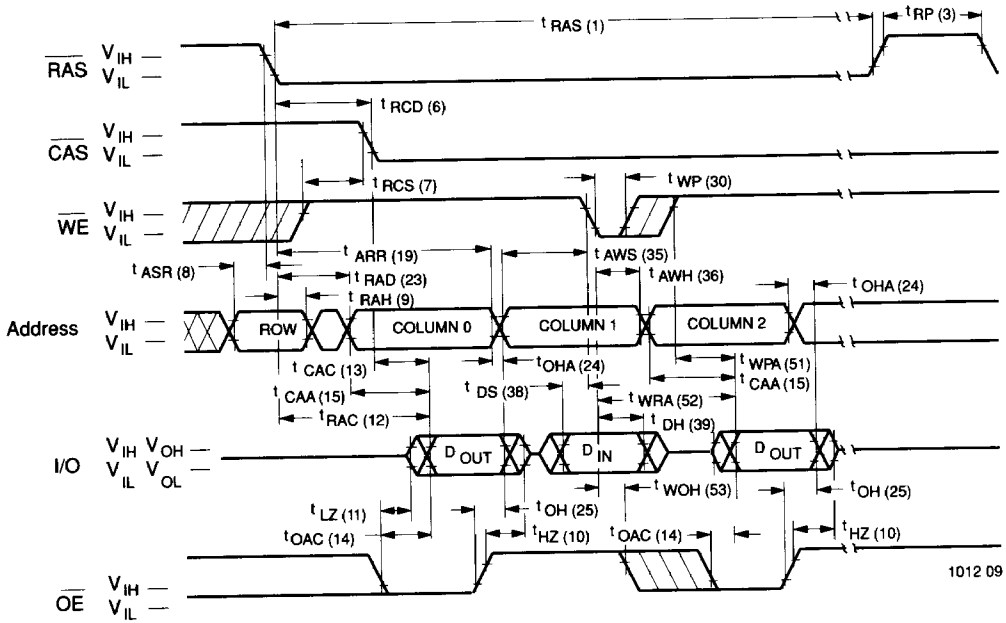
## Waveforms of Static Column Mode Read-Write-Read Cycle ($\overline{CAS}$-Controlled)

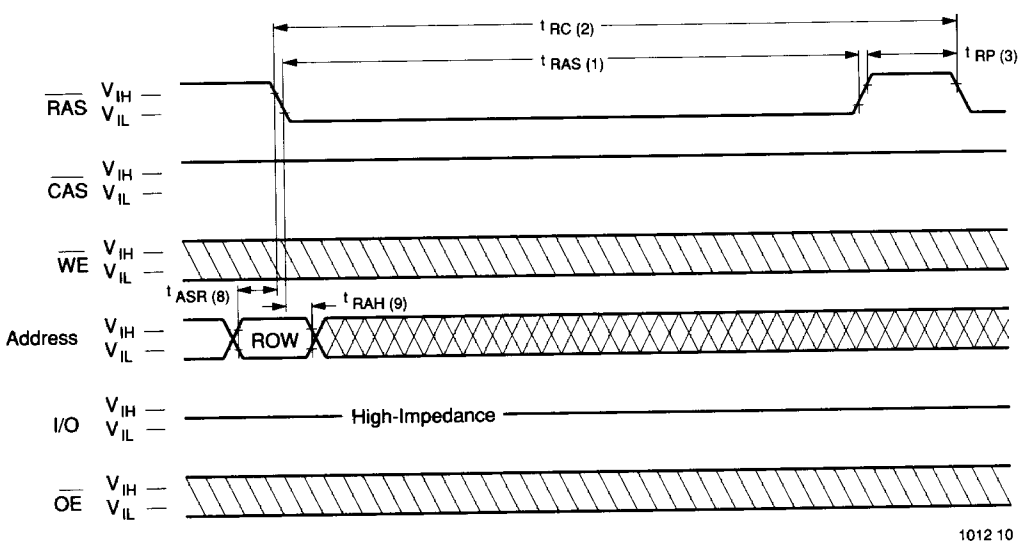



1012 08

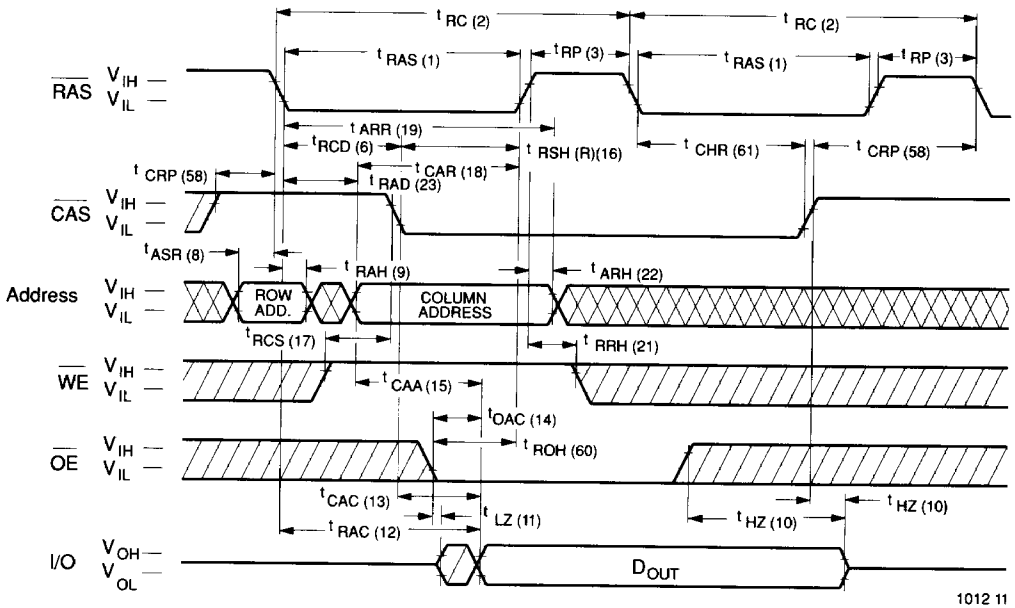
## Waveforms of Static Column Mode Read-Write-Read Cycle ($\overline{WE}$-Controlled)



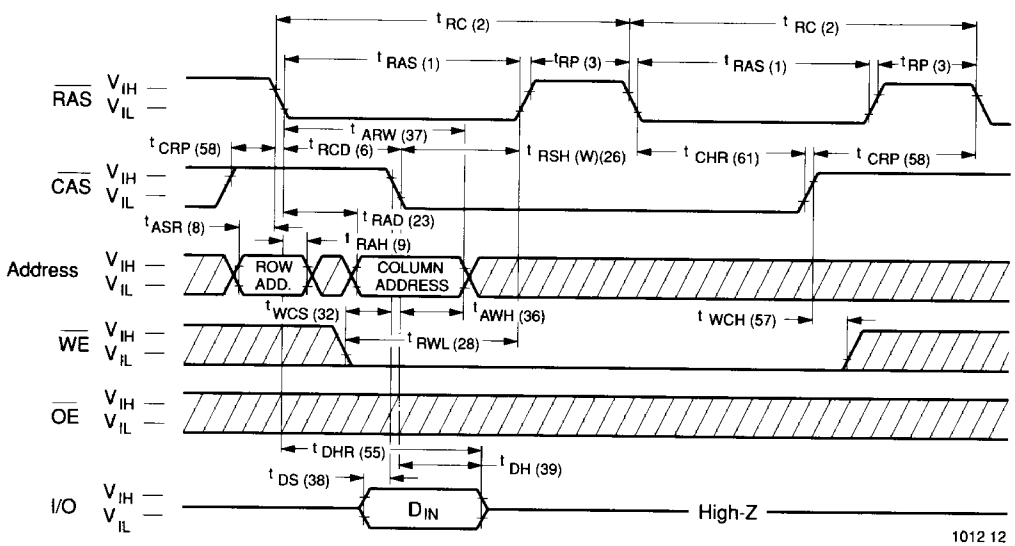

## Waveforms of $\overline{RAS}$-Only Refresh Cycle



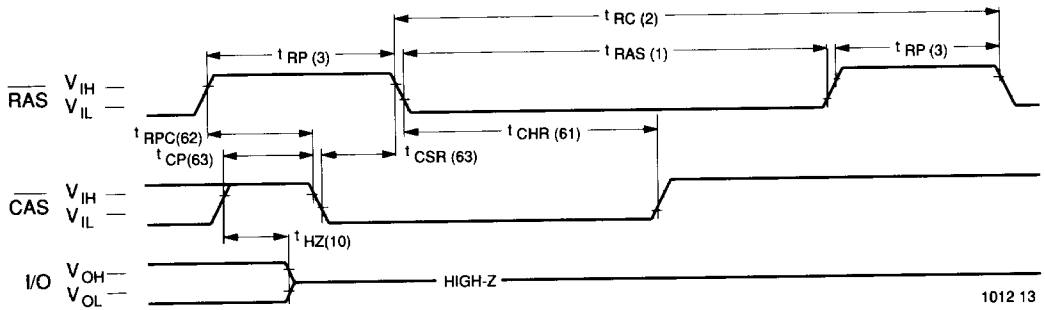
## Waveforms of Hidden Refresh Cycle (Read)



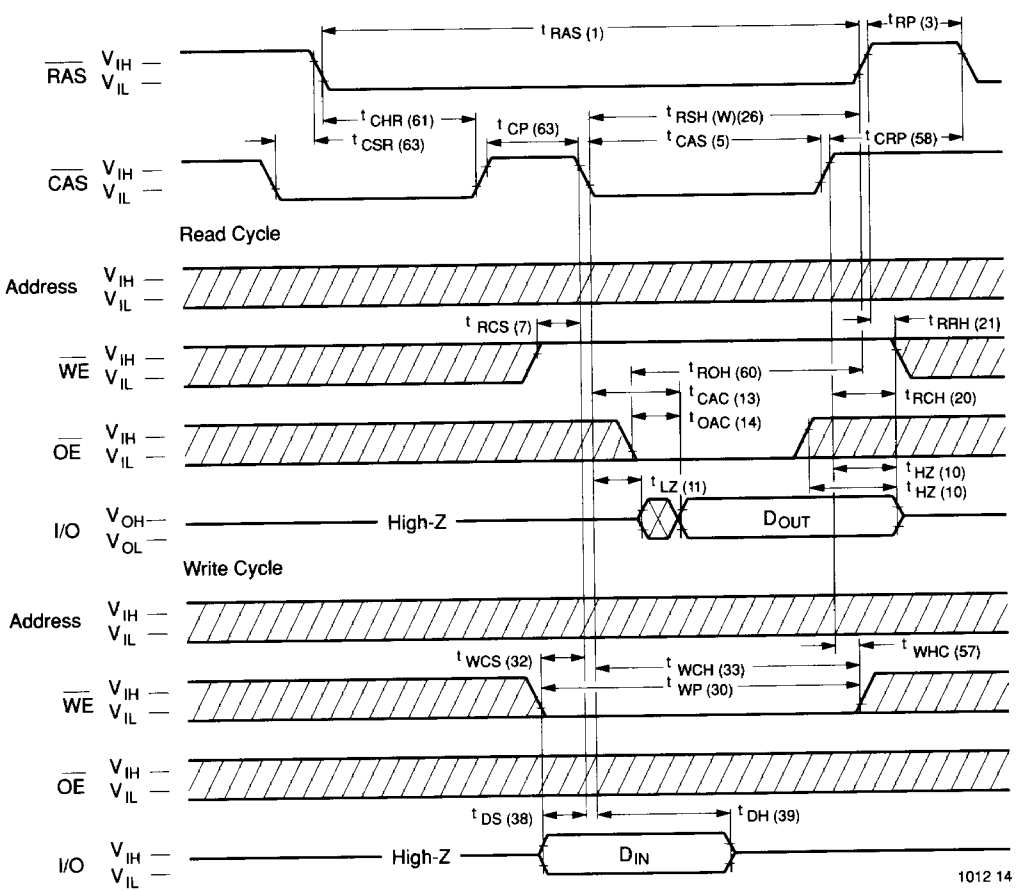

## Waveforms of Hidden Refresh Cycle (Write)



## Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle




## Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



## Functional Description

The V53C866 is a CMOS dynamic RAM optimized for high bandwidth and low power applications. It is functionally similar to other dynamic RAMs. The V53C866 can either read or write eight bits of data at a time by multiplexing a 16-bit address into an 8-bit row and an 8-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address, however, is only latched during a Write cycle by either Column Address Strobe ($\overline{CAS}$) or Write Enable ($\overline{WE}$), whichever occurs last. During a Read cycle, the column address is not latched and continuously "flows through" the internal input latches. Access time is primarily dependent on a valid column address. $\overline{CAS}$ acts as an output enable signal in the access path.

## Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. To ensure proper device operation and data integrity, a memory cycle must not be ended or aborted before fulfilling the minimum $t_{RAS}$ timing specification. Also, a new cycle must not be initiated until the minimum precharge time, $t_{RP}/t_{CP}$, has elapsed.

## Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address is not latched and must be held valid until $D_{OUT}$ becomes valid. I/O is controlled by the Output Enable ($\overline{OE}$) and $\overline{CAS}$. This relationship is discussed in the I/O Operation paragraph.

## Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$-initiated cycle. The column address is latched by the later of either $\overline{WE}$ or $\overline{CAS}$ going low. The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the cycle can be $\overline{WE}$-controlled or $\overline{CAS}$-controlled. In a $\overline{CAS}$ controlled Write cycle where the leading edge of $\overline{WE}$ occurs prior to or coincident with $\overline{CAS}$ low transition, the I/O pin will be in the High-Z state at the beginning of the Write cycle. Terminating the Write with $\overline{CAS}$ going high will maintain the I/O pins in the High-Z state. Terminating the Write cycle with $\overline{WE}$ going high allows the output to go active and starts a Read (Read after Write). If an input cycle is desired immediately after terminating a Write with $\overline{WE}$ going high, $\overline{OE}$ may be brought high to prevent the outputs from being in the active state and to allow inputs on the I/O lines.

The V53C866 incorporates a self-timed write feature that simplifies the system interface and optimizes data bandwidth. After the Write has been initiated, the V53C866 internally completes the write action and unlatches the address and data latches to be ready for the next input/output cycle. This eliminates the need for long address and data hold times during Write operations and allows a subsequent column address to be applied earlier. The write pulse width, write precharge and hold time are minimized, providing maximum flexibility in system design.

## Refresh Cycle

To retain data, 256 Refresh Cycles are required in each 4 ms period. There are two ways to refresh the memory:

1. By selecting each of the 256 row addresses determined by A0 through A7 at least once every 4 ms. Any Read, Write, Read-Modify-Write or refresh cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ is low during the falling edge of $\overline{RAS}$, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C866 will use the output of an internal 8-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a refresh mode only, and no data access or device selection is allowed. Therefore, the state of $D_{OUT}$ will remain at High-Z. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to execute 256 consecutive Write cycles and then verify the written data by applying 256 consecutive Read cycles. In this mode, the V53C866 ignores external row/column addresses and takes the output from the internal counter instead.

### Data Retention Mode

The V53C866 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid $V_{IL}$ and an "extra high" $V_{IH}$ within 0.2 V of $V_{DD}$. While the $\overline{RAS}$ clock is at the "extra high" level, the power consumption is reduced to the low CMOS standby level ($I_{DD6}$). Overall $I_{DD}$ consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where $t_{RC}$ = Refresh Cycle Time
$t_{RX}$ = Refresh Interval / 256

### Static Column Mode Operation

Static Column Mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, Write and Read-Write-Read cycles can be performed during Static Column operation. The row address is internally retained by maintaining $\overline{RAS}$ active. Following the entry cycle into Static Column mode, data are accessed by simply changing the column address. Because the column address buffer acts as transparent or flow-through latches, access begins from a valid column address. Thus, the V53C866 behaves like a Static RAM for multiple column accesses within an active row that has been accessed by $\overline{RAS}$. Static Column mode allows mixed Read and Write cycles.

Static Column Mode provides a sustained data rate of over 22 MHz (x 4 bits) for applications that require high bandwidth. The following equation can be used to calculate the data rate achievable:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255 \times t_{SRC}}$$

### I/O Operation

The V53C866 Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. An $\overline{OE}$ low transition or an $\overline{OE}$ low level enables the output drivers when the I/O data path is enabled. An $\overline{OE}$ high transition or an $\overline{OE}$ high level disables the output driver but does not affect the data stored in output latches. If a $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enabled prior to the $\overline{WE}$ low transition, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time ($t_{DS}$) to be satisfied.

### Power-On

After application of the $V_{DD}$ supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods exceeding the Refresh Interval of bias without clocks.

During Power-On, the $V_{DD}$ current requirement of the V53C866 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during Power-On, the device will go into an active cycle, and $I_{DD}$ will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with $V_{DD}$ or be held at a valid $V_{IH}$ during Power-On to avoid current surges.

**Table 1. Vitelic V53C866 Data Output**
*Operation for Various Cycle Types*

| Cycle Type | $D_{OUT}$ State |
|---|---|
| Read Cycles | Data from Addressed Memory Cell |
| $\overline{CAS}$-Controlled Write Cycle (Early Write) | High–Z |
| $\overline{WE}$-Controlled Write Cycle (Late Write) | Active, not valid |
| Read-Modify-Write Cycles | Data from Addressed Memory Cell |
| Static Column Mode Read Cycle | Data from Addressed Memory Cell |
| Static Column Mode Write Cycle (Early Write) | High-Z |
| Static Column Mode Read-Modify-Write Cycle | Data from Addressed Memory Cell |
| $\overline{RAS}$-only Refresh | High-Z |
| $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle | Data remains as in previous cycle |
| $\overline{CAS}$-only Cycles | High-Z |