DATA SHEET

TDA9150
Programmable deflection controller

Objective specification
File under Integrated circuits, IC02

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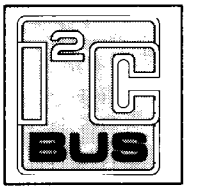
Philips Semiconductors

PHILIPS

Programmable deflection controller TDA9150



FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I²C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Two-level sandcastle pulse

Vertical deflection

- Self-adaptive 16-bit precision vertical scan
- DC coupled deflection to prevent picture bounce
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity

East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity

Horizontal deflection

- φ 2 loop with low jitter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I²C-bus
- Flash detector with automatic soft restart
- over-voltage protection with restart by I²C-bus

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter

General description

The TDA9150 is a programmable deflection controller contained in a 20-pin DIL package and constructed using BIMOS technology. This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards. The TDA9150 uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device is self-adaptive for a number of functions and is fully programmable via the I²C-bus.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9150	20	DIL	plastic	SOT146

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	f_{CLK} = 6.75 MHz	–	22	–	mA
P_{tot}	total power dissipation		–	175	–	mW
T_{amb}	operating ambient temperature range		−25	–	+70	°C
Inputs						
V_{14}	line-locked clock (LLC) logic level		–	TTL	–	V
V_{13}	horizontal sync (H_A) logic level		–	TTL	–	V
V_{12}	vertical sync (V_A) logic level		–	TTL	–	V
V_5	line-locked clock select (LLCS) logic level	note 1	–	CMOS 5 V	–	V
V_{18}	serial clock (SCL) logic level		–	CMOS 5 V	–	V
V_{17}	serial data (SDA) input logic level		–	CMOS 5 V	–	V
V_1	horizontal flyback (HFB) phase slice level	FBL = 0 FBL = 1	– –	4.0 1.3	– –	V V
V_1	horizontal flyback (HFB) blanking slice level		–	100	–	mV
V_3	over-voltage protection (PROT) detection level		–	4.0	–	V
V_7	EHT flash detection level		–	550	–	mV
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10 mA	–	–	0.5	V
$I_{11}/I_{10(p-p)}$	vertical differential ($VOUT_{A, B}$) output current (peak-to-peak value)	vertical amplitude = 100%; I_8 = −100 µA	–	1000	–	µA
$V_{10,11}$	vertical output voltage range		0	–	3.9	V
$I_{6(peak)}$	EW (EWOUT) total output current (peak value)	I_8 = −100 µA	–	500	–	µA
V_6	EW (EWOUT) output voltage range		1.0	–	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_{BL}	base level		–	0.5	–	V
V_{HV}	horizontal and vertical blanking level		–	2.5	–	V
V_{clamp}	video clamp level		–	4.5	–	V

Note to the quick reference data

1. Hard wired to V_{SS} or V_{CC} is highly recommended.

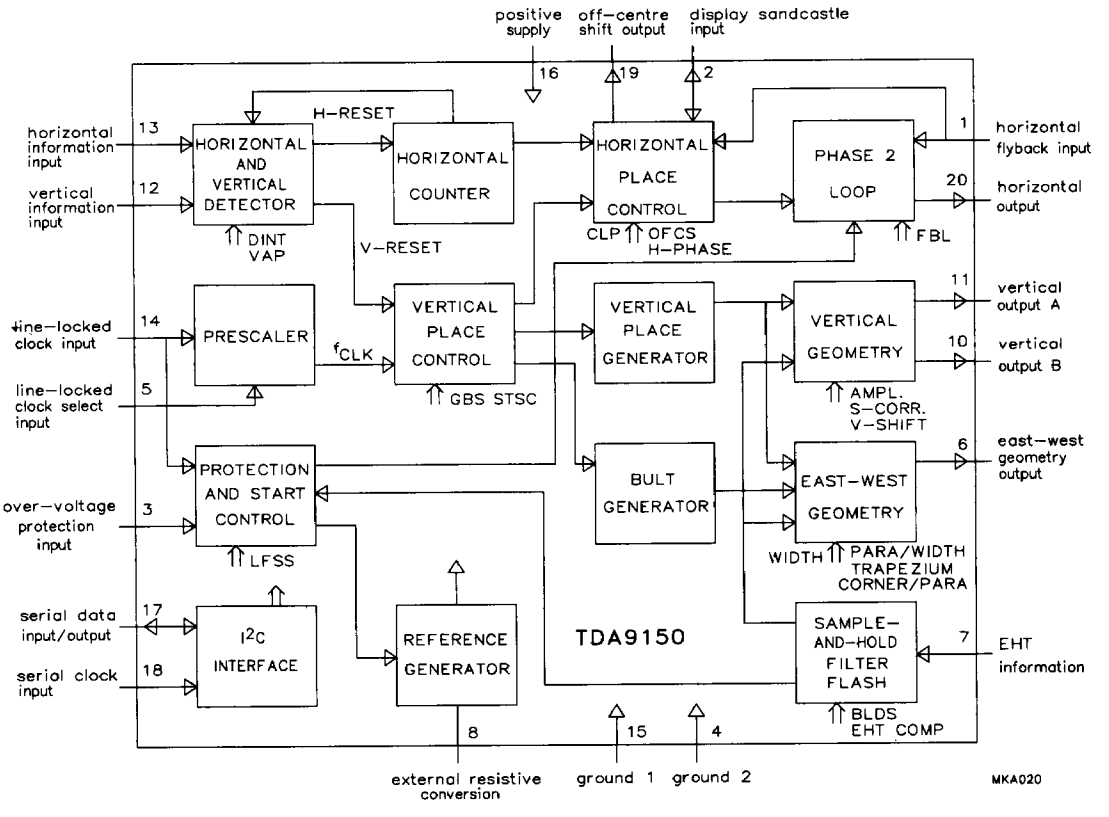


Fig.1 Block diagram.

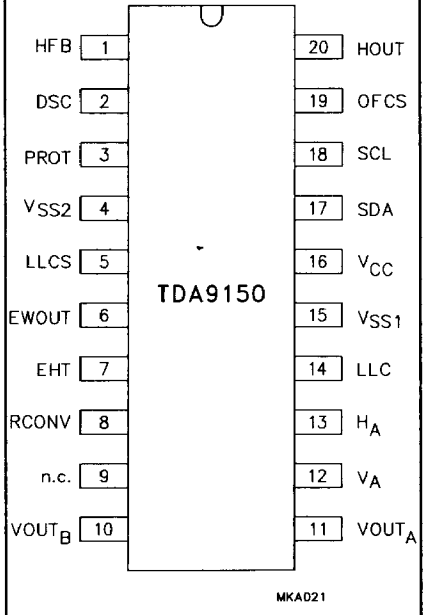


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
HFB	1	horizontal flyback input
DSC	2	display sandcastle input/output
PROT	3	over-voltage protection input
V_{SS2}	4	ground 2
LLCS	5	line-locked clock select input
EWOUT	6	east-west geometry output
EHT	7	EHT information
RCONV	8	external resistive conversion
n.c.	9	not connected
$VOUT_B$	10	vertical output B
$VOUT_A$	11	vertical output A
V_A	12	vertical information input
H_A	13	horizontal information input
LLC	14	line-locked clock input
V_{SS1}	15	ground 1
V_{CC}	16	positive supply input
SDA	17	serial data input/output
SCL	18	serial clock input
OFCS	19	off-centre shift output
HOUT	20	horizontal output

Functional description

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9150 requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I²C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.
I²C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the H_A and V_A for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 µs and the vertical and EW output current will drop to zero within 100 µs). The SDA and SCL inputs meet the I²C specification, the other three inputs are TTL compatible.
The LLC frequency can be divided by two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.
The LLC timing is given in the characteristics.

I²C-bus commands

Slave address:
8C HEX = 1000110X BIN

READ MODE

The format of the status byte is;
PON PROT 0 0 0 0 0 0

Where;

PON is the status bit for power-on-reset and after power failure

logic 1 — after the first POR and after power failure. Also set to 1 after a severe voltage dip that may have disturbed the various settings.

logic 0 — after a successful read of the status byte.

PROT is the over-voltage detection e.g. for the scaled EHT

logic 1 — if the input voltage rises above the reference value of 4 V. This results also in a reset of LFSS which terminates the deflection. A restart is achieved with an I²C-bus command i.e. by writing a logic 1 to LFSS (deflection will not start as long as the PROT bit is still logic 1; a read action must first be performed).

logic 0 — after a successful read of the status byte.

Note: A read action is considered successful when an End Of Data signal has been detected (i.e. no master acknowledge).

Table 1 Write mode: subaddress and data byte format

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
vertical amplitude	00	X	X	A5	A4	A3	A2	A1	A0
vertical S-correction	01	X	X	A5	A4	A3	A2	A1	A0
vertical start scan	02	X	X	A5	A4	A3	A2	A1	A0
vertical off-centre shift	03	X	*	*	*	X	A2	A1	A0
EW trapezium correction	03	X	A6	A5	A4	X	*	*	*
EW width/width ratio	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width ratio	05	X	X	A5	A4	A3	A2	A1	A0
EW corner/parabola ratio	06	X	X	A5	A4	A3	A2	A1	A0
EHT compensation	07	X	X	A5	A4	A3	A2	A1	A0
horizontal phase	08	X	X	A5	A4	A3	A2	A1	A0
horizontal off-centre shift	09	X	X	A5	A4	A3	A2	A1	A0
clamp shift	0A	X	X	X	X	X	A2	A1	A0
control	0B	X	X	FBL	VAP	BLDS	LFSS	DINT	GBS

Where: X = don't care; * = data bit used in another function

Table 2 Control bits

CONTROL BIT	LOGIC	FUNCTION
LFSS	0	line stop: becomes 0 after a HIGH on PON or PROT
	1	line start enable: the soft start mechanism is now activated
DINT	0	de-interlace ON: the V_A pulse is sampled with the detected rising edge of H_A
	1	de-interlace OFF: the V_A pulse is sampled with the system clock and the detected rising edge is used as vertical reset
BLDS	0	aquadag selected
	1	bleeder selected
GBS	0	guardband 16/12 lines: becomes 0 after power-on
	1	guardband 48/12 lines
VAP	0	positive $V_A$edge detection
	1	negative $V_A$edge detection
FBL	0	horizontal flyback slicing level = 4 V
	1	horizontal flyback slicing level = 1.3 V

Table 3 Clock frequency control bit (pin 5)

CONTROL BIT	LOGIC	FUNCTION
LLCS	0	prescaler ON: the internal clock frequency $f_{CLK} = f_{LLC}/2$
	1	prescaler OFF: (default by internal pull-up resistor). The internal clock frequency $f_{CLK} = f_{LLC}$

Note to Table 3

Switching of the prescaler is only allowed when LFSS is LOW. It is highly recommended to hard wire LLCS to V_{SS} or V_{CC}.

Active switching may damage the output power transistor due to the changing HOUT pulse. This may cause very high currents and huge flyback pulses. The permitted combinations of LLC and the prescaler are given in table 4.

Table 4 Line duration with prescaler

LLC (MHz)	ON (µs)	OFF (µs)
6.75	*	64
13.5	64	32
27	32	*

Where: * = not allowed combination.

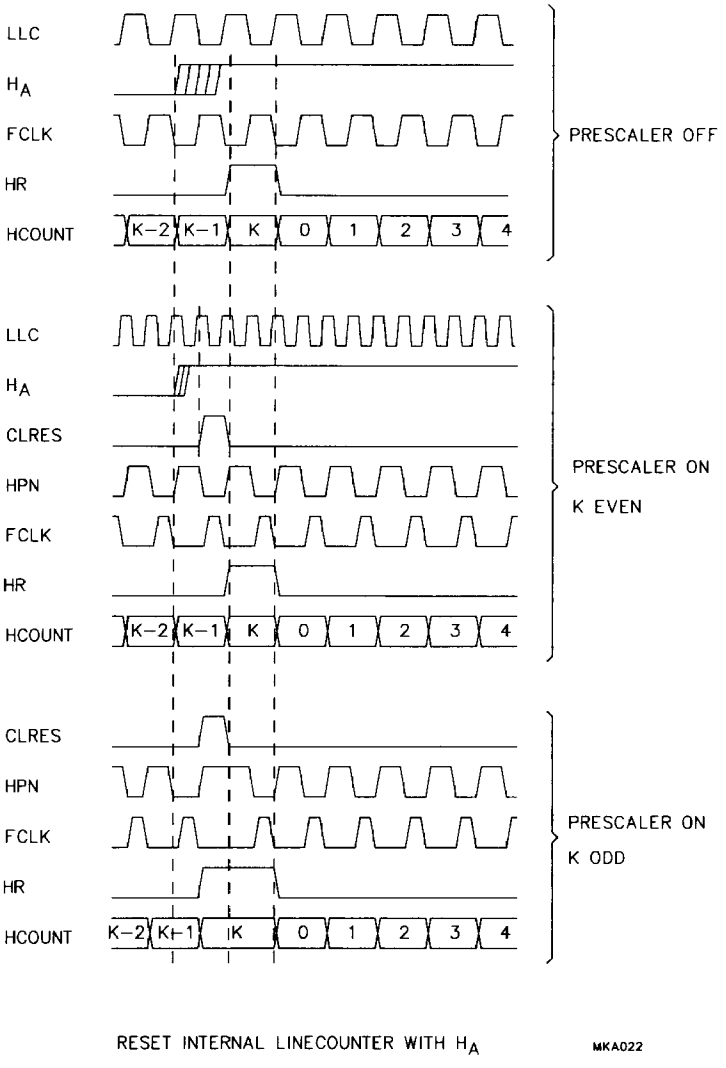


Fig.3 Timing relations between LLC, H_A and line counter.

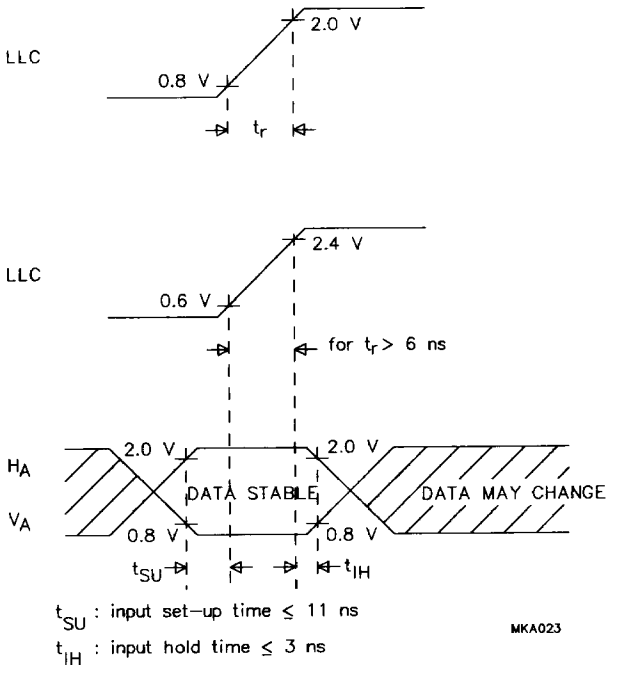


Fig.4 Timing requirements for LLC, H_A and V_A.

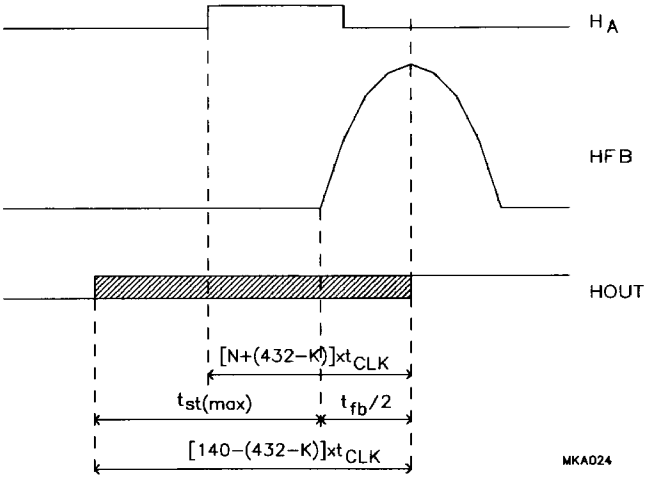


Fig.5 Horizontal phase and HOUT control range.

Horizontal part (pins 1, 2, 13, 19 and 20)

SYNCHRONIZATION PULSE

The H_A input (pin 13) is a TTL-compatible ESD protected CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.4. For proper detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods.

FLYBACK INPUT PULSE

The HFB input (pin 1) is an ESD protected CMOS input. The delay of the centre of the flyback pulse to the leading edge of the H_A pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08) as illustrated in Fig.5. The resolution is 6-bit.

OUTPUT PULSE

The HOUT pulse (pin 20) is an ESD protected open-drain NMOS output. The duty factor for this output is typically 55/45 (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 0 to 55% over a period of 400 lines in 400 steps.

OFF-CENTRE SHIFT

The OFCS output (pin 19) is an ESD protected push-pull CMOS output which is driven by a pulse-width modulated DAC.
By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 x 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.6.

SANDCASTLE

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamp. As an input it acts as a current sensor during the blanking interval for guard detection.

Clamp pulse

The clamp pulse width is 21 internal clock periods. The shift, w.r.t. H_A can be varied from 35 to 49 clock periods in 7 steps via the I²C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.7

Horizontal blanking

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{CLK}/f_H ratio 'K' [according to 41–(432–K)].
When the horizontal blanking pulse finishes is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level coincidence, as illustrated in Fig.8.

Vertical blanking

The vertical blanking pulse starts two internal clock pulses after the rising edge of the V_A pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Vertical guard).

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I²C-bus subaddress 02, (see Figs 9 and 10).

Vertical guard

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 500 µA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in case of missing or malfunctioning vertical deflection.

Vertical part (pins 6, 8, 10, 11 and 12)

Synchronization pulse

The V_A input (pin 12) is a TTL-compatible ESD protected CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.4. For proper detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods.

VERTICAL PLACE GENERATOR

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 x 432 clock periods, in 63 steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.
The minimum number of

synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15625 or 31250 Hz respectively.
If the V_A pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 µs.
Amplitude control is automatic, with a setting time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. The difference sequence and the difference sequence length are not important.

DE-INTERLACE

With De-interlace ON, the V_A pulse is sampled with the detected rising edge of the H_A pulse. The duration of the V_A pulse must, therefore, be sufficient to enable the H_A pulse to coincide, in this case an active time of minimum of half a line (see Fig.11).
With De-interlace OFF, the V_A pulse is sampled with the system clock. The rising edge is used as the vertical reset.

VERTICAL GEOMETRY PROCESSING

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The resistive conversion (pin 8) sets the reference current for both the vertical and EW geometry processing. A useful range is 50 to 100 µA, the recommended value is 100 µA.

VERTICAL OUTPUTS

The vertical outputs (pins 10 and 11) together form a differential current output and are ESD protected. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I²C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with 6-bit resolution.
The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is –2 to +2% in 7 steps set by the least significant nibble at subaddress 03.

EW GEOMETRY PROCESSING

The EW geometry processing is DC-coupled and therefore independent of field frequency. The resistive conversion (pin 8) sets the reference current for both the vertical and EW geometry processing. The EW output is an ESD-protected single-ended current output.
The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of –46 to 0% in 63 steps via subaddress 06.
The EW trapezium correction can be set from –4 to +4% in 7 steps via the most significant nibble at subaddress 03

BULT GENERATOR

The Bult generator makes the EW waveform continuous (see Fig.18).

EHT compensation (pin 7)

The EHT input is an ESD protected MOS input which permits scan amplitude modulation should the EHT supply be non-perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, given by the ratio R_{conv}_EW/R_{conv}, must be $V_{scan}/(20 \times V_{ref})$ (see Fig.12).
The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS). EHT compensation can be set via subaddress 07 in 63 steps allowing a scan modulation range from –10 to +9.7%. When the EHT input voltage drops below 0.55 V the outputs will be inhibited and an automatic restart will be performed.

Over-voltage protection (pin 3)

The over-voltage protection input is an ESD protected MOS input.
The input voltage can be the scaled EHT and has the following characteristics:

If the protection voltage is less than 4 V do nothing
If the protection voltage is greater than 4 V stop line drive

Restart by I²C-bus command:

1. perform read action to clear the PROT bit
2. write the LFSS bit

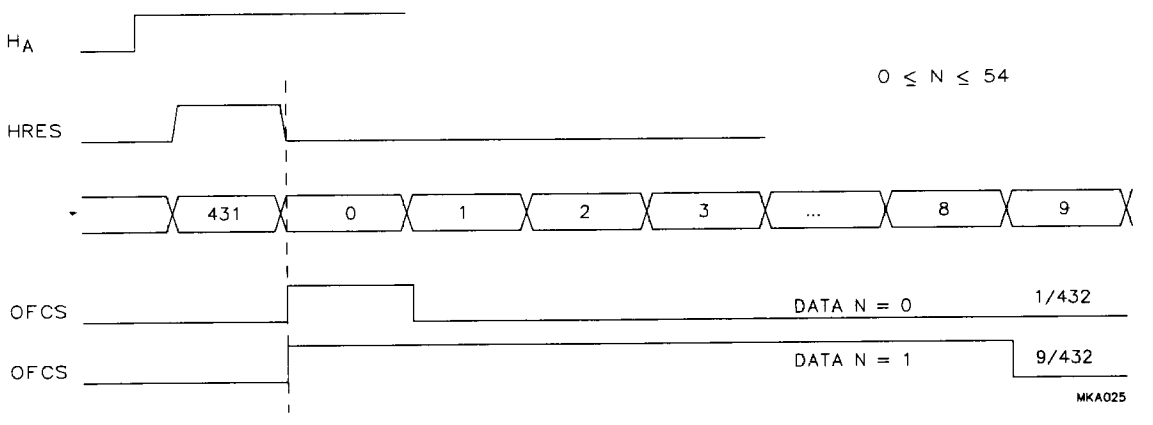


Fig.6 OFCS duty factor.

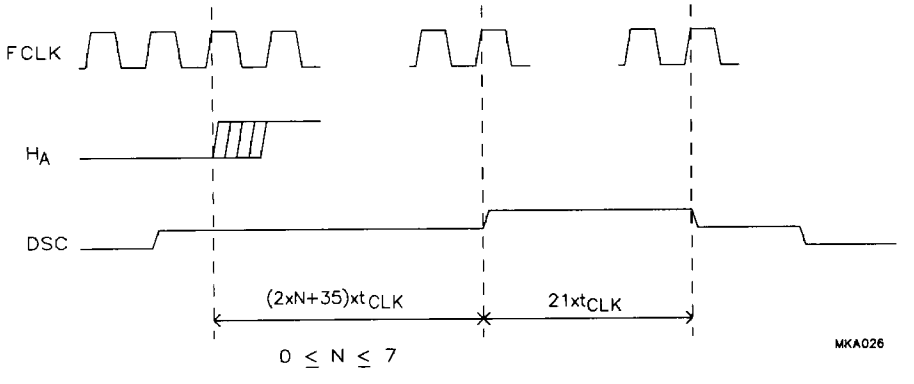


Fig.7 DSC clamp pulse.

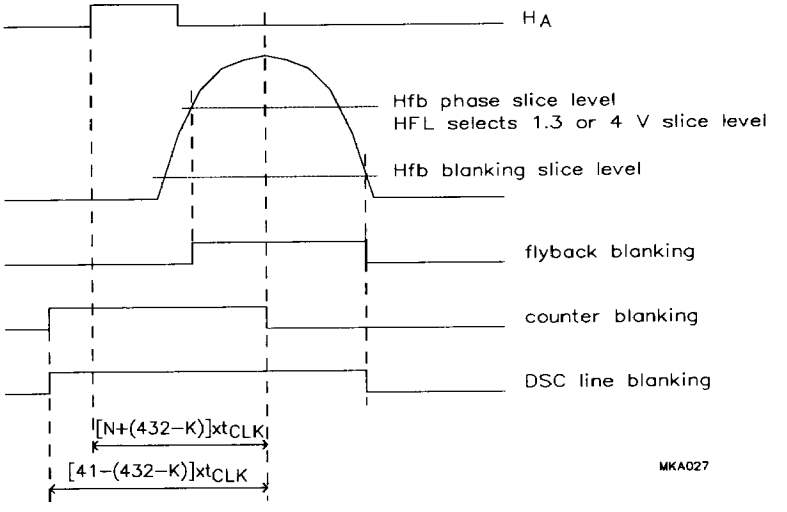


Fig.8 DSC line blanking.

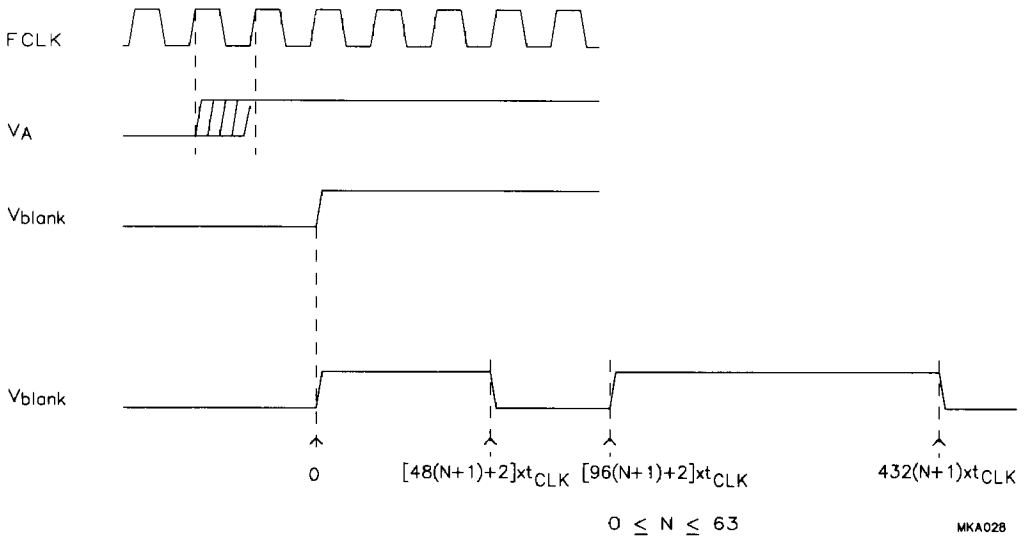


Fig.9 DSC vertical blanking with unblanking.

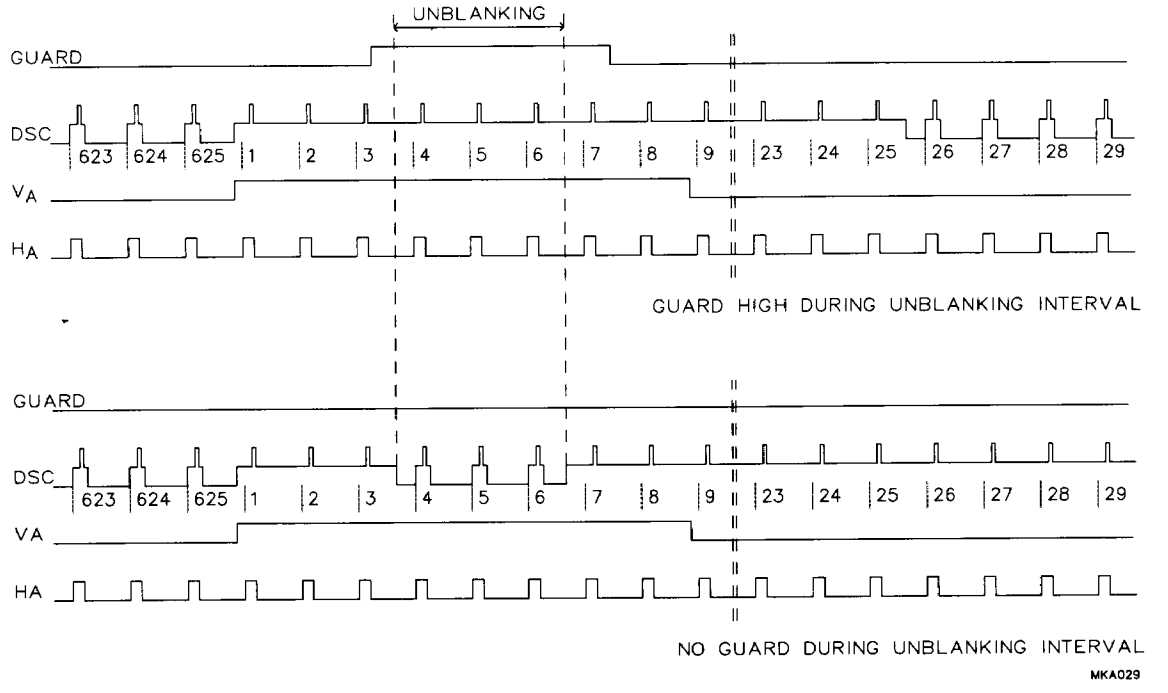


Fig.10 DSC with guard interval.

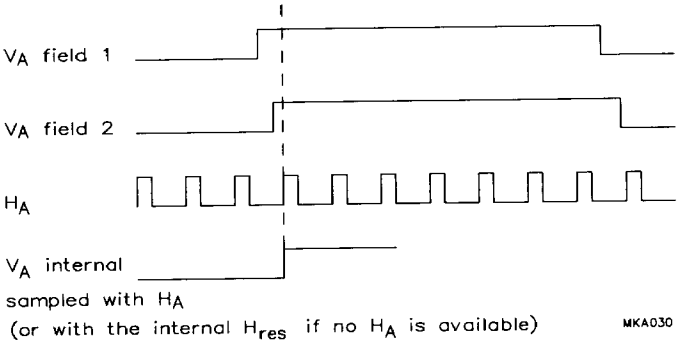


Fig.11 De-interlace timing.

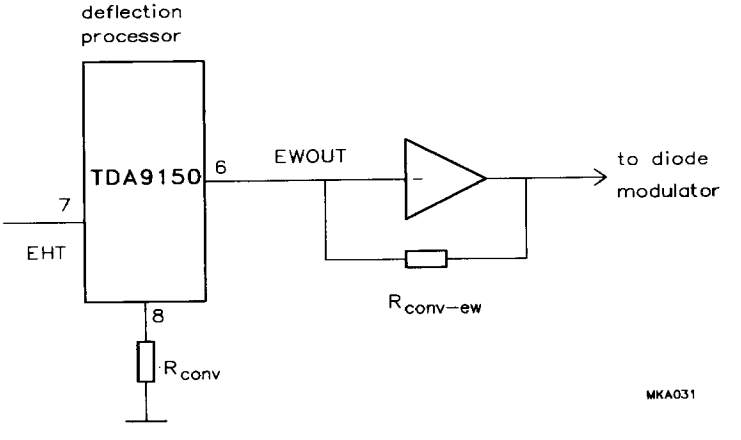


Fig.12 Explanation of R_{conv}_EW/R_{conv} ratio.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		−0.5	8.8	V
I_{CC}	supply current		−10	50	mA
P_{tot}	total power dissipation		−	500	mW
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−25	+70	°C
V_{supply}	voltage supplied to pins 1 to 3, 5 to 8, 10 to 14 and 17 to 20		−0.5	V_{CC}+0.5	V
$I_{I/O}$	current in or out of any pin except pins 4, 15 and 16		−20	+20	mA

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	70 K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; V_{SS1} = V_{SS2} = 0 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	note 1; f_{CLK} = 6.75 MHz	17	22	28	mA
P_{tot}	total power dissipation		−	175	−	mW
SDA and SCL (pins 17 and 18)						
V_{17}	SDA input voltage		0	−	5.5	V
V_{IL}	LOW level input voltage (pin 17)		−	−	1.5	V
V_{IH}	HIGH level input voltage (pin 17)		3.5	−	−	V
I_{IL}	LOW level input current (pin 17)	V_{17} = V_{SS1}	−	−	−10	µA
I_{IH}	HIGH level input current (pin 17)	V_{17} = V_{CC}	−	−	10	µA
V_{OL}	LOW level output voltage (pin 17)	I_{IL} = 3 mA	−	−	0.4	V
V_{18}	SCL input voltage		0	−	5.5	V
V_{IL}	LOW level input voltage (pin 18)		−	−	1.5	V
V_{IH}	HIGH level input voltage (pin 18)		3.5	−	−	V
I_{IL}	LOW level input current (pin 18)	V_{18} = V_{SS1}	−	−	−10	µA
I_{IH}	HIGH level input current (pin 18)	V_{18} = V_{CC}	−	−	10	µA
Line locked clock and Line locked clock select (pins 14 and 5)						
V_{IL}	LOW level input voltage (pin 14)		−	−	0.8	V
V_{IH}	HIGH level input voltage (pin 14)		2.0	−	−	V
I_{14}	input current	V_{14} = < 5.5 V	−	−	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r, t_f	rise and fall times		0	–	$t_{LLC}/2$	ns
	duty factor	note 2; LLCS = 0	40	50	60	%
		LLCS = 1	25	50	75	%
TIMING (PRESCALER ON) ($F_{CLK} = F_{LLC}/2$) WHERE F_{CLK} = INTERNAL CLOCK						
f_{LLC}	line-locked clock frequency		12.4	–	29.2	MHz
		f_{LLC}/f_H; H locked	856	864	865	
		f_{LLC}/f_H; H unlocked	–	866	–	
K	line-locked clock frequency ratio	f_{CLK}/f_H; H locked	428	432	432.5	
		f_{CLK}/f_H; H unlocked	–	433	–	
TIMING (PRESCALER OFF) ($F_{CLK} = F_{LLC}$) WHERE F_{CLK} = INTERNAL CLOCK						
f_{LLC}	line-locked clock frequency		6.2	–	14.6	MHz
		f_{LLC}/f_H; H locked	428	432	432	
		f_{LLC}/f_H; H unlocked	–	433	–	
K	line-locked clock frequency ratio	f_{CLK}/f_H; H locked	428	432	432	
		f_{CLK}/f_H; H unlocked	–	433	–	
V_5	LLCS input voltage		0	–	8.8	V
V_{IL}	LOW level input voltage (pin 5)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 5)		3.5	–	–	V
I_{IL}	LOW level input current (pin 5)	$V_5 = V_{SS1}$	–	–	–150	µA
I_{IH}	HIGH level input current (pin 5)	$V_5 = V_{CC}$	–	–	100	µA
Horizontal part						
INPUT SIGNALS						
H_A (pin 13)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_I	input current	V_{13} = 5.5 V	–	–	±10	µA
t_r; t_f	rise and fall times		0	–	$t_{LLC}/2$	ns
t_{WH}	pulse width HIGH		2	–	–	t_{CLK}
t_{WL}	pulse width LOW		2	–	–	t_{CLK}
HFB (pin 1)						
V_{PS1}	phase slice level	FBL = 0	3.8	4.0	4.2	V
V_{PH2}	phase slice level	FBL = 1	1.1	1.3	1.5	V
V_{blank}	blanking slice level		0	0.1	0.2	V
I_1	input current		–	–	±10	µA
Horizontal phase (delay centre flyback pulse to leading edge of H_A; where N = horizontal phase data)						
CR	control range		0	N	N+(432–K)	t_{CLK}
	number of steps		–	63	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT SIGNALS						
HOUT (pin 20)						
V_{20}	output voltage	$I_{20} = 0$	0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{20} = 10$ mA	–	–	0.5	V
I_I	input current	output OFF	–	–	±10	µA
	duty factor	normal operation	54.5	55.5	56.5	%
Soft start (duty factor controlled line drive)						
t_W	initial pulse width soft start		–	–	1.5	%
CR	control range		0	–	56.5	%
t_{ss}	soft start time		250	400	600	lines
Switch-off time to the centre of the flyback pulse						
CR	control range		0	–	140–(432–K)	t_{CLK}
Φ	control sensitivity (loop gain)		400	1000	–	µs/µs
f_G/f_H	unity gain frequency ratio		–	0.15	–	
t_{pj}	phase jitter with respect to LLC		–	–	5	ns
PSRR	power supply rejection ratio		tbf	–	–	µs/V
HORIZONTAL OFF-CENTRE SHIFT (PIN 19) (N = OFF-CENTRE SHIFT DATA)						
V_{19}	output voltage		0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{19} = 2$ mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	$I_{19} = -2$ mA	V_{CC}–0.5	–	–	V
	maximum duty factor	N < 54	1/K	(8N+1)/K	425/K	%
	duty factor	N ≥ 54	–	1	–	%
	number of steps		–	54	–	
SANDCASTLE (PIN 2)						
DSC output voltage						
V_{clamp}	video clamp voltage		4.0	4.5	5.0	V
V_{blank}	horizontal and vertical blanking level		2.0	2.5	3.0	V
V_{base}	base level		0	0.5	1.0	V
I_2	output current		–1.0	–	0.35	mA
		guard detected	0.8	–	2.5	mA
t_r; t_f	rise and fall times		–	60	–	ns
Clamp pulse (N = clamp pulse shift data)						
t_W	clamp pulse width		–	21	–	t_{CLK}
t_{clamp}	clamp pulse shift w.r.t H_A		35	2N+35	49	t_{CLK}
	number of steps		–	7	–	
t_{start}	start of horizontal blanking before middle of flyback pulse		38	41–(432–K)	41	t_{CLK} x 432

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical blanking width (N = vertical start-scan data)						
CR	control range		1	N+1	64	t_{CLK}
		K = 432	1	–	64	lines
	number of steps		–	63	–	
Guard detection (N = vertical start-scan data)						
t_{start}	start interval w.r.t V_A		48(N+1)+2	–	–	t_{CLK}
t_{stop}	stop interval w.r.t V_A		96(N+1)+2	–	–	t_{CLK}
Vertical section						
INPUT SIGNALS (PIN 12) (V_A)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{12}	input current	V_{12} < 5.5 V	–	–	±10	µA
t_r; t_f	rise and fall times		0	–	$t_{LLC}/2$	t_{CLK}
t_{WH}	pulse width HIGH		2	–	–	t_{CLK}
t_{WL}	pulse width LOW		2	–	–	t_{CLK}
t_{WH}	pulse width HIGH	de-interlace mode	0.5	–	–	t_{line}
t_{WL}	pulse width LOW	de-interlace mode	0.5	–	–	t_{line}
VERTICAL PLACE GENERATOR (N = VERTICAL START–SCAN DATA)						
CR	control range		1	N+1	64	t_{CLK} x 432
		K = 432	1	–	64	lines
	number of steps		–	63	–	
$Lines_{max}$	maximum number of synchronized lines per scan		–	910	–	lines/scan
f_{eq}	equivalent field frequency at 910 lines/scan	f_H = 15625 Hz	–	17.2	–	Hz
		f_H = 31250 Hz	–	34.4	–	Hz
$Lines_{min}$	minimum number of synchronized lines per scan		–	200	–	lines/scan
f_{eq}	equivalent field frequency at 200 lines/scan	f_H = 15625 Hz	–	78	–	Hz
		f_H = 31250 Hz	–	156	–	Hz
CA	amplitude control		–	automatic	–	
CA_g	amplitude control guardband	GBS = 0	–	16/12	–	lines
		GBS = 1	–	48/12	–	lines
	setting time		1	1.5	2	fields

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL GEOMETRY PROCESSING						
$I_{diff(p-p)}$	vertical output differential current (peak-to-peak value)	I_8 = −100 µA	0.96	1.0	1.04	mA
D/ΔT	drift over temperature range		–	10^{-4}	–	
	amplitude error due to S-correction setting		–	tbf	–	%
I_{bias}	vertical output signal bias current		–	−300	–	µA
I_{os}	vertical output offset current		–	–	tbf	µA
OS/ΔT	offset over temperature range		–	–	tbf	µA/K
$V_{10, 11}$	vertical output voltage range		0	–	3.9	V
CMRR	common mode rejection ratio		–	tbf	–	dB
LE	linearity error		–	0.2	2.0	%
Vertical amplitude (N = vertical amplitude data)						
CR	control range		80	–	120	%
	number of steps		–	63	–	
Vertical S-correction (N = S-correction data)						
CR	control range		0	–	16	%
	number of steps		–	63	–	
Vertical shift						
CR	control range		−2	–	+2	%
	number of steps		–	7	–	
EW OUTPUT (PIN 6)						
V_6	output voltage range		0.5	–	5.5	V
I_6	output current range	I_8 = −100 µA	0	–	1000	µA
EW width/width ratio						
CR	control range		100	–	80	%
I_{eq}	equivalent output current		0	–	400	µA
	number of steps		–	63	–	
EW parabola/width ratio						
CR	control range		0	–	20	%
I_{eq}	equivalent output current	width = 100% width = 80%	0 0	– –	400 320	µA µA
	number of steps		–	63	–	
EW corner/EW parabola ratio (note 3)						
CR	control range		−46	–	0	%
I_{eq}	equivalent output current	width = 100% width = 80%	0 0	– –	184 147	µA µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	number of steps		–	63	–	
EW corner/EW parabola ratio (note 3)						
CR	control range		–46	–	0	%
I_{eq}	equivalent output current	width = 100% width = 80%	0 0	– –	184 147	µA µA
	number of steps		–	63	–	
EW trapezium correction						
	EW trapezium/width ratio		–4	–	+4	%
	number of steps		–	7	–	
EHT INPUT (PIN 7)						
V_{ref}	reference voltage	BLDS = 1 BLDS = 0	– –	3.9 V_{CC}	– –	V V
V_I	input voltage range w.r.t V_{ref}	BLDS = 1	–20	–	+20	%
V_I	input voltage range w.r.t V_{CC}	BLDS = 0	–	0	$-2V_{ref}$	V
m_{scan}	scan modulation range		–10	0	–9.7	
m_{GC}	modulation gain control		0	–	1	
	number of steps		–	63	–	
V_7	flash detection level		–	550	–	mV
H	flash detection level hysteresis		400	–	–	mV
I_7	input current		–	–	±100	nA
RCONV INPUT (PIN 8)						
V_O	output voltage		3.7	3.9	4.1	V
I_8	current range		–50	–100	–100	µA
PROT INPUT (PIN 3)						
V_I	input voltage		0	–	V_{CC}	V
V_3	voltage detection level		3.8	4.0	4.2	V
I_I	input current		–	–	±10	µA

Notes to the characteristics

1. When f_{CLK} = 13.5 MHz, an increase of 10 mA in supply current should be expected.
2. When the prescaler is ON, one in two LLC HIGH periods is omitted.
3. The value of –46% corresponds with data 3F Hex and implies maximum 4th order.

TEST AND APPLICATION INFORMATION

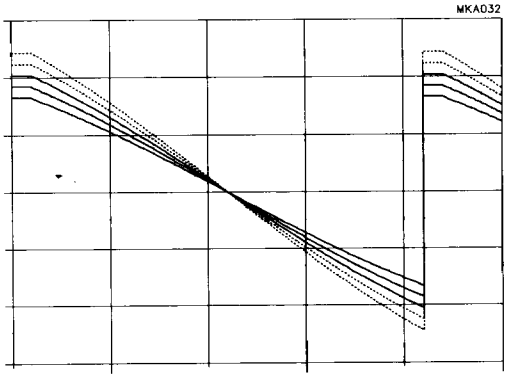


Fig.13 Control range amplitude.

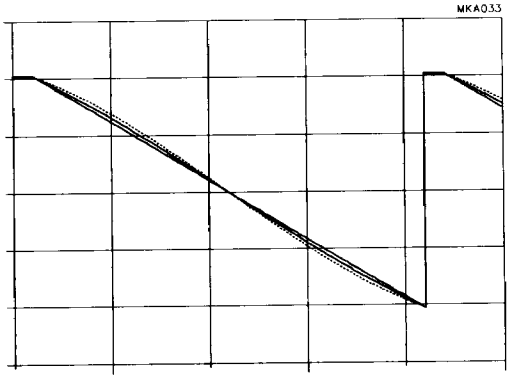


Fig.14 Control range S-correction.

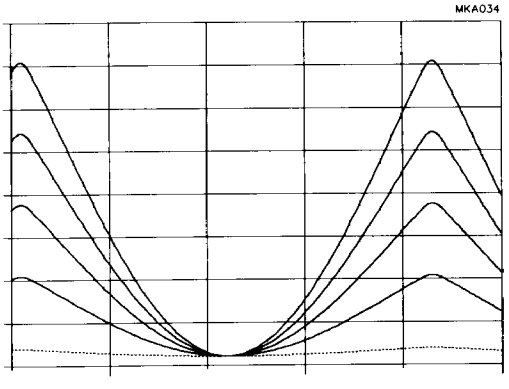


Fig.15 Control range EW parabola/width ratio.

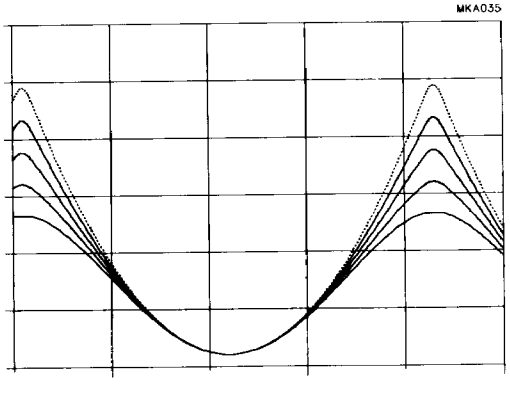


Fig.16 Control range EW corner/EW parabola ratio.

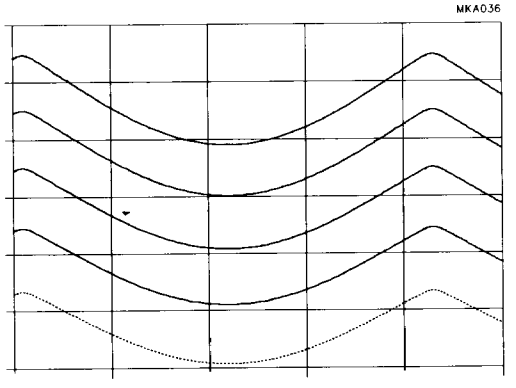


Fig.17 Control range EW width.

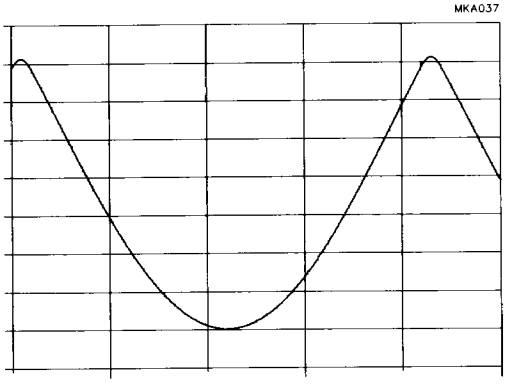


Fig.18 The BULT makes the EW waveform continuous.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PACKAGE OUTLINE

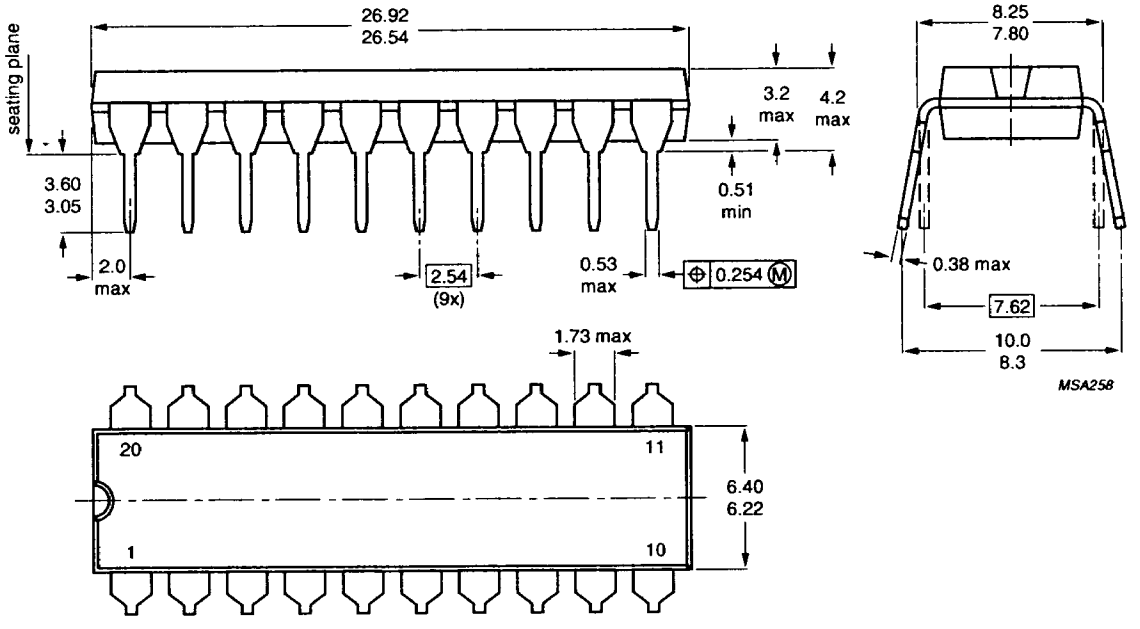


Fig.19 20-lead dual in-line; plastic (SOT146).

SOLDERING

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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