

## Features

1 Meg x 16 bit CMOS Dynamic  
Random Access Memory

- Access Times: 60 and 70ns
  - EDO Cycle time 25 and 30ns
  - Single +3.3V ( $\pm 10\%$ ) Supply Operation
  - 1024 cycles/16ms Refresh
  - RAS-Only,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ , and  
HIDDEN refresh capability
  - Low Operating Power Dissipation
  - Low Standby Power
  - Common I/O
  - All Inputs/Outputs TTL Compatible
- Package Style
- 44/50 pin Plastic TSOP
  - 42 pin Plastic SOJ

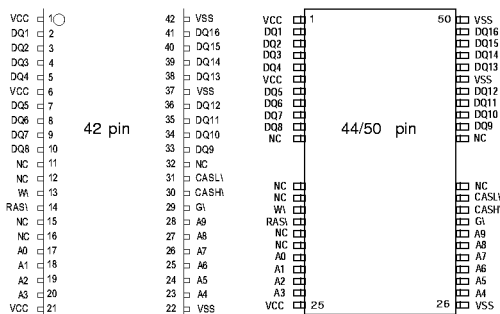
## 1 Megabit x 16 Dynamic RAM 3.3V, Extended Data Out

EDI's ruggedized plastic 1Mx16 DRAM allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on EDI's fully compliant DRAMs. EDI fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. Users of EDI's ruggedized plastic benefit from EDI's extensive experience in characterizing DRAMs for use in military systems.

The x16 width of the memory allows the user to build a cost effective x64 wide main memory array for the Power PC microprocessor. The wider memory width provides for a higher memory bandwidth required by today's systems.

## Pin Configurations



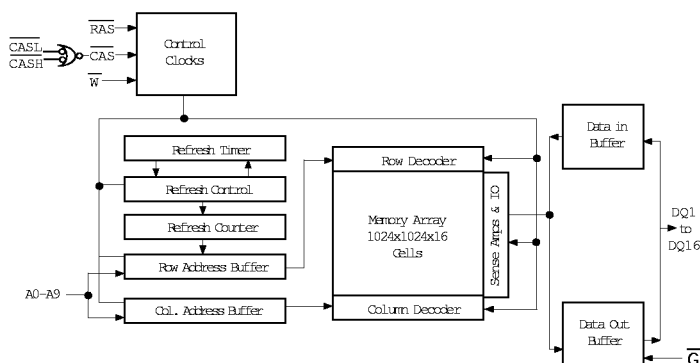
## Pin Names

|                                                       |                         |
|-------------------------------------------------------|-------------------------|
| A0-A9                                                 | Address Inputs          |
| $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ | Column Address Strobe   |
| $\overline{\text{RAS}}$                               | Row Address Strobe      |
| $\overline{\text{WA}}$                                | Write Control Input     |
| $\overline{\text{G}}$                                 | Output Enable           |
| DQ1-DQ16                                              | Data Inputs/Outputs     |
| VCC                                                   | Power (+5V $\pm 10\%$ ) |
| VSS                                                   | Ground                  |
| NC                                                    | No Connection           |

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## Block Diagram



## Absolute Maximum Ratings\*

|                                    |                   |
|------------------------------------|-------------------|
| Voltage on any pin relative to VSS | -1.0V to 5.5V     |
| Operating Temperature TA (Ambient) |                   |
| Industrial                         | -40 °C to +85 °C  |
| Military                           | -55 °C to +125 °C |
| Storage Temperature                | -65 °C to +125 °C |
| Power Dissipation                  | 1 Watt            |
| Output Current                     | 50 mA             |

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

Note 1

| Parameter          | Sym | Min  | Typ | Max | Units |
|--------------------|-----|------|-----|-----|-------|
| Supply Voltage     | VCC | 3.0  | 3.3 | 3.6 | V     |
| Supply Voltage     | VSS | 0    | 0   | 0   | V     |
| Input High Voltage | VIH | 2    | --  | 5.5 | V     |
| Input Low Voltage  | VIL | -1.0 | --  | 0.8 | V     |

Notes: 1. All voltage values are with respect to VSS.

## Electrical Characteristics

(VCC = 5.0V ±10%) Note 2.

| Parameter                                                       | Sym  | Conditions                                            | Min | Typ | Max | Units |
|-----------------------------------------------------------------|------|-------------------------------------------------------|-----|-----|-----|-------|
| Average Supply Current from VCC Operating (Notes 3, 4)          | ICC1 | RAS\, CAS\ Cycling<br>TRC = TWC = Min, Output Open    |     |     | 170 | mA    |
| Supply Current from VCC Standby                                 | ICC2 | RAS\ = CAS\ = W\ = VIH, Outputs Open                  |     |     | 2   | mA    |
|                                                                 | ICC5 | RAS\ = CAS\ = W\ = VCC-0.2, Outputs Open              |     |     | 1   | mA    |
| Average Supply Current from VCC Refreshing (Note 3)             | ICC3 | RAS\, CAS\ Address Cycling<br>TRC = Min, Outputs Open |     |     | 150 | mA    |
| Average Supply Current from VCC EDO Page Mode (Notes 3, 4)      | ICC4 | RAS\ = VIL, CAS\ = Cycling<br>TPC = Min, Outputs Open |     |     | 120 | mA    |
| Average Supply Current from VCC RAS\ Only Refresh Mode (Note 3) | ICC6 | CAS\ before RAS\ Refresh Cycling                      |     |     | 160 | mA    |
| CAS\ before RAS\ Refresh Mode (Note 3)                          |      | TRC = Min, Outputs Open                               |     |     |     |       |
| Input Current                                                   | IIL  | 0V - VIN - 6.5V<br>All Other Input Pins = 0V          | -2  |     | 10  | µA    |
| Off-State Output Current                                        | IOZ  | Q Floating 0V - V OUT - 5.5V                          | -10 |     | 2   | µA    |
| Output High Voltage                                             | VOH  | IOH = -2.0mA                                          | 2.4 | --  | VCC | V     |
| Output Low Voltage                                              | VOL  | IOL = 2.2mA                                           | 0   | --  | 0.4 | V     |

Notes: 2. Current flowing into an IC is positive, out is negative.

3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

## EDI4161MEV-RP

1Megx16 EDODRAM

**Capacitance**

(f=1.0MHz, VIN=VCC or VSS)

| Parameter                       | Sym        | Test Conditions                  | Min | Typ | Max | Unit |
|---------------------------------|------------|----------------------------------|-----|-----|-----|------|
| Address Input Capacitance       | CA         | VI = VSS                         |     |     | 5   | pF   |
| Input Capacitance (D)           | CD         | f = 1MHz                         |     |     | 7   | pF   |
| Input Capacitance (CAS, W, RAS) | CC, CW, CR | Vi = 25mVrms                     |     |     | 7   | pF   |
| Output Capacitance (Q)          | CQ         | VO = VSS, f = 1MHz, Vi = 25mVrms |     |     | 7   | pF   |

**Input Conditions for Each Mode**

The ED14161MEV provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g. Extended Data Out, RAS-only Refresh, and Delayed Write. The input conditions for each are shown below.

ACT = Active  
NAC = Non-active  
DNC = Don't care  
VLD = Valid  
APD = Applied  
OPN = Open

| Operation              | Inputs |     |     |     | Row Address | Column Address | Input/Output |     |
|------------------------|--------|-----|-----|-----|-------------|----------------|--------------|-----|
|                        | RAS    | CAS | W   | G   |             |                | D            | Q   |
| Read*                  | ACT    | ACT | NAC | ACT | APD         | APD            | OPN          | VLD |
| Early Write*           | ACT    | ACT | ACT | DNC | APD         | APD            | VLD          | OPN |
| Read-Modify-Write*     | ACT    | ACT | ACT | ACT | APD         | APD            | VLD          | VLD |
| RAS-only Refresh       | ACT    | NAC | DNC | DNC | APD         | DNC            | DNC          | OPN |
| Hidden Refresh         | ACT    | ACT | DNC | ACT | APD         | DNC            | OPN          | VLD |
| CAS before RAS Refresh | ACT    | ACT | NAC | DNC | DNC         | DNC            | DNC          | OPN |
| Standby                | NAC    | DNC | DNC | DNC | DNC         | DNC            | DNC          | OPN |

\*Extended Data Out Mode Identical.

## Timing Requirements

### Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(VCC=3.3V±10%) Note 1,2,5,11,12

| Parameter                                 | Sym  | 60ns |        | 70ns |        | Unit | Notes  |
|-------------------------------------------|------|------|--------|------|--------|------|--------|
|                                           |      | Min  | Max    | Min  | Max    |      |        |
| Random Read or Write Cycle Time           | TRC  | 105  |        | 125  |        | ns   |        |
| Read-Modify-Write Cycle Time              | TRWC | 145  |        | 170  |        | ns   |        |
| Access Time from CAS\                     | TCAC |      | 15     |      | 20     | ns   | 3,4,5  |
| Access Time from RAS\                     | TRAC |      | 60     |      | 70     | ns   | 3,4,10 |
| Access Time From Column Address           | TAA  |      | 30     |      | 35     | ns   | 3,10   |
| CAS to output in Low-Z                    | TCLZ | 0    |        | 0    |        | ns   | 6      |
| Output buffer turn-off delay              | TOFF | 3    | 15     | 3    | 15     | ns   | 6,14   |
| Transition Time                           | TT   | 2    | 50     | 2    | 50     | ns   | 2      |
| RAS\ Precharge Time                       | TRP  | 40   |        | 50   |        | ns   |        |
| RAS\ Low Pulse Width                      | TRAS | 60   | 10,000 | 70   | 10,000 | ns   |        |
| RAS\ Hold Time after CAS\ Low             | TRSH | 13   |        | 15   |        | ns   |        |
| CAS\ Hold Time after RAS\ Low             | TCSH | 50   |        | 55   |        | ns   |        |
| CAS\ Low Pulse Width                      | TCAS | 12   | 10,000 | 13   | 10,000 | ns   |        |
| RAS\ to CAS\ Delay Time                   | TRCD | 14   | 45     | 14   | 50     | ns   | 4      |
| Column Address Delay from RAS\ Low        | TRAD | 12   | 30     | 12   | 35     | ns   | 10     |
| Delay CAS\ High to RAS\ Low               | TCRP | 5    |        | 5    |        | ns   |        |
| Row Address Set Up Time                   | TASR | 0    |        | 0    |        | ns   |        |
| Row Address Hold Time                     | TRAH | 10   |        | 10   |        | ns   |        |
| Column Address Set Up Time                | TASC | 0    |        | 0    |        | ns   |        |
| Column Address Hold Time                  | CAH  | 10   |        | 12   |        | ns   |        |
| Column Address Hold Time Referenced RAS   | TAR  | 45   |        | 50   |        | ns   |        |
| Column Address to RAS\ Setup              | TRAL | 30   |        | 35   |        | ns   |        |
| Read Set Up Time before CAS\ Low          | TRCS | 0    |        | 0    |        | ns   |        |
| Read Hold Time after CAS\ High            | TRCH | 0    |        | 0    |        | ns   | 8      |
| Read Hold Time after RAS\ High            | TRRH | 0    |        | 0    |        | ns   | 8      |
| Write Hold Time after CAS\ Low            | TWCH | 10   |        | 12   |        | ns   |        |
| Write Command Hold Time Referenced to RAS | TWCR | 45   |        | 55   |        | ns   |        |
| Write Pulse Width                         | TWP  | 10   |        | 12   |        | ns   |        |
| RAS\ Hold Time after Write Low            | TRWL | 15   |        | 15   |        | ns   |        |
| CAS\ Hold Time after Write Low            | TCWL | 15   |        | 15   |        | ns   |        |
| Data Setup Time                           | TDS  | 0    |        | 0    |        | ns   | 9      |
| Data Hold Time after CAS\ Low             | TDH  | 10   |        | 12   |        | ns   | 9      |
| Data Hold Time Referenced to RAS          | TDHR | 45   |        | 55   |        | ns   |        |
| Refresh Cycle                             | TREF |      | 16     |      | 16     | ns   |        |
| Write Setup Time before CAS\ Low          | TWCS | 0    |        | 0    |        | ns   | 7      |
| CAS\ Low to W\ Low Delay                  | TCWD | 35   |        | 40   |        | ns   | 7      |
| RAS\ Low to W\ Low Delay                  | TRWD | 80   |        | 90   |        | ns   | 7      |
| Column Address Setup to CAS High          | TACH | 15   |        | 15   |        | ns   |        |
| G\ Low to Output Valid                    | TOE  |      | 15     |      | 20     | ns   | 13     |
| CAS Low to DOUT                           | TCOH | 3    |        | 3    |        | ns   |        |
| RAS Low to W Low                          | TWRH | 10   |        | 10   |        | ns   |        |
| Write High to RAS Low                     | TWRP | 10   |        | 10   |        | ns   |        |
| Address to W\ Low Delay                   | TAWD | 55   |        | 60   |        | ns   | 7      |

**Write Cycle, Early and Delayed Write**

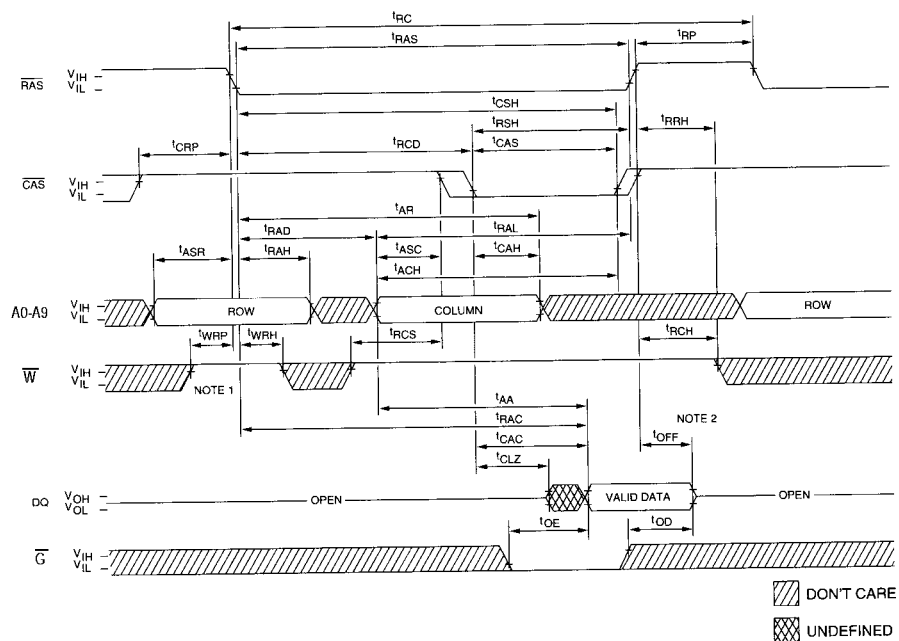
(VCC = 5.0V±10%) Notes 1,2,5,11,12

| Parameter                                                | Sym     | 60ns |      | 70ns |      | Unit | Notes |
|----------------------------------------------------------|---------|------|------|------|------|------|-------|
|                                                          |         | Min  | Max  | Min  | Max  |      |       |
| CAS\Setup for CAS\before RAS\Refresh                     | TCSR    | 5    |      | 5    |      | ns   |       |
| CAS\Hold for CAS\before RAS\Refresh                      | TCHR    | 10   |      | 12   |      | ns   |       |
| Precharge to CAS\Active                                  | TRPC    | 5    |      | 5    |      | ns   |       |
| Access Time from CAS\Precharge                           | TCPA    |      | 35   |      | 40   | ns   | 3     |
| EDO Page Cycle Time                                      | TPC     | 25   |      | 30   |      | ns   |       |
| EDO Page Read-Modify-Write Cycle Time                    | TPRWC75 |      | 85   |      |      | ns   |       |
| CAS precharge time (EDO cycle)                           | TCP     | 10   |      | 10   |      | ns   |       |
| RAS pulse width (EDO Cycle)                              | TRASP   | 60   | 125K | 70   | 125K | ns   |       |
| RAS Hold Time From CAS Precharge                         | TRHCP   | 35   |      | 40   |      | ns   |       |
| Output Disable Time after $\bar{G}$ High                 | TOD     | 0    | 15   | 0    | 15   | ns   | 6     |
| Write Low to Next $\bar{G}$ Low                          | TOEH    | 12   |      | 12   |      | ns   |       |
| $\bar{G}$ Low to $\bar{C}$ AS High Setup Time            | TOES    | 5    |      | 5    |      | ns   |       |
| $\bar{G}$ High Hold From $\bar{C}$ AS High               | TOEHC   | 10   |      | 10   |      | ns   |       |
| OE High Pulse Width                                      | TOEP    | 10   |      | 10   |      | ns   |       |
| $\bar{G}$ Setup prior to RAS during Hidden Refresh Cycle | TORD    | 0    |      | 0    |      | ns   |       |
| $\bar{G}$ delay from $\bar{W}$                           | TWHZ    | 0    | 13   | 0    | 15   | ns   |       |
| $\bar{W}$ pulse to disable at $\bar{C}$ AS high          | TWPZ    | 10   |      | 12   |      | ns   |       |

**Notes:**

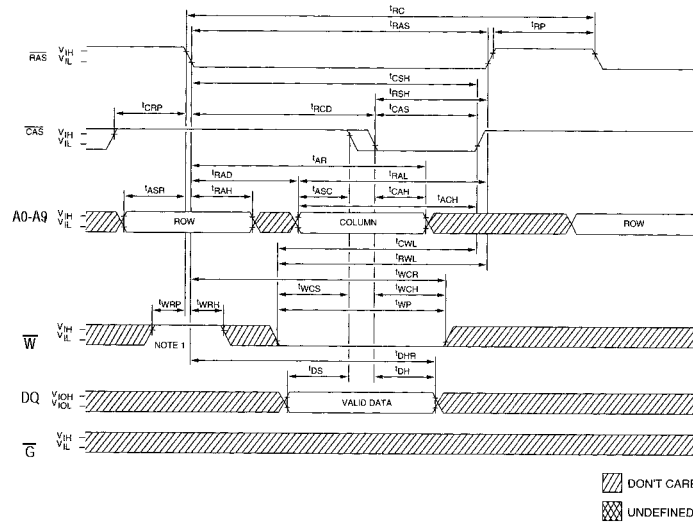
1. An initial pause of 100 $\mu$ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved, and must be repeated whenever TREF is exceeded.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 3ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the TRCD (max) limit insures that TRAC (max) can be met. TRCD (max) is specified as a reference point only. If TRCD is greater than the specified TRCD(max) limit, then access time is controlled exclusively by TCAC.
5. Assumes that TRCD>TRCD (max)
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. TWCS, TRWD, TCWD and TAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If TWCS>TWCS(min), the cycle is an early write and the data output will remain high impedance for the duration of the cycle. If TCWD>TCWD(min), TRWD>TRWD(min) and TAWD>TAWD(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either TRCH or TRRH must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles and to the  $\bar{W}$  leading edge in read-modify-write cycles.
10. Operation within the TRAD(max) limit insures that TRAC(max) can be met. TRAD (max) is specified as a reference point only. If TRAD is greater than the specified TRAD(max) limit, then access time is controlled by TAA.
11. 1024 (1K Ref.) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
12. TAR, TWCR, and TDHR are referenced to TRAD (max).
13. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally,  $\bar{W}$ E must be pulsed during CAS HIGH time in order to place I/O buffers in High Z.
14. TOFF (MAX) defines the time at which the output achieves the open circuit conditions, and is not referenced to VOH or VOL. It is referenced from the rising edge of RAS or CAS, whichever occurs last.

## Read Cycle



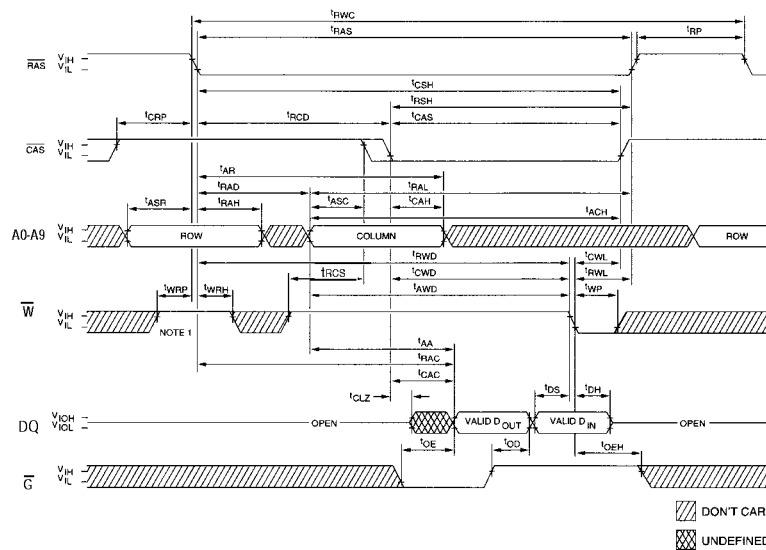
- Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for  $t_{WRP}$  and  $t_{WRH}$ . The design implementation will facilitate compatibility with future EDO DRAMs.  
2.  $t_{OFF}$  is referenced from rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

### Write Cycle, Early Write



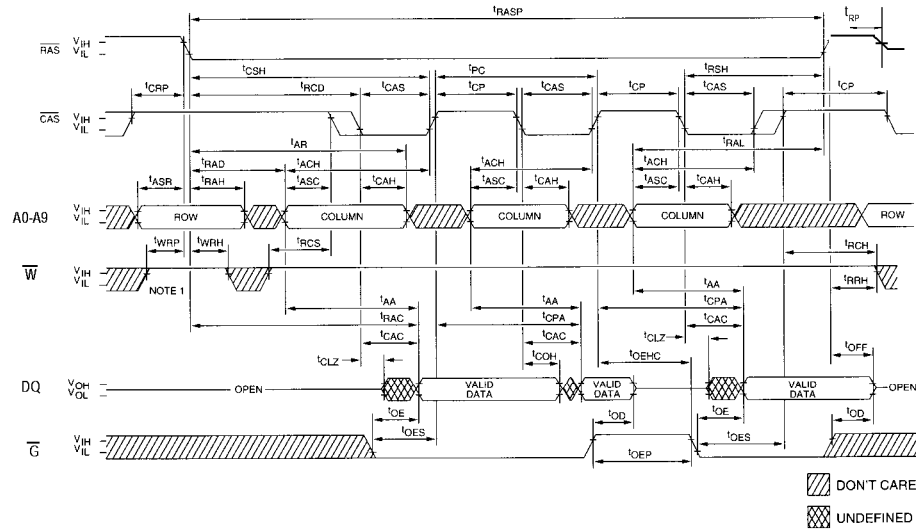
Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

### Read Write Cycle Late Write and Read-Modify-Write Cycles



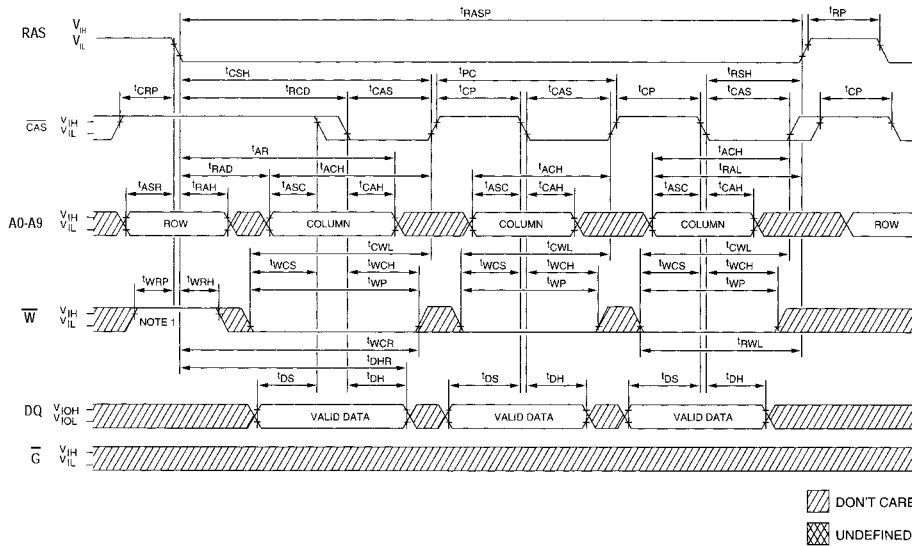
Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

## EDO-Page-Mode Read Cycle



Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

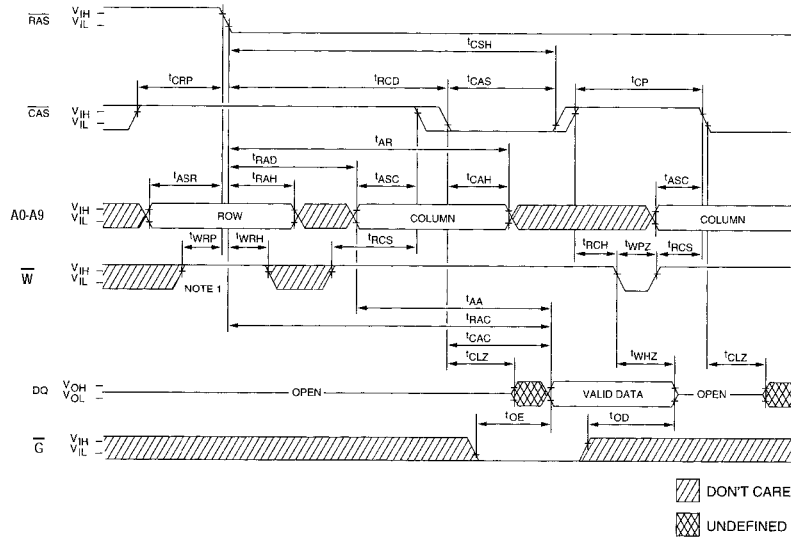
## EDO-Page-Mode Early Write Cycle



Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

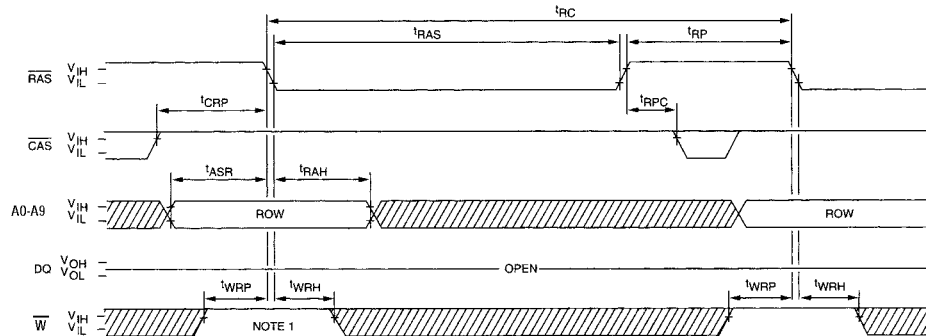


## Read Cycle with WE Controlled Disable



Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

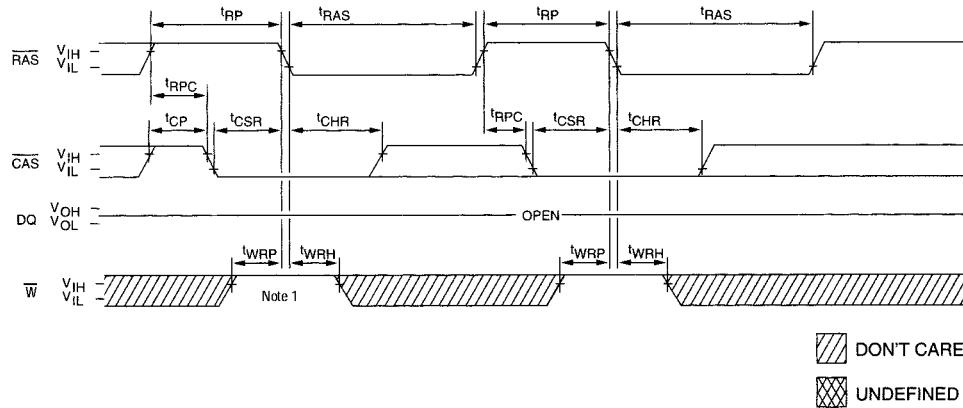
## RAS-Only Refresh Cycle



Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

### CBR Refresh Cycle

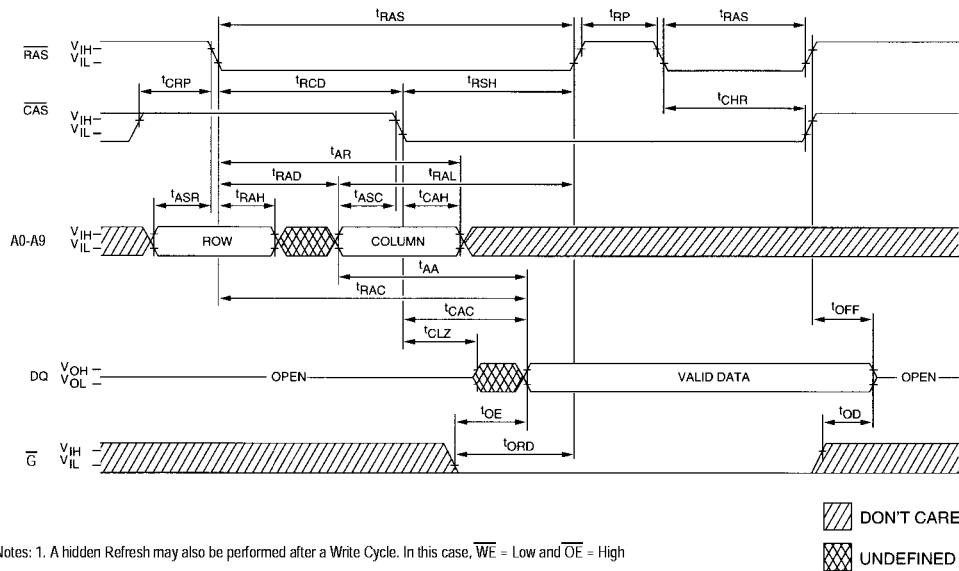
(A0-A9 and  $\overline{G}$ =Don't Care)



Notes: 1. Although  $\overline{W}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (Read or Write), the system designer should implement  $\overline{W}$  high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

### Hidden Refresh Cycle

( $\overline{W}$ =High,  $\overline{G}$ =Low) Note 1



Notes: 1. A hidden Refresh may also be performed after a Write Cycle. In this case,  $\overline{WE}$  = Low and  $\overline{OE}$  = High

## Ordering Information

### MILITARY (-55 °C TO +125 °C)

| Part No.       | Speed (ns) | Package No. |
|----------------|------------|-------------|
| EDI4161MEV60SM | 60         | 371         |
| EDI4161MEV70SM | 70         | 371         |
| EDI4161MEV60MM | 60         | 420         |
| EDI4161MEV70MM | 70         | 420         |

### INDUSTRIAL (-40 °C TO +85 °C)

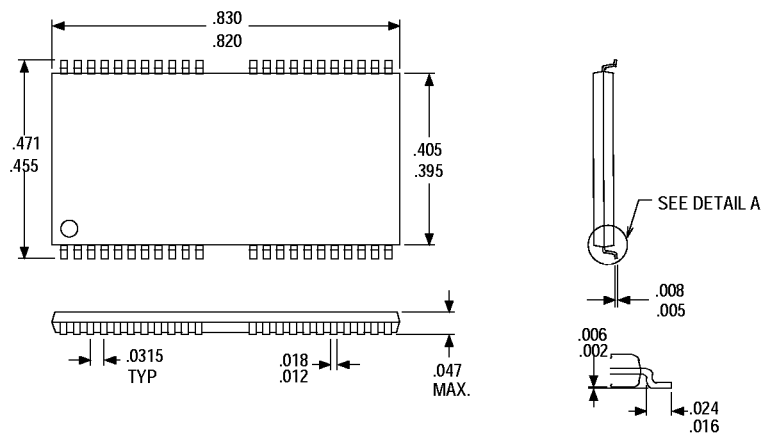
| Part No.       | Speed (ns) | Package No. |
|----------------|------------|-------------|
| EDI4161MEV60SI | 60         | 371         |
| EDI4161MEV70SI | 70         | 371         |
| EDI4161MEV60MI | 60         | 420         |
| EDI4161MEV70MI | 70         | 420         |

## Package Description

### Package No. 371

#### 44/50 Pin

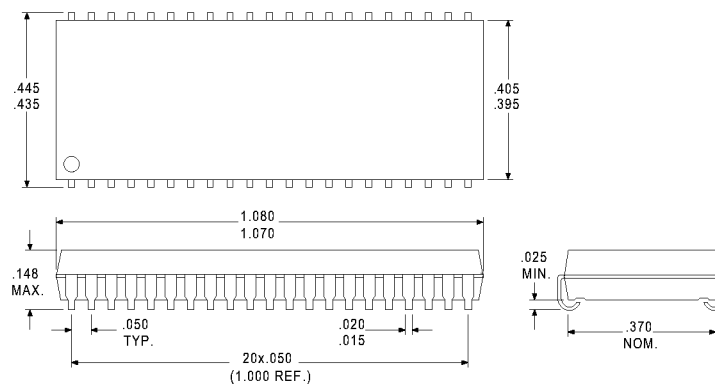
#### Plastic TSOP



### Package No. 420

#### 42 Pin

#### Plastic SOJ



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