HM66205L Series

524,288-word × 8-bit High Density CMOS Static RAM Module

The HM66205L is a high density 4-Mbit static RAM module which consists of 4 pieces HM628128LT products (TSOP type 1M static RAM) and a HD74ACT138FP equivalent product (SOP type CMOS decoder logic).
An outline of the HM66205L is the standard 600-mil width 32-pin dual-in-line package. Its pin arrangement is completely compatible with 4-Mbit monolithic static RAM.
The HM66205L offers the features of low power and high speed by using high speed CMOS devices. And, the HM66205L makes high density mounting possible without surface mount technology.
These features make the HM66205L ideally suited for high density compacted memory systems.

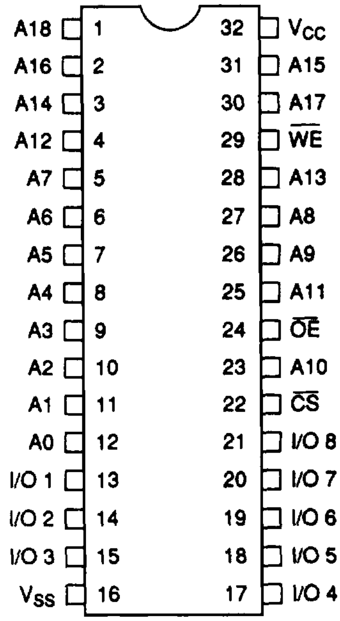
Features

- High density 32-pin DIP
  - Mounting 4 pcs. of 1M static RAM (TSOP; HM628128LT) and CMOS decoder logic (SOP; HD74ACT138FP equivalent)
- Pin compatible with 4M monolithic static RAM
- High speed
  - Fast access time: 85 ns/100 ns/120 ns (max)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby: 40 µW (typ)
  - Operation: 80 mW (typ)
- Comon data input and output, three state outputs
- Capable of battery backup operation
- Directry TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM66205L-85	85 ns	600-mil 32-pin DIP
HM66205L-10	100 ns	
HM66205L-12	120 ns	

Pin Arrangement

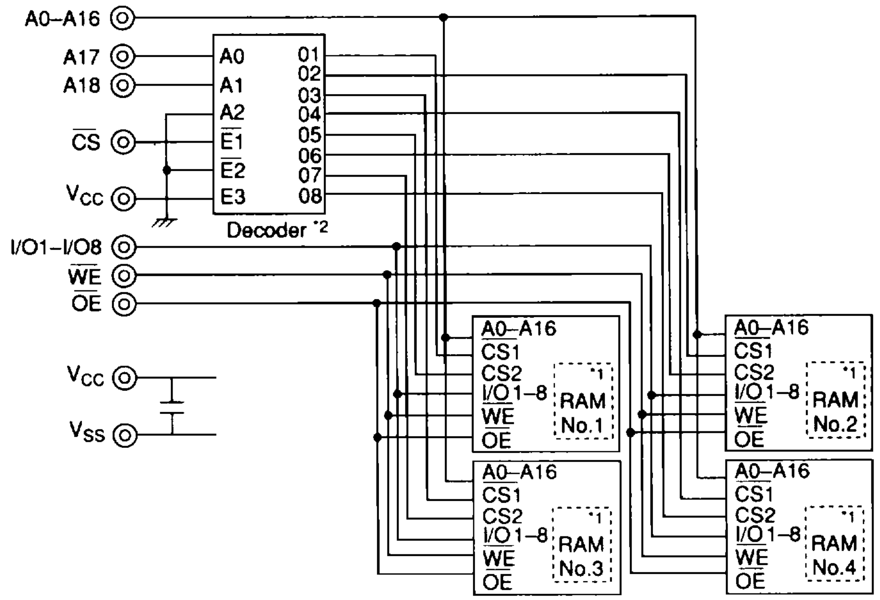


(Top view)

Pin Description

Pin name	Function
A0 – A18	Address
I/O1 – I/O8	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Notes: 1. RAM No.1–No. 4: HM628128LT
2. CMOS Decoder: HD74ACT138FP

Truth Table

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Ref. cycle
Not selected (Power down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note: X = Don't care (H or L)

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.3[*1]	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions
Input leakage currentent	$\lvert I_{LI} \rvert$	—	—	8	µA	Vin = V_{SS} to V_{CC}
Output leakage currentent	$\lvert I_{LO} \rvert$	—	—	8	µA	$\overline{\mathrm{CS}} = V_{IH}$, $\overline{\mathrm{OE}} = V_{IH}$ or $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current: DC	I_{CC}	—	19	46	mA	$\overline{\mathrm{CS}} = V_{IL}$, others V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
Average operating power supply current (1)	I_{CC1}	—	48	89	mA	Min cycle, duty = 100% $\overline{\mathrm{CS}} = V_{IL}$, $I_{I/O}$ = 0 mA, others V_{IH}/V_{IL}
Average operating power supply current (2)	I_{CC2}	—	16	36	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{\mathrm{CS}} \le 0.2$ V, $V_{IH} = V_{CC} - 0.2$ V, $V_{IL} \le 0.2$ V
Standby power supply current: DC	I_{SB}	—	4	12	mA	$\overline{\mathrm{CS}} = V_{IH}$
Standby power supply current (1)	I_{SB1}	—	8	400	µA	Vin ≥ 0 V $\overline{\mathrm{CS}} = V_{CC} - 0.2$
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions	Notes
Input capacitance (1)	Cin1	—	45	pF	Vin = 0 V	A0 – A16, WE, OE
Input capacitance (2)	Cin2	—	45	pF	Vin = 0 V	A17 – A18, CS
Input/output capacitance	$C_{I/O}$	—	50	pF	$V_{I/O}$ = 0 V	I/O1 – I/O8

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

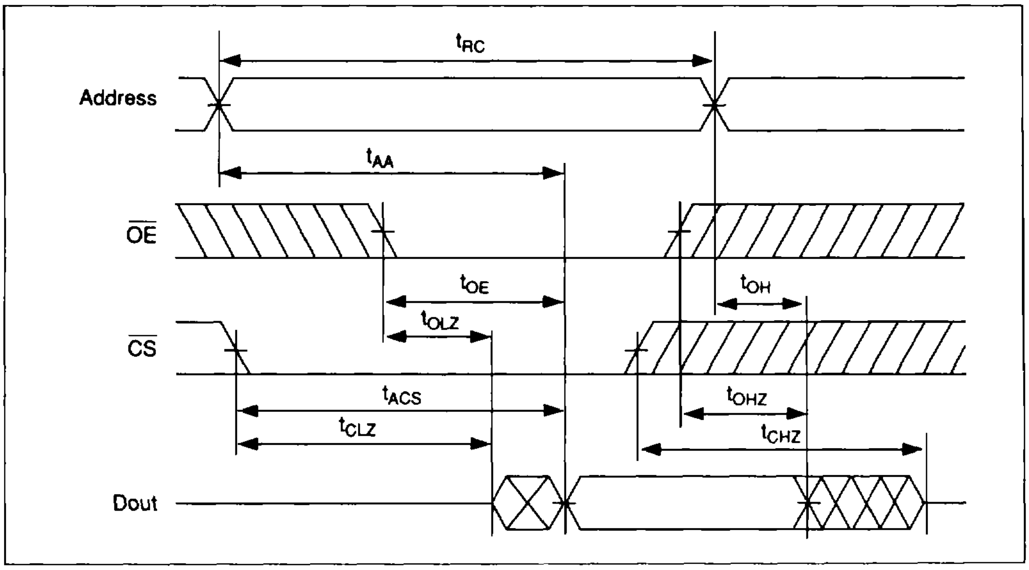
Test Condition

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5 V
- Output load: 1 TTL Gate and CL = 100 pF (Including scope and jig)

Read Cycle

		HM66205L-85		HM66205L-10		HM66205L-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	85	—	100	—	120	ns
Chip select access time	t_{ACS}	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	45	—	50	—	60	ns
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	ns
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	45	ns
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	45	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns

Read Timing Waveform (1) *1



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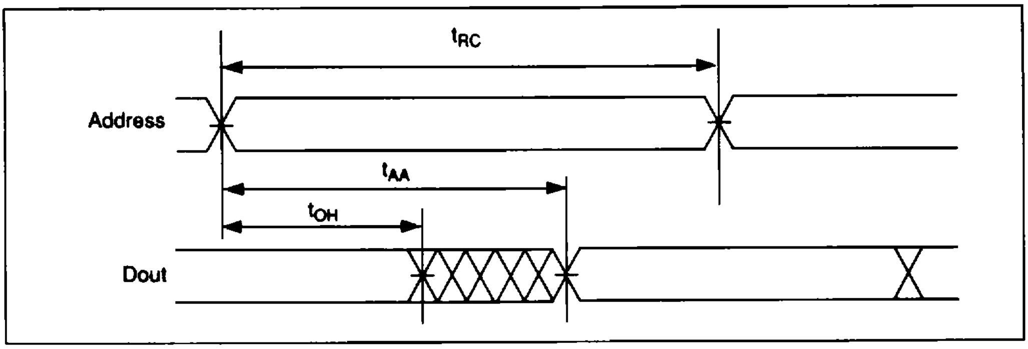
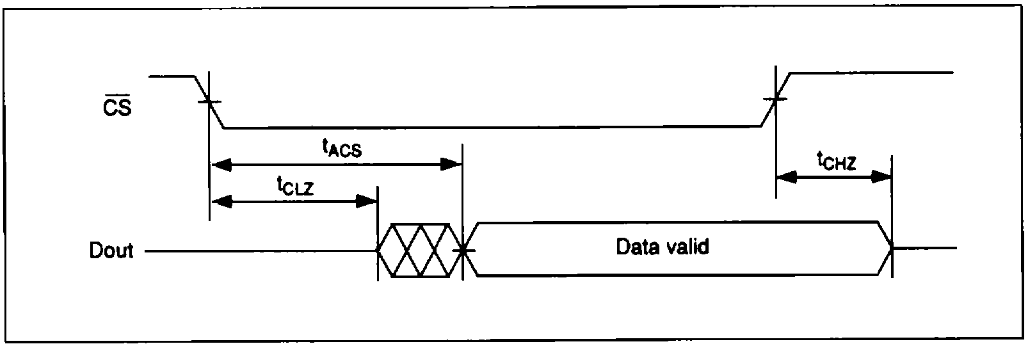
Read Timing Waveform (2) *1, *2, *4



Read Timing Waveform (3) *1, *3, *4

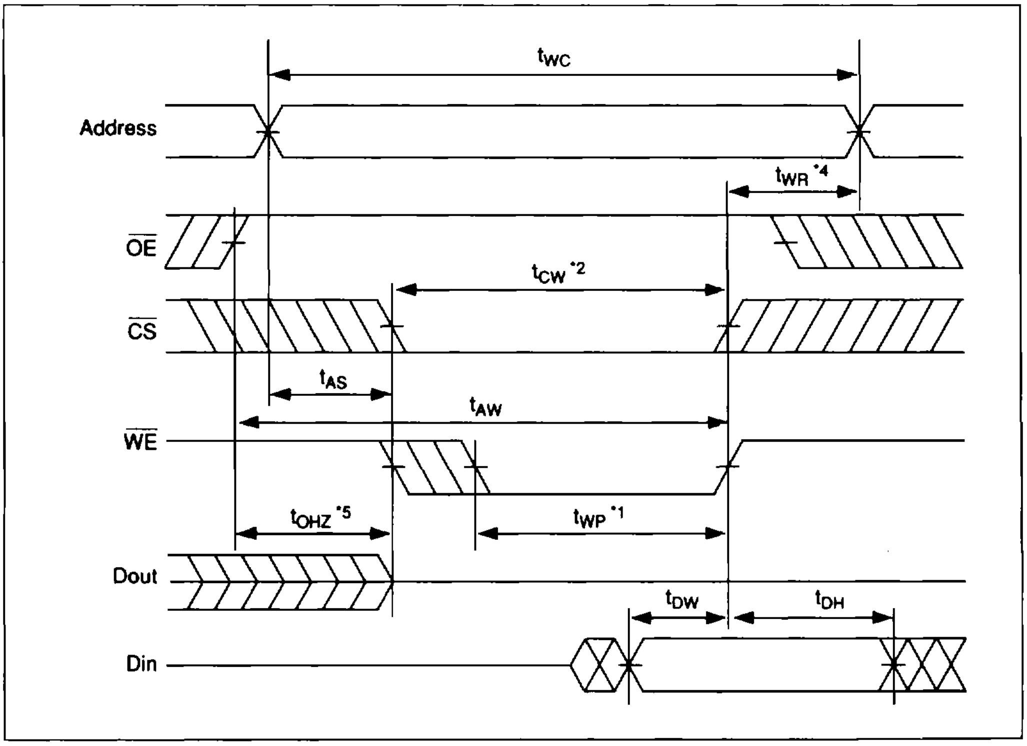


Notes:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address should be valid prior to or coinsident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}

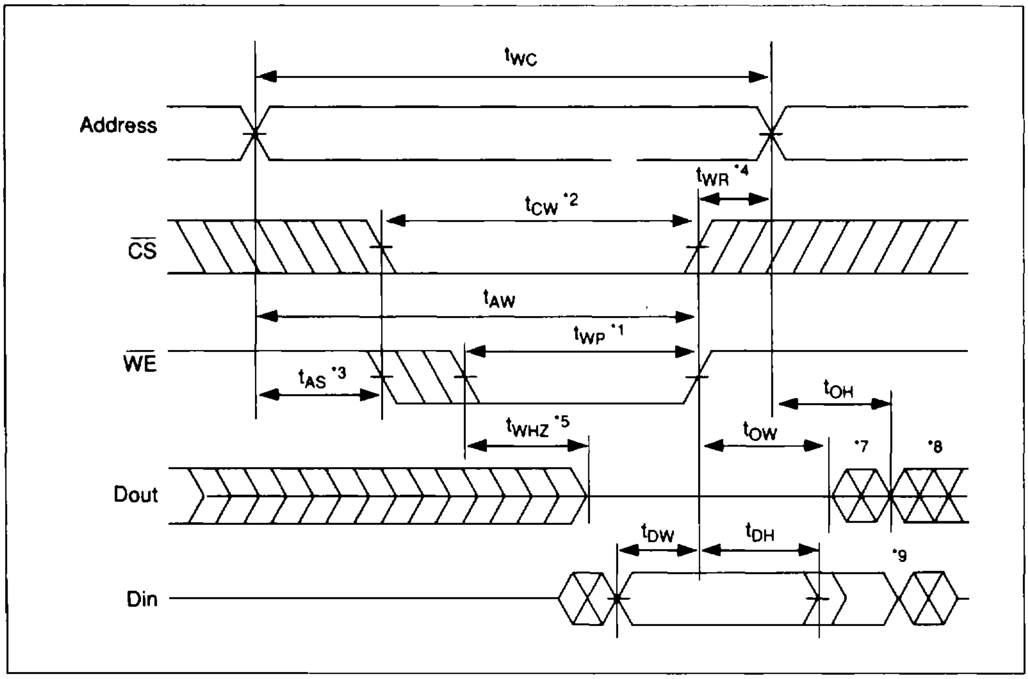
Write Cycle

Parameter	Symbol	HM66205L-85 Min	HM66205L-85 Max	HM66205L-10 Min	HM66205L-10 Max	HM66205L-12 Min	HM66205L-12 Max	Unit
Write cycle time	t_{WC}	85	—	100	—	120	—	ns
Chip selection to end of write	t_{CW}	75	—	90	—	100	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address valid to end of write	t_{AW}	75	—	90	—	100	—	ns
Write pulse width	t_{WP}	65	—	75	—	85	—	ns
Write recovery	t_{WR}	5	—	5	—	10	—	ns
Write to output in high-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to write time overlap	t_{DW}	35	—	40	—	45	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) *5 (OE Low Fixed)

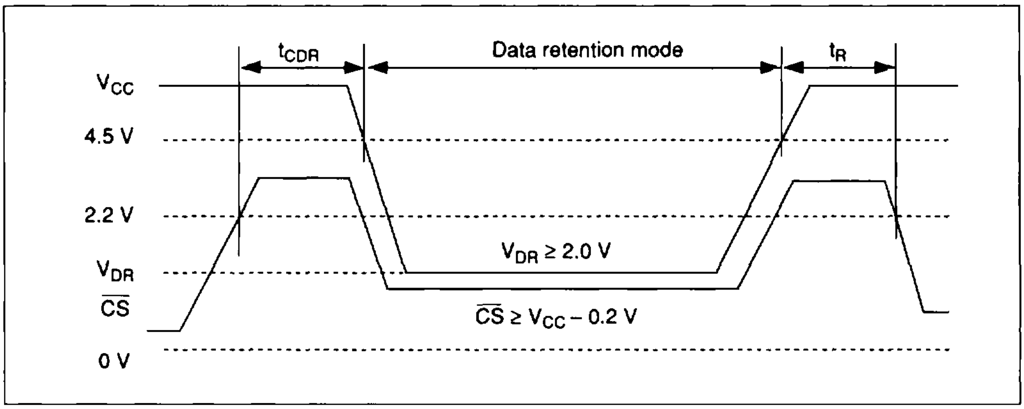


Notes:
1. A write occures during the overlap (t_{WP}) of a low CS and low WE.
2. t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state.
   The input signals out of phase must not be applied.
4. If the CS low transition occures simultaneously with the WE low transition or after the WE low transition, output remain in a high impedance state.
5. OE is continuously low. (OE = V_{IL}).
6. Dout should be held in the phase of the written data during this write cycle.
7. Dout is the read data of next address.
8. If CS is low during this period, I/O pins are in the output state.
   The input signals which are opposite to the output level should not be applied to I/O pins.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, A17•A18 $\geq V_{CC} - 0.2$ V, Vin $\geq$ 0 V
Data retention current	I_{CCDR}	—	4	200	µA	$V_{CC} = 3.0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq$ 0 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Waveform



Package Dimension

Unit: mm (inch)