

TENTATIVE

TOSHIBA SMALL FORM FACTOR CARD

**CompactFlash™ Card****DESCRIPTION**

The THNCFxxxMBA/BAI series CompactFlash™ card is a flash technology based with ATA interface flash memory card. It is constructed with flash disk controller chip and NAND-type (Toshiba) flash memory device. The CompactFlash™ card operates in both 5-Volt and 3.3-Volt power supplies. It comes in capacity of 8, 16, 32, 48, 64, 96, 128, 160, 192, 256, 320, 384 and up to 512 MB unformatted for type-I card. Emulating IDE hard disk drives and being certified in accordance with the CompactFlash™ Certification Plan it is a perfect choice of solid-state mass-storage cards for battery backup handheld devices such as Digital Camera, Audio Player, PDA, or the applications that require high environment tolerance with high performance sustained write speed.

**FEATURES**

- CompactFlash™ Compatibility
  - Certified in accordance with the CompactFlash™ Certification Plan
  - Substantially compatible with PC Card standard and PC Card ATA
  - Support for CIS implemented with 256 bytes of attribute memory
- ATA/IDE interface
  - ATA command set compatible
  - Support for 8- or 16-bit host transfers
  - Programmable and auto-wait-state generation for compatibility with any host speed using IORDY
- High performance
  - Supports PIO mode 4, both at 16.6 Mbytes/second theoretically
  - Sustained write : max 1.5 Mbytes/second (8MB to 48MB), 3.2 Mbytes/second (64MB to 512MB)
  - Sustained read : max 6.5Mbytes/second
  - Single +5 Volt or 3.3 Volt power supply and very low power consumption with automatic power management.

Notes: CompactFlash™ is a trademark of SanDisk Corporation and is licensed royalty-free to the CFA, which in turn will license it royal-free to CFA members.

CFA: CompactFlash™ Association.

**Products Models**

| unformatted | Cylinder | Head | Sector | Model No.         |
|-------------|----------|------|--------|-------------------|
| 8MB         | 248      | 2    | 32     | THNCF008MBA / BAI |
| 16MB        | 248      | 4    | 32     | THNCF016MBA / BAI |
| 32MB        | 496      | 4    | 32     | THNCF032MBA / BAI |
| 48MB        | 744      | 4    | 32     | THNCF048MBA / BAI |
| 64MB        | 978      | 4    | 32     | THNCF064MBA / BAI |
| 96MB        | 733      | 8    | 32     | THNCF096MBA / BAI |
| 128MB       | 978      | 8    | 32     | THNCF128MBA / BAI |
| 160MB       | 611      | 16   | 32     | THNCF160MBA / BAI |
| 192MB       | 733      | 16   | 32     | THNCF192MBA / BAI |
| 256MB       | 978      | 16   | 32     | THNCF256MBA / BAI |
| 320MB       | 814      | 16   | 48     | THNCF320MBA / BAI |
| 384MB       | 977      | 16   | 48     | THNCF384MBA / BAI |
| 512MB       | 993      | 16   | 63     | THNCF512MBA / BAI |

**Products Specifications**

- **Dimensions:**  
Type I card : 36.4mm(L) x 42.8mm (W) x 3.3mm (H)
- **Storage Capacities:**  
8,16, 32, 48, 64, 96,128, 160, 192, 256, 320, 384 and up to 512 MB (unformatted)
- **System Compatibility:**  
Please refer to the compatibility list.
- **Performance:**  
Supports PIO mode 4, both at 16.6 Mbytes/second theoretically  
Sustained write max 1.5 Mbyte/sec (max) in ATA PIO mode 4 (8MB to 48MB)  
Sustained write max 3.2 Mbyte/sec (max) in ATA PIO mode 4 (64MB to 512MB)  
Sustained read max 6.5 Mbyte/sec (max ) in ATA PIO mode 4
- **Operating Voltage:**  
3.3V  $\pm$  0.3V  
5.0V  $\pm$  0.5V
- **Power consumption:**
  - 5V operation  
Active mode:  
Write operation : 43 mA (Typ.)  
Read operation : 35 mA (Typ.)  
Sleep mode : 1.2mA (Typ) \*1 2.0mA (max.)
  - 3.3V operation  
Active mode:  
Write operation : 38 mA (Typ.)  
Read operation : 30 mA (Typ.)  
Sleep mode : 1.0mA (Typ) \*1 1.5mA (max.)
- **Environment conditions:**
  - Operating temperature: 0°C to 70°C (THNCFxxxMBA Series) — Commercial grade —  
-40°C to 85°C (THNCFxxxMBAI Series) — Industrial grade —
  - Storage temperature: -20°C to 85°C (THNCFxxxMBA Series) — Commercial grade —  
-45°C to 90°C (THNCFxxxMBAI Series) — Industrial grade —

**Electrical Interface**

- **Physical Description:**

The host is connected to the CompactFlash™ Storage Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

- **Pin Assignments and Pin Type:**

The signal/pin assignments are listed in Table 4. Low active signals have a “—” prefix. Pin types are Input, Output or Input/Output. Section “Electrical specification” and “DC characteristics” defines the all input and output type structures.

- **Electrical Description:**

The CompactFlash™ Storage Card functions in three basic modes: 1) PC Card ATA using I/O Mode, 2) PC Card ATA using Memory Mode and 3) True IDE Mode, which is compatible with most disk drives. CompactFlash™ Storage Cards are required to support all three modes. The CF Cards normally function in the first and second modes, however they can optionally function in True IDE mode. The configuration of the CompactFlash™ Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the storage card. Or for True IDE Mode, pin 9 being grounded. The configuration of the CF Card will be controlled using configuration registers. The configuration registers are starting at the address defined in the Configuration Tuple (CISTPL\_CONFIG) in the Attribute Memory space of the CF Card. Signals, whose source is the host, is designated as inputs while signals that the CompactFlash™ Storage Card sources are outputs. The CompactFlash™ Storage Card logic levels conform to those specified in the PC Card Standard Release 8. Each signal has three possible operating modes:

- 1) PC Card Memory mode
- 2) PC Card I/O mode
- 3) True IDE mode

True IDE mode is required for CompactFlash™ Storage cards. All outputs from the card are totem pole except the data bus signals that are bi-directional tri-state

**Pin Assignments and Pin Type**

| PC Card Memory Mode |                   |          |              | PC Card I/O Mode |                   |          |              | True IDE Mode <sup>4</sup> |                   |          |              |
|---------------------|-------------------|----------|--------------|------------------|-------------------|----------|--------------|----------------------------|-------------------|----------|--------------|
| Pin                 | Signal Name       | Pin Type | In, Out Type | Pin              | Signal Name       | Pin Type | In, Out Type | Pin                        | Signal Name       | Pin Type | In, Out Type |
| 1                   | GND               |          | Ground       | 1                | GND               |          | Ground       | 1                          | GND               |          | Ground       |
| 2                   | D03               | I/O      | I4Z,OZ1      | 2                | D03               | I/O      | I4Z,OZ1      | 2                          | D03               | I/O      | I4Z,OZ1      |
| 3                   | D04               | I/O      | I4Z,OZ1      | 3                | D04               | I/O      | I4Z,OZ1      | 3                          | D04               | I/O      | I4Z,OZ1      |
| 4                   | D05               | I/O      | I4Z,OZ1      | 4                | D05               | I/O      | I4Z,OZ1      | 4                          | D05               | I/O      | I4Z,OZ1      |
| 5                   | D06               | I/O      | I4Z,OZ1      | 5                | D06               | I/O      | I4Z,OZ1      | 5                          | D06               | I/O      | I4Z,OZ1      |
| 6                   | D07               | I/O      | I4Z,OZ1      | 6                | D07               | I/O      | I4Z,OZ1      | 6                          | D07               | I/O      | I4Z,OZ1      |
| 7                   | –CE1              | I        | I3U          | 7                | –CE1              | I        | I3U          | 7                          | –CS0              | I        | I3U          |
| 8                   | A10               | I        | I3Z          | 8                | A10               | I        | I3Z          | 8                          | A10 <sup>2</sup>  | I        | I3Z          |
| 9                   | –OE               | I        | I4U          | 9                | –OE               | I        | I4U          | 9                          | –ATA SEL          | I        | I4U          |
| 10                  | A09               | I        | I3Z          | 10               | A09               | I        | I3Z          | 10                         | A09 <sup>2</sup>  | I        | I3Z          |
| 11                  | A08               | I        | I3Z          | 11               | A08               | I        | I3Z          | 11                         | A08 <sup>2</sup>  | I        | I3Z          |
| 12                  | A07               | I        | I3Z          | 12               | A07               | I        | I3Z          | 12                         | A07 <sup>2</sup>  | I        | I3Z          |
| 13                  | VCC               |          | Power        | 13               | VCC               |          | Power        | 13                         | VCC               |          | Power        |
| 14                  | A06               | I        | I3Z          | 14               | A06               | I        | I3Z          | 14                         | A06 <sup>2</sup>  | I        | I3Z          |
| 15                  | A05               | I        | I3Z          | 15               | A05               | I        | I3Z          | 15                         | A05 <sup>2</sup>  | I        | I3Z          |
| 16                  | A04               | I        | I3Z          | 16               | A04               | I        | I3Z          | 16                         | A04 <sup>2</sup>  | I        | I3Z          |
| 17                  | A03               | I        | I3Z          | 17               | A03               | I        | I3Z          | 17                         | A03 <sup>2</sup>  | I        | I3Z          |
| 18                  | A02               | I        | I3Z          | 18               | A02               | I        | I3Z          | 18                         | A02               | I        | I3Z          |
| 19                  | A01               | I        | I3Z          | 19               | A01               | I        | I3Z          | 19                         | A01               | I        | I3Z          |
| 20                  | A00               | I        | I3Z          | 20               | A00               | I        | I3Z          | 20                         | A00               | I        | I3Z          |
| 21                  | D00               | I/O      | I4Z,OZ1      | 21               | D00               | I/O      | I4Z,OZ1      | 21                         | D00               | I/O      | I4Z,OZ1      |
| 22                  | D01               | I/O      | I4Z,OZ1      | 22               | D01               | I/O      | I4Z,OZ1      | 22                         | D01               | I/O      | I4Z,OZ1      |
| 23                  | D02               | I/O      | I4Z,OZ1      | 23               | D02               | I/O      | I4Z,OZ1      | 23                         | D02               | I/O      | I4Z,OZ1      |
| 24                  | WP                | O        | OT1          | 24               | –IOIS16           | O        | OT1          | 24                         | –IOCS16           | O        | ON1          |
| 25                  | –CD2              | O        | Ground       | 25               | –CD2              | O        | Ground       | 25                         | –CD2              | O        | Ground       |
| 26                  | –CD1              | O        | Ground       | 26               | –CD1              | O        | Ground       | 26                         | –CD1              | O        | Ground       |
| 27                  | D11 <sup>1</sup>  | I/O      | I4Z,OZ1      | 27               | D11 <sup>1</sup>  | I/O      | I4Z,OZ1      | 27                         | D11 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 28                  | D12 <sup>1</sup>  | I/O      | I4Z,OZ1      | 28               | D12 <sup>1</sup>  | I/O      | I4Z,OZ1      | 28                         | D12 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 29                  | D13 <sup>1</sup>  | I/O      | I4Z,OZ1      | 29               | D13 <sup>1</sup>  | I/O      | I4Z,OZ1      | 29                         | D13 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 30                  | D14 <sup>1</sup>  | I/O      | I4Z,OZ1      | 30               | D14 <sup>1</sup>  | I/O      | I4Z,OZ1      | 30                         | D14 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 31                  | D15 <sup>1</sup>  | I/O      | I4Z,OZ1      | 31               | D15 <sup>1</sup>  | I/O      | I4Z,OZ1      | 31                         | D15 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 32                  | –CE2 <sup>1</sup> | I        | I3U          | 32               | –CE2 <sup>1</sup> | I        | I3U          | 32                         | –CS1 <sup>1</sup> | I        | I3U          |
| 33                  | –VS1              | O        | Ground       | 33               | –VS1              | O        | Ground       | 33                         | –VS1              | O        | Ground       |
| 34                  | –IORD             | I        | I4U          | 34               | –IORD             | I        | I4U          | 34                         | –IORD             | I        | I4U          |
| 35                  | –IOWR             | I        | I4U          | 35               | –IOWR             | I        | I4U          | 35                         | –IOWR             | I        | I4U          |
| 36                  | –WE               | I        | I4U          | 36               | –WE               | I        | I4U          | 36                         | –WE <sup>3</sup>  | I        | I4U          |
| 37                  | RDY/BSY           | O        | OT1          | 37               | IREQ              | O        | OT1          | 37                         | INTRQ             | O        | OZ1          |
| 38                  | VCC               |          | Power        | 38               | VCC               |          | Power        | 38                         | VCC               |          | Power        |
| 39                  | –CSEL             | I        | I1U          | 39               | –CSEL             | I        | I1U          | 39                         | –CSEL             | I        | I1U          |
| 40                  | –VS2              | O        | OPEN         | 40               | –VS2              | O        | OPEN         | 40                         | –VS2              | O        | OPEN         |
| 41                  | RESET             | I        | I3U          | 41               | RESET             | I        | I3U          | 41                         | –RESET            | I        | I3U          |

| PC Card Memory Mode |                  |          |              | PC Card I/O Mode |                  |          |              | True IDE Mode <sup>4</sup> |                   |          |              |
|---------------------|------------------|----------|--------------|------------------|------------------|----------|--------------|----------------------------|-------------------|----------|--------------|
| Pin                 | Signal Name      | Pin Type | In, Out Type | Pin              | Signal Name      | Pin Type | In, Out Type | Pin                        | Signal Name       | Pin Type | In, Out Type |
| 42                  | –WAIT            | O        | OT1          | 42               | –WAIT            | O        | OT1          | 42                         | IORDY             | O        | ON1          |
| 43                  | –INPACK          | O        | OT1          | 43               | –INPACK          | O        | OT1          | 43                         | –INPACK           | O        | OZ1          |
| 44                  | –REG             | I        | I3U          | 44               | –REG             | I        | I3U          | 44                         | –REG <sup>3</sup> | I        | I3U          |
| 45                  | BVD2             | I/O      | I4U,OT1      | 45               | –SPKR            | I/O      | I4U,OT1      | 45                         | –DASP             | I/O      | I4U,ON1      |
| 46                  | BVD1             | I/O      | I4U,OT1      | 46               | –STSCHG          | I/O      | I4U,OT1      | 46                         | –PDIAG            | I/O      | I4U,ON1      |
| 47                  | D08 <sup>1</sup> | I/O      | I4Z,OZ1      | 47               | D08 <sup>1</sup> | I/O      | I4Z,OZ1      | 47                         | D08 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 48                  | D09 <sup>1</sup> | I/O      | I4Z,OZ1      | 48               | D09 <sup>1</sup> | I/O      | I4Z,OZ1      | 48                         | D09 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 49                  | D10 <sup>1</sup> | I/O      | I4Z,OZ1      | 49               | D10 <sup>1</sup> | I/O      | I4Z,OZ1      | 49                         | D10 <sup>1</sup>  | I/O      | I4Z,OZ1      |
| 50                  | GND              |          | Ground       | 50               | GND              |          | Ground       | 50                         | GND               |          | Ground       |

- Notes:
1. These signals are required only for 16 bit access and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
  2. Should be grounded by the host.
  3. Should be tied to VCC by the host.

## Signal Description

| Signal Name                         | Dir | Pin No.                                    | Description                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------|-----|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A10 to A0<br>(PC Card Memory Mode)  | I   | 8,10,11,12,14,15,16,17,18,19,20            | These address lines along with the-REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers.                                                                       |
| A10 to A0<br>(PC Card I/O Mode)     |     |                                            |                                                                                                                                                                                                                                                                                                                                                                                                          |
| A2 to A0<br>(True IDE Mode)         |     | 18,19,20                                   | In True IDE Mode only A [2 : 0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.                                                                                                                                                                                                                                              |
| BVD1<br>(PC Card Memory Mode)       | I/O | 46                                         | This signal is asserted high as BVD1 is not supported                                                                                                                                                                                                                                                                                                                                                    |
| –STSCHG<br>(PC Card I/O Mode)       |     |                                            | This signal is asserted low to alert the host to changes in the RDY/–BSY and Write Protect states; while the I/O interface is configured .Its use is controlled by the Card Config and Status Register.                                                                                                                                                                                                  |
| –PDIAG<br>(True IDE Mode)           |     |                                            | In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol                                                                                                                                                                                                                                                                                             |
| BVD2<br>(PC Card Memory Mode)       | I/O | 45                                         | This signal is asserted high, as BVD2 is not supported.                                                                                                                                                                                                                                                                                                                                                  |
| –SPKR<br>(PC Card I/O Mode)         |     |                                            | This line is the Binary Audio output from the card .If the Card does not support the Binary Audio function, this line should be held negated.                                                                                                                                                                                                                                                            |
| –DASP<br>(True IDE Mode)            |     |                                            | In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.                                                                                                                                                                                                                                                                                  |
| –CD1, –CD2<br>(PC Card Memory Mode) | O   | 26,25                                      | These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket.                                                                                                                                                                                                            |
| –CD1, –CD2<br>(PC Card I/O Mode)    |     |                                            |                                                                                                                                                                                                                                                                                                                                                                                                          |
| –CD1, –CD2<br>(True IDE Mode)       |     |                                            |                                                                                                                                                                                                                                                                                                                                                                                                          |
| –CE1, –CE2<br>(PC Card Memory Mode) | I   | 7,32                                       | These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2.A multiplexing scheme based on A0, –CE1, –CE2 allows 8 bit hosts to access all data on D0~D7.<br>See Access specification below. |
| –CE1, –CE2<br>(PC Card I/O Mode)    |     |                                            |                                                                                                                                                                                                                                                                                                                                                                                                          |
| –CS0, –CS1<br>(True IDE Mode)       |     |                                            | In the True IDE Mode CS0 is the chip select for the task file registers while CS1 is used to select the Alternate Status Register and the Device Control Register.                                                                                                                                                                                                                                       |
| –CSEL<br>(PC Card Memory Mode)      | I   | 39                                         | This signal is not used for this mode.                                                                                                                                                                                                                                                                                                                                                                   |
| –CSEL<br>(PC Card I/O Mode)         |     |                                            |                                                                                                                                                                                                                                                                                                                                                                                                          |
| –CSEL<br>(True IDE Mode)            |     |                                            | This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.                                                                                                                                             |
| D15 to D00<br>(PC Card Memory Mode) | I/O | 31,30,29,28,27,49,48,47,6,5,4,3,2,23,22,21 | These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word.                                                                                                                                                                                                                 |
| D15 to D00<br>(PC Card I/O Mode)    |     |                                            |                                                                                                                                                                                                                                                                                                                                                                                                          |
| D15 to D00<br>(True IDE Mode)       |     |                                            | True IDE Mode, all Task File operations occur in byte mode on the low order bus D00 to D07 while all data transfers are 16 bit using D00 to D15.                                                                                                                                                                                                                                                         |

| Signal Name                      | Dir | Pin No. | Description                                                                                                                                                                                                                                                                                                           |
|----------------------------------|-----|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND<br>(PC Card Memory Mode)     | —   | 1,50    | Ground                                                                                                                                                                                                                                                                                                                |
| GND<br>(PC Card I/O Mode)        |     |         |                                                                                                                                                                                                                                                                                                                       |
| GND<br>(True IDE Mode)           |     |         |                                                                                                                                                                                                                                                                                                                       |
| —INPACK<br>(PC Card Memory Mode) | O   | 43      | This signal is not used in this mode.                                                                                                                                                                                                                                                                                 |
| —INPACK<br>(PC Card I/O Mode)    |     |         | The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU. |
| —INPACK<br>(True IDE Mode)       |     |         | In True IDE Mode this output signal is not used and should not be connected at the host.                                                                                                                                                                                                                              |
| —IORD<br>(PC Card Memory Mode)   | I   | 34      | This signal is not used in this mode.                                                                                                                                                                                                                                                                                 |
| —IORD<br>(PC Card I/O Mode)      |     |         | This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface.                                                                                                                                    |
| —IORD<br>(True IDE Mode)         |     |         | In True IDE Mode, this signal has same function as in PC Card I/O Mode.                                                                                                                                                                                                                                               |
| —IOWR<br>(PC Card Memory Mode)   | I   | 35      | This signal is not used in this mode.                                                                                                                                                                                                                                                                                 |
| —IOWR<br>(PC Card I/O Mode)      |     |         | The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface.<br><br>The clocking will occur on the negative to positive edge of the signal (trailing edge)            |
| —IOWR<br>(True IDE Mode)         |     |         | In True IDE Mode, this signal has the same function as in PC Card I/O Mode.                                                                                                                                                                                                                                           |
| —OE<br>(PC Card Memory Mode)     | I   | 9       | This is an Output Enable strobe generated by the host interface .It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers.                                                                                                                           |
| —OE<br>(PC Card I/O Mode)        |     |         | In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.                                                                                                                                                                                                                                 |
| —ATA SEL<br>(True IDE Mode)      |     |         | To enable True IDE Mode this input should be grounded by the host.                                                                                                                                                                                                                                                    |

| Signal Name                                                                   | Dir | Pin No. | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------------------------|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RDY/-BSY<br>(PC Card Memory Mode)                                             | O   | 37      | In Memory Mode this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and held low when the card is busy .The Host memory card socket must provide a pull-up resistor.<br><br>At power up and at Reset the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time .The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true. The CompactFlash Storage Card has been powered up with + RESET continuously disconnected or asserted. |
| —IREQ<br>(PC Card I/O Mode)                                                   |     |         | Operation-After the CompactFlash Storage Card has been configured for I/O operation; this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| INTRQ<br>(True IDE Mode)                                                      |     |         | In True IDE Mode signal is the active high interrupt Request to the host.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| —REG<br>(PC Card Memory Mode)                                                 | I   | 44      | This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| —REG<br>(PC Card I/O Mode)                                                    |     |         | The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| —REG<br>(True IDE Mode)                                                       |     |         | In True IDE Mode this input signal is not used and should be connected to VCC by the host.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| RESET<br>(PC Card Memory Mode)                                                | I   | 41      | When the pin is high, this signal Resets the CompactFlash Storage Card. The CompactFlash Storage Card is Reset only at power up if this pin is left high or open from power-up .The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.                                                                                                                                                                                                                                                                                                                                                                                    |
| RESET<br>(PC Card I/O Mode)                                                   |     |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| —RESET<br>(True IDE Mode)                                                     |     |         | In the True IDE Mode this input pin is the active low hardware reset from the host.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| VCC<br>(PC Card Memory Mode)<br>(PC Card I/O Mode)<br>(True IDE Mode)         | —   | 13,38   | +5V +3.3V power                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| —VS1 / —VS2<br>(PC Card Memory Mode)<br>(PC Card I/O Mode)<br>(True IDE Mode) | O   | 33,40   | Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Storage Card CIS can be read at 3.3 volts and —VS2 is reserved by PCMCIA for a secondary voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| —WAIT<br>(PC Card Memory Mode)                                                | O   | 42      | The —WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| —WAIT<br>(PC Card I/O Mode)                                                   |     |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| IORDY<br>(True IDE Mode)                                                      |     |         | In True IDE Mode this output signal may be used as IORDY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| —WE<br>(PC Card Memory Mode)                                                  | I   | 36      | This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| —WE<br>(PC Card I/O Mode)                                                     |     |         | In PC Card I/O Mode, this signal is used for writing the configuration registers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

| Signal Name                   | Dir | Pin No. | Description                                                                                                                                                                                                                                                      |
|-------------------------------|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| –WE<br>(True IDE Mode)        |     |         | In True IDE Mode this input signal is not used and should be connected to VCC by the host.                                                                                                                                                                       |
| WP<br>(PC Card Memory Mode )  | O   | 24      | Memory Mode-The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.                                                                                               |
| –IOIS16<br>(PC Card I/O Mode) |     |         | I/O Operation-When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (–IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. |
| –IOIS16<br>(True IDE Mode)    |     |         | In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.                                                                                                                                                    |

## Access Specifications

### 1. Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of  $\text{--REG}=\text{"L"}$  as follows. That region can be accessed by Byte/World/Old-byte modes, which are defined by PC card standard specifications.

#### • Attribute Read Access Mode

| Mode                   | $\text{--REG}$ | $\text{--CE2}$ | $\text{--CE1}$ | A0 | $\text{--OE}$ | $\text{--WE}$ | D8 to D15 | D0 to D7  |
|------------------------|----------------|----------------|----------------|----|---------------|---------------|-----------|-----------|
| Standby mode           | X              | H              | H              | X  | X             | X             | High-Z    | High-Z    |
| Byte access (8bit)     | L              | H              | L              | L  | L             | H             | High-Z    | even byte |
|                        | L              | H              | L              | H  | L             | H             | High-Z    | invalid   |
| Word access (16bit)    | L              | L              | L              | X  | L             | H             | invalid   | even byte |
| Odd byte access (8bit) | L              | L              | H              | X  | L             | H             | invalid   | High-Z    |

Note: X  $\rightarrow$  L or H

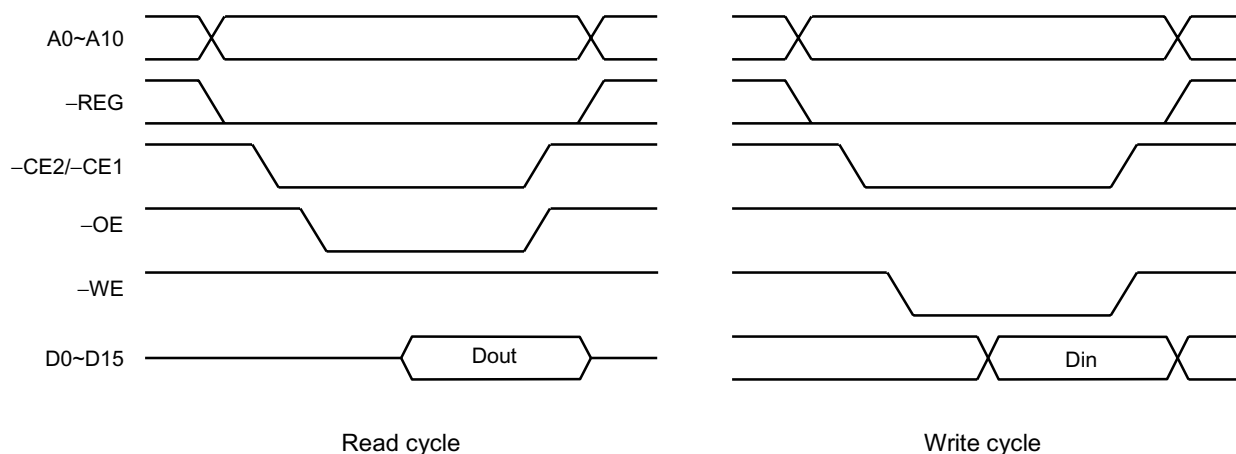
#### • Attribute Write Access Mode

| Mode                   | $\text{--REG}$ | $\text{--CE2}$ | $\text{--CE1}$ | A0 | $\text{--OE}$ | $\text{--WE}$ | D8 to D15  | D0 to D7   |
|------------------------|----------------|----------------|----------------|----|---------------|---------------|------------|------------|
| Standby mode           | X              | H              | H              | X  | X             | X             | Don't care | Don't care |
| Byte access (8bit)     | L              | H              | L              | L  | H             | L             | Don't care | even byte  |
|                        | L              | H              | L              | H  | H             | L             | Don't care | Don't care |
| Word access (16bit)    | L              | L              | L              | X  | H             | L             | Don't care | even byte  |
| Odd byte access (8bit) | L              | L              | H              | X  | H             | L             | Don't care | Don't care |

Note: X  $\rightarrow$  L or H

Write CIS-ROM region is invalid.

#### • Attribute Write Timing Example



## 2. Task File register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File registers read and write operations is executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte modes, which are defined by PC card standard specifications.

### (1) I/O address map

#### • Task File Register Read Access Mode (1)

| Mode                   | –REG | –CE2 | –CE1 | A0 | –IORD | –IOWR | –OE | –WE | D8 to D15 | D0 to D7  |
|------------------------|------|------|------|----|-------|-------|-----|-----|-----------|-----------|
| Standby mode           | X    | H    | H    | X  | X     | X     | X   | X   | High-Z    | High-Z    |
| Byte access (8bit)     | L    | H    | L    | L  | L     | H     | H   | H   | High-Z    | even byte |
|                        | L    | H    | L    | H  | L     | H     | H   | H   | High-Z    | odd byte  |
| Word access (16bit)    | L    | L    | L    | X  | L     | H     | H   | H   | odd byte  | even byte |
| Odd byte access (8bit) | L    | L    | H    | X  | L     | H     | H   | H   | odd byte  | High-Z    |

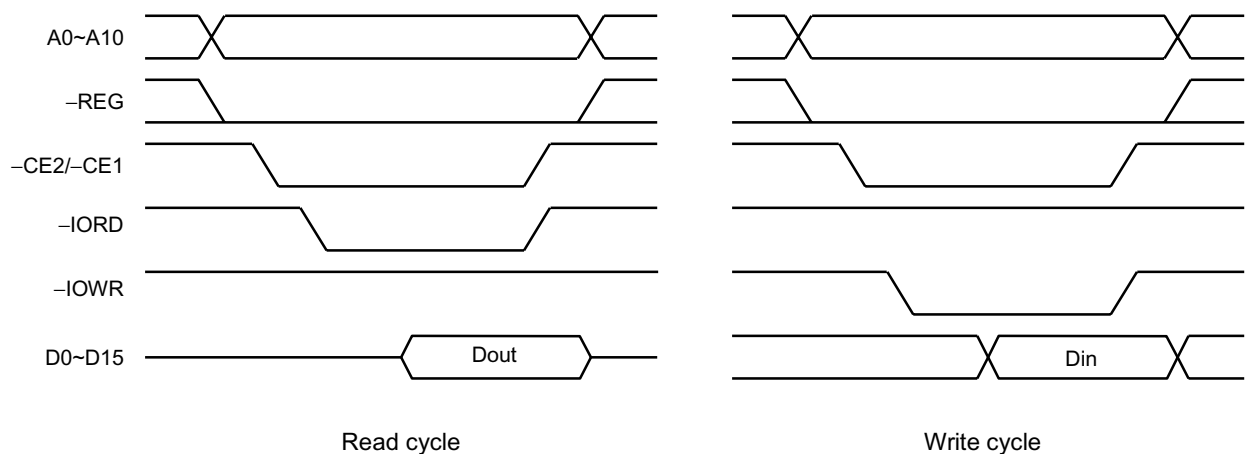
Note: X → L or H

#### • Task File Register Write Access Mode (1)

| Mode                   | –REG | –CE2 | –CE1 | A0 | –IORD | –IOWR | –OE | –WE | D8 to D15  | D0 to D7   |
|------------------------|------|------|------|----|-------|-------|-----|-----|------------|------------|
| Standby mode           | X    | H    | H    | X  | X     | X     | X   | X   | Don't care | Don't care |
| Byte access (8bit)     | L    | H    | L    | L  | H     | L     | H   | H   | Don't care | even byte  |
|                        | L    | H    | L    | H  | H     | L     | H   | H   | Don't care | odd byte   |
| Word access (16bit)    | L    | L    | L    | X  | H     | L     | H   | H   | odd byte   | even byte  |
| Odd byte access (8bit) | L    | L    | H    | X  | H     | L     | H   | H   | odd byte   | Don't care |

Note: X → L or H

#### • Task File Register Access Timing Example (1)



## (2) Memory address map

### • Task File Register Read Access Mode (2)

| Mode                   | -REG | -CE2 | -CE1 | A0 | -OE | -WE | -IORD | -IOWR | D8 to D15 | D0 to D7  |
|------------------------|------|------|------|----|-----|-----|-------|-------|-----------|-----------|
| Standby mode           | X    | H    | H    | X  | X   | X   | X     | X     | High-Z    | High-Z    |
| Byte access (8bit)     | H    | H    | L    | L  | L   | H   | H     | H     | High-Z    | even byte |
|                        | H    | H    | L    | H  | L   | H   | H     | H     | High-Z    | odd byte  |
| Word access (16bit)    | H    | L    | L    | X  | L   | H   | H     | H     | odd byte  | even byte |
| Odd byte access (8bit) | H    | L    | H    | X  | L   | H   | H     | H     | odd byte  | High-Z    |

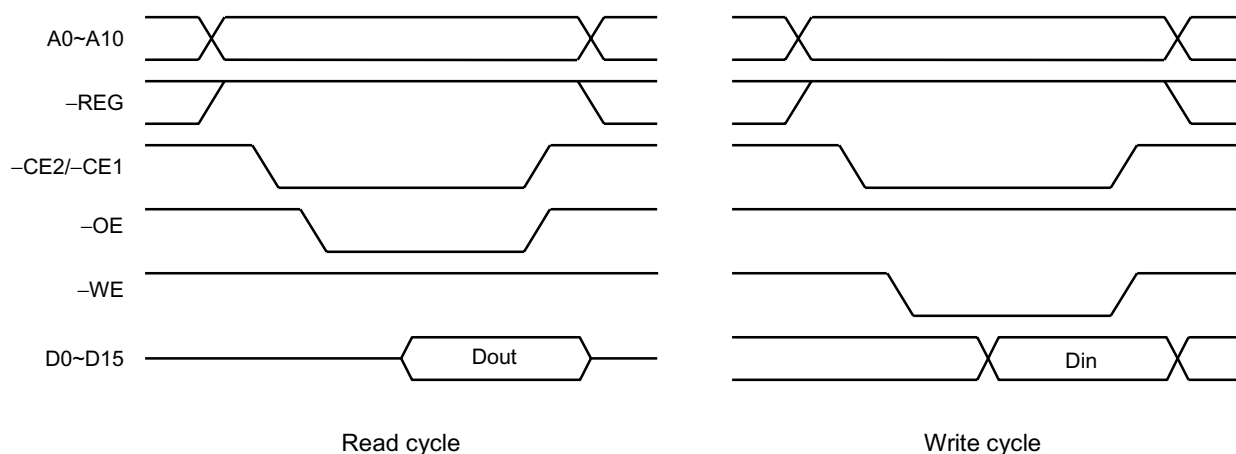
Note: X → L or H

### • Task File Register Write Access Mode (2)

| Mode                   | -REG | -CE2 | -CE1 | A0 | -OE | -WE | -IORD | -IOWR | D8 to D15  | D0 to D7   |
|------------------------|------|------|------|----|-----|-----|-------|-------|------------|------------|
| Standby mode           | X    | H    | H    | X  | X   | X   | X     | X     | Don't care | Don't care |
| Byte access (8bit)     | H    | H    | L    | L  | H   | L   | H     | H     | Don't care | even byte  |
|                        | H    | H    | L    | H  | H   | L   | H     | H     | Don't care | odd byte   |
| Word access (16bit)    | H    | L    | L    | X  | H   | L   | H     | H     | odd byte   | even byte  |
| Odd byte access (8bit) | H    | L    | H    | X  | H   | L   | H     | H     | odd byte   | Don't care |

Note: X → L or H

### • Task File Register Access Timing Example (2)



### 3. True IDE Mode

The card can be configured in a True IDE. This card is configured in this mode only when the OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register is allowed. If this card is configured during power on sequence, data register is accessed in word (16-bit). The card permits 8-bit access if the user issues a Set Feature Command to put the device in 8-bit mode.

#### • True IDE Mode Read I/O Function

| Mode                    | –CE2 | –CE1 | A0~A2 | –IORD | –IOWR | D8 to D15 | D0 to D7   |
|-------------------------|------|------|-------|-------|-------|-----------|------------|
| Invalid mode            | L    | L    | X     | X     | X     | High-Z    | High-Z     |
| Standby mode            | H    | H    | X     | X     | X     | High-Z    | High-Z     |
| Data register access    | H    | L    | 0     | L     | H     | odd byte  | even byte  |
| Alternate status access | L    | H    | 6H    | L     | H     | High-Z    | Status out |
| Other task file access  | H    | L    | 1~7H  | L     | H     | High-Z    | Data       |

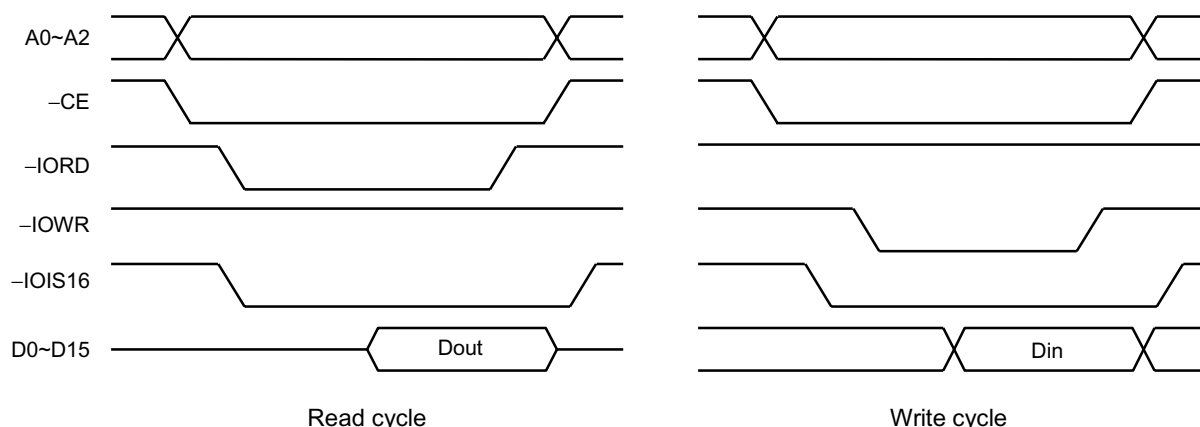
Note: X → L or H

#### • True IDE Mode Write I/O Function

| Mode                    | –CE2 | –CE1 | A0~A2 | –IORD | –IOWR | D8 to D15  | D0 to D7   |
|-------------------------|------|------|-------|-------|-------|------------|------------|
| Invalid mode            | L    | L    | X     | X     | X     | Don't care | Don't care |
| Standby mode            | H    | H    | X     | X     | X     | Don't care | even byte  |
| Data register access    | H    | L    | 0     | H     | L     | odd byte   | Don't care |
| Control register access | L    | H    | 6H    | H     | L     | Don't care | Control in |
| Other task file access  | H    | L    | 1~7H  | H     | L     | odd byte   | Data       |

Note: X → L or H

#### • True IDE Mode I/O Access Timing Example



**Configuration register specifications**

This card supports four Configuration registers for the purpose of the configuration and observation of this card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers cannot be used.

**1. Configuration Option register (Address 200h)**

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

| bit7   | bit6    | bit5  | bit4 | bit3 | bit2 | bit1 | bit0 |
|--------|---------|-------|------|------|------|------|------|
| SRESET | LevIREQ | INDEX |      |      |      |      |      |

Note: initial value → 00H

| Name                | R/W | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRESET              | R/W | Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence. |
| LevIREQ<br>(HOST->) | R/W | This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected.                                                                                                                                                                                                                                                                                                                                                                        |
| INDEX<br>(HOST->)   | R/W | This bits is used for select operation mode of the card as follows.<br>When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition.                                                                                                                                                                                                                                                                                 |

Note: initial value → 00H

- INDEX bit assignment

INDEX bit

| 5 | 4 | 3 | 2 | 1 | 0 | Card mode   | Task file register address | Mapping mode          |
|---|---|---|---|---|---|-------------|----------------------------|-----------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | Memory card | 0H to FH, 400H to 7FFH     | Memory mapped         |
| 0 | 0 | 0 | 0 | 0 | 1 | I/O card    | xx0H to xxFH               | Contiguous I/O mapped |
| 0 | 0 | 0 | 0 | 1 | 0 | I/O card    | 1F0H to 1F7H, 3F6H to 3F7H | Primary I/O mapped    |
| 0 | 0 | 0 | 0 | 1 | 1 | I/O card    | 170H to 177H, 376H to 377H | Secondary I/O mapped  |

## 2. Configuration and Status register (Address 202h)

This register is used for observing the state of the card.

| bit7  | bit6   | bit5  | bit4 | bit3 | bit2 | bit1 | bit0 |
|-------|--------|-------|------|------|------|------|------|
| CHGED | SIGCHG | IOIS8 | 0    | 0    | PWD  | INTR | 0    |

Note: initial value → 00H

| Name               | R/W | Function                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHGED<br>(CARD->)  | R   | This bit indicates that CRDY/–BSY bit on Pin Replacement register is set to “1”. When CHGED bit is set to “1”, –STSCHG pin is held “L” at the condition of SIGCHG bit set to “1” and the card configured for the I/O interface.                                                                                                                                                                                                |
| SIGCHG<br>(HOST->) | R/W | This bit is set or reset by the host for enabling and disabling the status-change signal (–STSCHG pin). When the card is configured I/O card interface and this bit is set “1”, –STSCHG pin is controlled by CHGED bit. If this bit is set to “0”, –STSCHG pin is kept “H”.                                                                                                                                                    |
| IOIS8<br>(HOST->)  | R/W | The host sets this field to “1” when it can provide I/O cycles only with on 8 bit data bus (D7 to D0).                                                                                                                                                                                                                                                                                                                         |
| PWD<br>(HOST->)    | R/W | When this bit is set to “1”, the card enters sleep state (Power Down mode). When this bit is reset to “0”, the card transfers to idle state (active mode). RRDY/BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle and powers back up when it receives a command. |
| INTR<br>(CARD->)   | R   | This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition, which caused the interrupt request, has been serviced. If the –IEN bit in the Device Control Register disables interrupts, this bit is a zero.                                                                                |

## 3. Pin Replacement register (Address 204h)

This register is used for providing the state of  $\text{-IREQ}$  signal when the card configured I/O card interface.

| bit7 | bit6 | bit5                | bit4 | bit3 | bit2 | bit1                | bit0 |
|------|------|---------------------|------|------|------|---------------------|------|
| 0    | 0    | CRDY/ $\text{-BSY}$ | 0    | 1    | 1    | RRDY/ $\text{-BSY}$ | 0    |

Note: initial value  $\rightarrow$  0CH

| Name                                         | R/W | Function                                                                                                             |
|----------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------|
| CRDY/ $\text{-BSY}$<br>(HOST $\rightarrow$ ) | R/W | This bit is set to "1" when the RRDY/ $\text{-BSY}$ bit changes state. The host may also write this bit.             |
| RRDY/ $\text{-BSY}$<br>(HOST $\rightarrow$ ) | R   | When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/ $\text{-BSY}$ bit masking. |

## 4. Socket and Copy register (Address 206h)

This register is used for identification of the card from the other cards. Host can read and write this register. Host should set this register before this card's Configuration Option register set.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| 0    | 0    | 0    | DRV# | 0    | 0    | 0    | 0    |

Note: initial value  $\rightarrow$  00H

| Name                          | R/W | Function                                                                                                                                                                                                                  |
|-------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DRV#<br>(HOST $\rightarrow$ ) | R/W | These fields are used for the configuration of the plural cards. When host configures the plural cards, written the card's copy number in this field. In this way, host can perform the card's master/slave organization. |

**CIS information**

CIS information of Compact Flash card is defined as follows.

| Address | Data | Description of contents                 | CIS function |
|---------|------|-----------------------------------------|--------------|
| 000H    | 01H  | CISTPL_DEVICE                           | Tuple code   |
| 002H    | 03H  | TPL_LINK                                | Tuple link   |
| 004H    | D9H  | Device information                      | Tuple data   |
| 006H    | 01H  | Device information                      | Tuple data   |
| 008H    | FFH  | END MARKER                              | End of Tuple |
| 00AH    | 1CH  | CISTPL_DEVICE_OC                        | Tuple code   |
| 00CH    | 04H  | TPL_LINK                                | Tuple link   |
| 00EH    | 03H  | Conditions information                  | Tuple data   |
| 010H    | D9H  | Device information                      | Tuple data   |
| 012H    | 01H  | Device information                      | Tuple data   |
| 014H    | FFH  | END MARKER                              | End of Tuple |
| 016H    | 18H  | CISTPL_JEDEC_C                          | Tuple code   |
| 018H    | 02H  | TPL_LINK                                | Tuple link   |
| 01AH    | DFH  | PCMCIA's manufacture's JEDEC ID code    | Tuple data   |
| 01CH    | 01H  | PCMCIA's JEDEC device code              | Tuple data   |
| 01EH    | 20H  | CISTPL_MANFID                           | Tuple code   |
| 020H    | 04H  | TPL_LINK                                | Tuple link   |
| 022H    | 98H  | Low byte of manufacturer's ID code      | Tuple data   |
| 024H    | 00H  | High byte of manufacturer's ID code     | Tuple data   |
| 026H    | 00H  | Low byte of product code                | Tuple data   |
| 028H    | 00H  | High byte of product code               | Tuple data   |
| 02AH    | 15H  | CISTPL_VERS_1                           | Tuple code   |
| 02CH    | 20H  | TPL_LINK                                | Tuple link   |
| 02EH    | 04H  | TPLL1_MAJOR                             | Tuple data   |
| 030H    | 01H  | TPLL1_MINOR                             | Tuple data   |
| 032H    | 54H  | ' T ' (Vender Specific Strings)         | Tuple data   |
| 034H    | 4FH  | ' O ' (Vender Specific Strings)         | Tuple data   |
| 036H    | 53H  | ' S ' (Vender Specific Strings)         | Tuple data   |
| 038H    | 48H  | ' H ' (Vender Specific Strings)         | Tuple data   |
| 03AH    | 49H  | ' I ' (Vender Specific Strings)         | Tuple data   |
| 03CH    | 42H  | ' B ' (Vender Specific Strings)         | Tuple data   |
| 03EH    | 41H  | ' A ' (Vender Specific Strings)         | Tuple data   |
| 040H    | 20H  | ' ' (Vender Specific Strings)           | Tuple data   |
| 042H    | 54H  | ' T ' (Vender Specific Strings)         | Tuple data   |
| 044H    | 48H  | ' H ' (Vender Specific Strings)         | Tuple data   |
| 046H    | 4EH  | ' N ' (Vender Specific Strings)         | Tuple data   |
| 048H    | 43H  | ' C ' (Vender Specific Strings)         | Tuple data   |
| 04AH    | 46H  | ' F ' (Vender Specific Strings)         | Tuple data   |
| 04CH    | 30H  | ' 0 ' (Card capacity dependent strings) | Tuple data   |
| 04EH    | 30H  | ' 0 ' (Card capacity dependent strings) | Tuple data   |
| 050H    | 30H  | ' 0 ' (Card capacity dependent strings) | Tuple data   |
| 052H    | 4DH  | ' M ' (Card capacity dependent strings) | Tuple data   |
| 054H    | 42H  | ' B ' (Vender Specific Strings)         | Tuple data   |
| 056H    | 41H  | ' A ' (Vender Specific Strings)         | Tuple data   |

| Address | Data | Description of contents                    | CIS function |
|---------|------|--------------------------------------------|--------------|
| 058H    | 20H  | ' '                                        | Tuple data   |
| 05AH    | 00H  | Null Terminator                            | Tuple data   |
| 05CH    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 05EH    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 060H    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 062H    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 064H    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 066H    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 068H    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 06AH    | 00H  | Reserved (Vender Specific Strings)         | Tuple data   |
| 06CH    | FFH  | END MARKER                                 | End of Tuple |
| 06EH    | 21H  | CISTPL_FUNCID                              | Tuple code   |
| 070H    | 02H  | TPL_LINK                                   | Tuple link   |
| 072H    | 04H  | IC Card function code                      | Tuple data   |
| 074H    | 01H  | System initialization bit mask             | Tuple data   |
| 076H    | 22H  | CISTPL_FUNCE                               | Tuple code   |
| 078H    | 02H  | TPL_LINK                                   | Tuple link   |
| 07AH    | 01H  | Type of extended data                      | Tuple data   |
| 07CH    | 01H  | Function information                       | Tuple data   |
| 07EH    | 22H  | CISTPL_FUNCE                               | Tuple code   |
| 080H    | 03H  | TPL_LINK                                   | Tuple link   |
| 082H    | 02H  | Type of extended data                      | Tuple data   |
| 084H    | 0CH  | Function information                       | Tuple data   |
| 086H    | 0FH  | Function information                       | Tuple data   |
| 088H    | 1AH  | CISTPL_CONFIG                              | Tuple code   |
| 08AH    | 05H  | TPL_LINK                                   | Tuple link   |
| 08CH    | 01H  | Size field                                 | Tuple data   |
| 08EH    | 03H  | Index number of last entry                 | Tuple data   |
| 090H    | 00H  | Configuration register base address (Low)  | Tuple data   |
| 092H    | 02H  | Configuration register base address (High) | Tuple data   |
| 094H    | 0FH  | Configuration register present mask        | Tuple data   |
| 096H    | 1BH  | CISTPL_CFTABLE_ENTRY                       | Tuple code   |
| 098H    | 08H  | TPL_LINK                                   | Tuple link   |
| 09AH    | C0H  | Configuration Index Byte                   | Tuple data   |
| 09CH    | C0H  | Interface Descriptor                       | Tuple data   |
| 09EH    | A1H  | Feature Select                             | Tuple data   |
| 0A0H    | 01H  | Vcc Selection Byte                         | Tuple data   |
| 0A2H    | 55H  | Nom V Parameter                            | Tuple data   |
| 0A4H    | 08H  | Memory length (256 byte pages)             | Tuple data   |
| 0A6H    | 00H  | Memory length (256 byte pages)             | Tuple data   |
| 0A8H    | 20H  | Misc features                              | Tuple data   |
| 0AAH    | 1BH  | CISTPL_CFTABLE_ENTRY                       | Tuple code   |
| 0ACH    | 06H  | TPL_LINK                                   | Tuple link   |
| 0AEH    | 00H  | Configuration Index Byte                   | Tuple data   |
| 0B0H    | 01H  | Feature Select                             | Tuple data   |
| 0B2H    | 21H  | Vcc Selection Byte                         | Tuple data   |
| 0B4H    | B5H  | Nom V Parameter                            | Tuple data   |

| Address | Data | Description of contents   | CIS function |
|---------|------|---------------------------|--------------|
| 0B6H    | 1EH  | Nom V Parameter           | Tuple data   |
| 0B8H    | 4DH  | Peak I Parameter          | Tuple data   |
| 0BAH    | 1BH  | CISTPL_CFTABLE_ENTRY      | Tuple code   |
| 0BCH    | 0AH  | TPL_LINK                  | Tuple link   |
| 0BEH    | C1H  | Configuration Index Byte  | Tuple data   |
| 0C0H    | 41H  | Interface Descriptor      | Tuple data   |
| 0C2H    | 99H  | Feature Select            | Tuple data   |
| 0C4H    | 01H  | Vcc Selection Byte        | Tuple data   |
| 0C6H    | 55H  | Nom V Parameter           | Tuple data   |
| 0C8H    | 64H  | I/O Parameter             | Tuple data   |
| 0CAH    | F0H  | IRQ parameter             | Tuple data   |
| 0CCH    | FFH  | IRQ request mask          | Tuple data   |
| 0CEH    | FFH  | IRQ request mask          | Tuple data   |
| 0D0H    | 20H  | Misc features             | Tuple data   |
| 0D2H    | 1BH  | CISTPL_CFTABLE_ENTRY      | Tuple code   |
| 0D4H    | 06H  | TPL_LINK                  | Tuple link   |
| 0D6H    | 01H  | Configuration Index Byte  | Tuple data   |
| 0D8H    | 01H  | Feature Select            | Tuple data   |
| 0DAH    | 21H  | Vcc Selection Byte        | Tuple data   |
| 0DCH    | B5H  | Nom V Parameter           | Tuple data   |
| 0DEH    | 1EH  | Nom V Parameter           | Tuple data   |
| 0E0H    | 4DH  | Peak I Parameter          | Tuple data   |
| 0E2H    | 1BH  | CISTPL_CFTABLE_ENTRY      | Tuple code   |
| 0E4H    | 0FH  | TPL_LINK                  | Tuple link   |
| 0E6H    | C2H  | Configuration Index Byte  | Tuple data   |
| 0E8H    | 41H  | Interface Descriptor      | Tuple data   |
| 0EAH    | 99H  | Feature Select            | Tuple data   |
| 0ECH    | 01H  | Vcc Selection Byte        | Tuple data   |
| 0EEH    | 55H  | Nom V Parameter           | Tuple data   |
| 0F0H    | EAH  | I/O parameter             | Tuple data   |
| 0F2H    | 61H  | I/O range length and size | Tuple data   |
| 0F4H    | F0H  | Base address              | Tuple data   |
| 0F6H    | 01H  | Base address              | Tuple data   |
| 0F8H    | 07H  | Address length            | Tuple data   |
| 0FAH    | F6H  | Base address              | Tuple data   |
| 0FCH    | 03H  | Base address              | Tuple data   |
| 0FEH    | 01H  | Address length            | Tuple data   |
| 100H    | EEH  | IRQ parameter             | Tuple data   |
| 102H    | 20H  | Misc features             | Tuple data   |
| 104H    | 1BH  | CISTPL_CFTABLE_ENTRY      | Tuple code   |
| 106H    | 06H  | TPL_LINK                  | Tuple link   |
| 108H    | 02H  | Configuration Index Byte  | Tuple data   |
| 10AH    | 01H  | Feature Select            | Tuple data   |
| 10CH    | 21H  | Vcc Selection Byte        | Tuple data   |
| 10EH    | B5H  | Nom V Parameter           | Tuple data   |
| 110H    | 1EH  | Nom V Parameter           | Tuple data   |
| 112H    | 4DH  | Peak I Parameter          | Tuple data   |

| Address | Data | Description of contents   | CIS function |
|---------|------|---------------------------|--------------|
| 114H    | 1BH  | CISTPL_CFTABLE_ENTRY      | Tuple code   |
| 116H    | 0FH  | TPL_LINK                  | Tuple link   |
| 118H    | C3H  | Configuration Index Byte  | Tuple data   |
| 11AH    | 41H  | Interface Descriptor      | Tuple data   |
| 11CH    | 99H  | Feature Select            | Tuple data   |
| 11EH    | 01H  | Vcc Selection Byte        | Tuple data   |
| 120H    | 55H  | Nom V Parameter           | Tuple data   |
| 122H    | EAH  | I/O parameter             | Tuple data   |
| 124H    | 61H  | I/O range length and size | Tuple data   |
| 126H    | 70H  | Base address              | Tuple data   |
| 128H    | 01H  | Base address              | Tuple data   |
| 12AH    | 07H  | Address length            | Tuple data   |
| 12CH    | 76H  | Base address              | Tuple data   |
| 12EH    | 03H  | Base address              | Tuple data   |
| 130H    | 01H  | Address length            | Tuple data   |
| 132H    | EEH  | IRQ parameter             | Tuple data   |
| 134H    | 20H  | Misc features             | Tuple data   |
| 136H    | 1BH  | CISTPL_CFTABLE_ENTRY      | Tuple code   |
| 138H    | 06H  | TPL_LINK                  | Tuple link   |
| 13AH    | 03H  | Configuration Index Byte  | Tuple data   |
| 13CH    | 01H  | Feature Select            | Tuple data   |
| 13EH    | 21H  | Vcc Selection Byte        | Tuple data   |
| 140H    | B5H  | Nom V Parameter           | Tuple data   |
| 142H    | 1EH  | Nom V Parameter           | Tuple data   |
| 144H    | 4DH  | Peak I Parameter          | Tuple data   |
| 146H    | 14H  | CISTPL_NO_LINK            | Tuple code   |
| 148H    | 00H  | TPL_LINK                  | Tuple link   |
| 14AH    | FFH  | CISTPL_END                | End of Tuple |

**Task File Register specification**

These registers are used for reading and writing the storage data in this card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addresses are shown as follows.

**Memory map (INDEX=0)**

| –REG | A10 | A9~A4 | A3 | A2 | A1 | A0 | Offset | –OE=L                   | –WE=L                   |
|------|-----|-------|----|----|----|----|--------|-------------------------|-------------------------|
| 1    | 0   | X     | 0  | 0  | 0  | 0  | 0H     | Data register           | Data register           |
| 1    | 0   | X     | 0  | 0  | 0  | 1  | 1H     | Error register          | Feature register        |
| 1    | 0   | X     | 0  | 0  | 1  | 0  | 2H     | Sector count register   | Sector count register   |
| 1    | 0   | X     | 0  | 0  | 1  | 1  | 3H     | Sector number register  | Sector number register  |
| 1    | 0   | X     | 0  | 1  | 0  | 0  | 4H     | Cylinder low register   | Cylinder low register   |
| 1    | 0   | X     | 0  | 1  | 0  | 1  | 5H     | Cylinder high register  | Cylinder high register  |
| 1    | 0   | X     | 0  | 1  | 1  | 0  | 6H     | Drive head register     | Drive head register     |
| 1    | 0   | X     | 0  | 1  | 1  | 1  | 7H     | Status register         | Command register        |
| 1    | 0   | X     | 1  | 0  | 0  | 0  | 8H     | Dup. Even data register | Dup. even data register |
| 1    | 0   | X     | 1  | 0  | 0  | 1  | 9H     | Dup.odd data register   | Dup.odd data register   |
| 1    | 0   | X     | 1  | 1  | 0  | 1  | DH     | Dup.error register      | Dup.feature register    |
| 1    | 0   | X     | 1  | 1  | 1  | 0  | EH     | Alt. status register    | Device control register |
| 1    | 0   | X     | 1  | 1  | 1  | 1  | FH     | Drive address register  | Reserved                |
| 1    | 1   | X     | X  | X  | X  | 0  | 8H     | Even data register      | Even data register      |
| 1    | 1   | X     | X  | X  | X  | 1  | 9H     | Odd data register       | Odd data register       |

**Contiguous I/O map (INDEX=1)**

| –REG | A10~A4 | A3 | A2 | A1 | A0 | Offset | –OE=L                   | –WE=L                   |
|------|--------|----|----|----|----|--------|-------------------------|-------------------------|
| 0    | X      | 0  | 0  | 0  | 0  | 0H     | Data register           | Data register           |
| 0    | X      | 0  | 0  | 0  | 1  | 1H     | Error register          | Feature register        |
| 0    | X      | 0  | 0  | 1  | 0  | 2H     | Sector count register   | Sector count register   |
| 0    | X      | 0  | 0  | 1  | 1  | 3H     | Sector number register  | Sector number register  |
| 0    | X      | 0  | 1  | 0  | 0  | 4H     | Cylinder low register   | Cylinder low register   |
| 0    | X      | 0  | 1  | 0  | 1  | 5H     | Cylinder high register  | Cylinder high register  |
| 0    | X      | 0  | 1  | 1  | 0  | 6H     | Drive head register     | Drive head register     |
| 0    | X      | 0  | 1  | 1  | 1  | 7H     | Status register         | Command register        |
| 0    | X      | 1  | 0  | 0  | 0  | 8H     | Dup. even data register | Dup. even data register |
| 0    | X      | 1  | 0  | 0  | 1  | 9H     | Dup.odd data register   | Dup.odd data register   |
| 0    | X      | 1  | 1  | 0  | 1  | DH     | Dup.error register      | Dup.feature register    |
| 0    | X      | 1  | 1  | 1  | 0  | EH     | Alt. status register    | Device control register |
| 0    | X      | 1  | 1  | 1  | 1  | FH     | Drive address register  | Reserved                |

Primary I/O map (INDEX=2)

| –REG | A10 | A9~A4 | A3 | A2 | A1 | A0 | –IORD=L                | –IOWR=L                 |
|------|-----|-------|----|----|----|----|------------------------|-------------------------|
| 0    | X   | 1FH   | 0  | 0  | 0  | 0  | Data register          | Data register           |
| 0    | X   | 1FH   | 0  | 0  | 0  | 1  | Error register         | Feature register        |
| 0    | X   | 1FH   | 0  | 0  | 1  | 0  | Sector count register  | Sector count register   |
| 0    | X   | 1FH   | 0  | 0  | 1  | 1  | Sector number register | Sector number register  |
| 0    | X   | 1FH   | 0  | 1  | 0  | 0  | Cylinder low register  | Cylinder low register   |
| 0    | X   | 1FH   | 0  | 1  | 0  | 1  | Cylinder high register | Cylinder high register  |
| 0    | X   | 1FH   | 0  | 1  | 1  | 0  | Drive head register    | Drive head register     |
| 0    | X   | 1FH   | 0  | 1  | 1  | 1  | Status register        | Command register        |
| 0    | X   | 3FH   | 0  | 1  | 1  | 0  | Alt. status register   | Device control register |
| 0    | X   | 3FH   | 0  | 1  | 1  | 1  | Drive address register | Reserved                |

Secondary I/O map (INDEX=3)

| –REG | A10 | A9~A4 | A3 | A2 | A1 | A0 | –IORD=L                | –IOWR=L                 |
|------|-----|-------|----|----|----|----|------------------------|-------------------------|
| 0    | X   | 17H   | 0  | 0  | 0  | 0  | Data register          | Data register           |
| 0    | X   | 17H   | 0  | 0  | 0  | 1  | Error register         | Feature register        |
| 0    | X   | 17H   | 0  | 0  | 1  | 0  | Sector count register  | Sector count register   |
| 0    | X   | 17H   | 0  | 0  | 1  | 1  | Sector number register | Sector number register  |
| 0    | X   | 17H   | 0  | 1  | 0  | 0  | Cylinder low register  | Cylinder low register   |
| 0    | X   | 17H   | 0  | 1  | 0  | 1  | Cylinder high register | Cylinder high register  |
| 0    | X   | 17H   | 0  | 1  | 1  | 0  | Drive head register    | Drive head register     |
| 0    | X   | 17H   | 0  | 1  | 1  | 1  | Status register        | Command register        |
| 0    | X   | 37H   | 0  | 1  | 1  | 0  | Alt. status register   | Device control register |
| 0    | X   | 37H   | 0  | 1  | 1  | 1  | Drive address register | Reserved                |

True IDE Mode I/O map

| –CE2 | –CE1 | A2 | A1 | A0 | –IORD=L                | –IOWR=L                 |
|------|------|----|----|----|------------------------|-------------------------|
| 1    | 0    | 0  | 0  | 0  | Data register          | Data register           |
| 1    | 0    | 0  | 0  | 1  | Error register         | Feature register        |
| 1    | 0    | 0  | 1  | 0  | Sector count register  | Sector count register   |
| 1    | 0    | 0  | 1  | 1  | Sector number register | Sector number register  |
| 1    | 0    | 1  | 0  | 0  | Cylinder low register  | Cylinder low register   |
| 1    | 0    | 1  | 0  | 1  | Cylinder high register | Cylinder high register  |
| 1    | 0    | 1  | 1  | 0  | Drive head register    | Drive head register     |
| 1    | 0    | 1  | 1  | 1  | Status register        | Command register        |
| 0    | 1    | 1  | 1  | 0  | Alt. status register   | Device control register |
| 0    | 1    | 1  | 1  | 1  | Drive address register | Reserved                |

### 1. Data register

This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

|           |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|-----------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| bit15     | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| D0 to D15 |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |

### 2. Error register

This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0"(Ready).

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| BBK  | UNC  | 0    | IDNF | 0    | ABRT | 0    | AMNF |

| bit | Name                         | Function                                                                                                                             |
|-----|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BBK(Bad Block detected)      | This bit is set when a Bad Block is detected in requester ID field.                                                                  |
| 6   | UNC(Data ECC error)          | This bit is set when Uncorrectable error is occurred at reading the card.                                                            |
| 4   | IDNF(ID Not Found)           | The requested sector ID is in error or cannot be found.                                                                              |
| 2   | ABRT(ABoRTed command)        | This bit is set if the command has been aborted because of the card status condition.(Not ready, Write fault, Invalid command, etc.) |
| 0   | AMNF(Address Mark Not Found) | This bit is set in case of a general error.                                                                                          |

### 3. Feature register

This register is write-only register, and provides information regarding features of the drive that the host wishes to utilize.

|              |      |      |      |      |      |      |      |
|--------------|------|------|------|------|------|------|------|
| bit7         | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Feature byte |      |      |      |      |      |      |      |

### 4. Sector count register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

|                   |      |      |      |      |      |      |      |
|-------------------|------|------|------|------|------|------|------|
| bit7              | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Sector count byte |      |      |      |      |      |      |      |

### 5. Sector number register

This register contains the starting sector number, which is started by following sector transfer command.

|                    |      |      |      |      |      |      |      |
|--------------------|------|------|------|------|------|------|------|
| bit7               | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Sector number byte |      |      |      |      |      |      |      |

## 6. Cylinder low register

This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

|                   |      |      |      |      |      |      |      |
|-------------------|------|------|------|------|------|------|------|
| bit7              | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Cylinder low byte |      |      |      |      |      |      |      |

## 7. Cylinder high register

This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

|                    |      |      |      |      |      |      |      |
|--------------------|------|------|------|------|------|------|------|
| bit7               | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Cylinder high byte |      |      |      |      |      |      |      |

## 8. Drive head register

This register is used for selecting the Drive number and Head number for the following command.

|          |      |          |      |             |      |      |      |
|----------|------|----------|------|-------------|------|------|------|
| bit7     | bit6 | bit5     | bit4 | bit3        | bit2 | bit1 | bit0 |
| Obsolete | LBA  | Obsolete | DRV  | Head number |      |      |      |

| bit | Name               | Function                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Obsolete           | This bit is normally set to "1".                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6   | LBA                | LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA = 0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows:<br>LBA07~LBA00: Sector Number Register D7 to D0.<br>LBA15~LBA08: Cylinder Low Register D7 to D0.<br>LBA23~LBA16: Cylinder High Register D7 to D0.<br>LBA27~LBA24: Drive / Head Register bits HS3 to HS0. |
| 5   | Obsolete           | This bit is normally set to "1".                                                                                                                                                                                                                                                                                                                                                                                                                |
| 4   | DRV (Drive select) | This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.                                                                                                                                                                                                                                                            |
| 3   | Head number        | This bit is used for selecting the Head number for the following command. Bit 3 is MSB.                                                                                                                                                                                                                                                                                                                                                         |

## 9. Status register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode,  $\neg$ IREQ is negated.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| BSY  | DRDY | DWF  | DSC  | DRQ  | CORR | IDX  | ERR  |

| bit | Name                      | Function                                                                                                                                                                   |
|-----|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BSY (BuSY)                | This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.                                       |
| 6   | DRDY (Drive ReaDY)        | If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests. |
| 5   | DWF (Drive Write Fault)   | This bit is set if this card indicates the write fault status.                                                                                                             |
| 4   | DSC (Drive Seek Complete) | This bit is set when the drive seeks complete.                                                                                                                             |
| 3   | DRQ (Data ReQuest)        | This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.                  |
| 2   | CORR (CORRected data)     | This bit is set when a correctable data error has been occurred and the data has been corrected.                                                                           |
| 1   | IDX (InDeX)               | This bit is always set to "0".                                                                                                                                             |
| 0   | ERR (ERRor)               | This bit is set when the previous command has ended in some type of error. The error information is set in the error register. This bit is cleared by the next command.    |

## 10. Alternate status register

This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that  $\neg$ IREQ is not negated when data read.

## 11. Command register

This register is write only register, and it is used for writing the command to execute the requested operation. The command code is written in the command register, after the parameter is written in the Task File when the card is in Ready state.

| Command                     | Command code | Used parameter |    |    |    |    |    |     |
|-----------------------------|--------------|----------------|----|----|----|----|----|-----|
|                             |              | FR             | SC | SN | CY | DR | HD | LBA |
| Check power mode            | E5H or 98H   | N              | N  | N  | N  | Y  | N  | N   |
| Execute drive diagnostic    | 90H          | N              | N  | N  | N  | Y  | N  | N   |
| Erase sector                | C0H          | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Format track                | 50H          | N              | Y  | N  | Y  | Y  | Y  | Y   |
| Identify Drive              | ECH          | N              | N  | N  | N  | Y  | N  | N   |
| Idle                        | E3H or 97H   | N              | Y  | N  | N  | Y  | N  | N   |
| Idle immediate              | E1h or 95h   | N              | N  | N  | N  | Y  | N  | N   |
| Initialize drive parameters | 91H          | N              | Y  | N  | N  | Y  | Y  | N   |
| Read buffer                 | E4H          | N              | N  | N  | N  | Y  | N  | N   |
| Read multiple               | C4H          | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Read long sector            | 22H or 23H   | N              | N  | Y  | Y  | Y  | Y  | Y   |
| Read sector                 | 20H or 21H   | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Read verify sector          | 40h or 41h   | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Recalibrate                 | 1Xh          | N              | N  | N  | N  | Y  | N  | N   |
| Request sense               | 03H          | N              | N  | N  | N  | Y  | N  | N   |
| Seek                        | 7XH          | N              | N  | Y  | Y  | Y  | Y  | Y   |
| Set features                | EFH          | Y              | N  | N  | N  | Y  | N  | N   |
| Set multiple mode           | C6H          | N              | Y  | N  | N  | Y  | N  | N   |
| Set sleep mode              | E6h or 99h   | N              | N  | N  | N  | Y  | N  | N   |
| Stand by                    | E2h or 96h   | N              | N  | N  | N  | Y  | N  | N   |
| Stand by immediate          | E0h or 94h   | N              | N  | N  | N  | Y  | N  | N   |
| Translate sector            | 87H          | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Wear level                  | F5H          | N              | N  | N  | N  | Y  | Y  | N   |
| Write buffer                | E8H          | N              | N  | N  | N  | Y  | N  | N   |
| Write long sector           | 32h or 33h   | N              | N  | Y  | Y  | Y  | Y  | Y   |
| Write multiple              | C5H          | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Write multiple w/o erase    | CDH          | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Write sector                | 30H or 31H   | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Write sector w/o erase      | 38H          | N              | Y  | Y  | Y  | Y  | Y  | Y   |
| Write verify                | 3CH          | N              | Y  | Y  | Y  | Y  | Y  | Y   |

Notes: FR: Feature register

SC: Sector Count register

SN: Sector Number register

CY: Cylinder register

DR: DRV bit of Drive Head register

HD: Head Number of Drive Head Supported

Y: The register contains a valid parameter for this command.

N: The register does not contain a valid parameter for this command.

## 12. Device control register

This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| X    | X    | X    | X    | 1    | SRST | nIEN | 0    |

| bit    | Name                   | Function                                                                                                                                                                                                                          |
|--------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 4 | X                      | Don't care                                                                                                                                                                                                                        |
| 3      | 1                      | This bit is set to "1".                                                                                                                                                                                                           |
| 2      | SRST(Software ReSeT)   | This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0". |
| 1      | nIEN(Interrupt Enable) | This bit is used for enabling –IREQ. When this bit is set to "0", –IREQ is enabled. When this bit is set to "1", –IREQ is disabled.                                                                                               |
| 0      | 0                      | This bit is set to "0".                                                                                                                                                                                                           |

## 13. Drive Address register

This register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| X    | nWTG | nHS3 | nHS2 | nHS1 | nHS0 | nDS1 | nDS0 |

| bit    | Name                          | Function                                                                                  |
|--------|-------------------------------|-------------------------------------------------------------------------------------------|
| 7      | X                             | This bit remains tri-state when host read access.                                         |
| 6      | nWTG (WriTing Gate)           | This bit is set as 0                                                                      |
| 5 to 2 | nHS3 to nHS0 (Head Select3-0) | These bits are the negative value of Head Select bits (bit3 to 0) in Drive/Head register. |
| 1      | nDS1 (Idrive Select1)         | This bit is 0 when drive 1 is active and selected.                                        |
| 0      | nDS0 (Idrive Select0)         | This bit is 0 when drive 0 is active and selected.                                        |

**ATA Command specifications**

This table summarizes the ATA command set with the paragraphs. Following shows the supported commands and command codes, which are written in command registers.

**ATA Command Set**

| No. | Command set                 | Code       | FR | SC | SN | CY | DR | HD | LBA |
|-----|-----------------------------|------------|----|----|----|----|----|----|-----|
| 1   | Check power mode            | E5h or 98h | —  | —  | —  | —  | Y  | —  | —   |
| 2   | Execute drive diagnostic    | 90H        | —  | —  | —  | —  | Y  | —  | —   |
| 3   | Erase sector(s)             | C0H        | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 4   | Format track                | 50H        | —  | Y  | —  | Y  | Y  | Y  | Y   |
| 5   | Identify Drive              | ECH        | —  | —  | —  | —  | Y  | —  | —   |
| 6   | Idle                        | E3h or 97h | —  | Y  | —  | —  | Y  | —  | —   |
| 7   | Idle immediate              | E1h or 95h | —  | —  | —  | —  | Y  | —  | —   |
| 8   | Initialize drive parameters | 91H        | —  | Y  | —  | —  | Y  | Y  | —   |
| 9   | Read buffer                 | E4H        | —  | —  | —  | —  | Y  | —  | —   |
| 10  | Read multiple               | C4H        | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 11  | Read long sector            | 22H or 23H | —  | —  | Y  | Y  | Y  | Y  | Y   |
| 12  | Read sector (s)             | 20H or 21H | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 13  | Read verify sector (s)      | 40H or 41H | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 14  | Recalibrate                 | 1XH        | —  | —  | —  | —  | Y  | —  | —   |
| 15  | Request sense               | 03H        | —  | —  | —  | —  | Y  | —  | —   |
| 16  | Seek                        | 7XH        | —  | —  | Y  | Y  | Y  | Y  | Y   |
| 17  | Set features                | EFH        | Y  | —  | —  | —  | Y  | —  | —   |
| 18  | Set multiple mode           | C6H        | —  | Y  | —  | —  | Y  | —  | —   |
| 19  | Set sleep mode              | E6h or 99h | —  | —  | —  | —  | Y  | —  | —   |
| 20  | Stand by                    | E2h or 96h | —  | —  | —  | —  | Y  | —  | —   |
| 21  | Stand by immediate          | E0h or 94h | —  | —  | —  | —  | Y  | —  | —   |
| 22  | Translate sector            | 87H        | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 23  | Wear level                  | F5H        | —  | —  | —  | —  | Y  | Y  | —   |
| 24  | Write buffer                | E8H        | —  | —  | —  | —  | Y  | —  | —   |
| 25  | Write long sector           | 32H or 33H | —  | —  | Y  | Y  | Y  | Y  | Y   |
| 26  | Write multiple              | C5H        | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 27  | Write multiple w/o erase    | CDH        | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 28  | Write sector                | 30H or 31H | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 29  | Write sector w/o erase      | 38H        | —  | Y  | Y  | Y  | Y  | Y  | Y   |
| 30  | Write verify                | 3CH        | —  | Y  | Y  | Y  | Y  | Y  | Y   |

Notes: FR: Feature register

SC: Sector Count register (00H~FFH)

SN: Sector Number register (01H~20H)

CY: Cylinder Low / High register

DR: Drive bit of Drive / Head register

HD: Head No.(0~3) of Drive / Head register

LBA: Logical Block Address Mode supported

Y: Set up

—: Not set up

- (1) Check Power Mode (code: E5h or 98h): This command checks the power mode.
- (2) Execute Drive Diagnostic (code: 90h): This command performs the internal diagnostic tests implemented by the Card.
- (3) Erase Sector(s)(code: C0h): This command is used to erase data sectors.
- (4) Format Track (code: 50h): This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the card expects one sector (512Bytes) of data from the host to follow the command with same protocol as the Write Sector Command.
- (5) Identify Drive (code: ECh): This command enables the host to receive parameter information from the Card.

#### Identify Drive Information

| Word address | Default value | Total bytes | Data field type information                                  |
|--------------|---------------|-------------|--------------------------------------------------------------|
| 0            | 848AH         | 2           | General configuration bit-significant information            |
| 1            | XXXX          | 2           | Default number of cylinders                                  |
| 2            | 0000H         | 2           | Reserved                                                     |
| 3            | 00XXH         | 2           | Default number of heads                                      |
| 4            | 0000H         | 2           | Number of unformatted bytes per track                        |
| 5            | XXXX          | 2           | Number of unformatted bytes per sector                       |
| 6            | XXXX          | 2           | Default number of sectors per track                          |
| 7 to 8       | XXXX          | 4           | Number of sectors per card(Word7=MSW,Words=LSW)              |
| 9            | 0000H         | 2           | Reserved                                                     |
| 10 to 19     | XXXX          | 20          | Serial number in ASCII                                       |
| 20           | 0001H         | 2           | Buffer type (single ported)                                  |
| 21           | 0004H         | 2           | Buffer size in 512 byte increments                           |
| 22           | 0004H         | 2           | # of ECC bytes passed on Read/Write Long Commands            |
| 23 to 46     | XXXX          | 48          | Firmware revision in ASCII etc.                              |
| 47           | 0001H         | 2           | Maximum of 1 sector on Read/Write Multiple command           |
| 48           | 0000H         | 2           | Double Word not supported                                    |
| 49           | 0200H         | 2           | Capabilities: DMA NOT Supported(bit 8), LBA supported (bit9) |
| 50           | 0000H         | 2           | Reserved                                                     |
| 51           | 0200H         | 2           | PIO data transfer cycle timing mode 2                        |
| 52           | 0000H         | 2           | DMA data transfer cycle timing mode not Supported            |
| 53 to 58     | XXXX          | 12          | Reserved                                                     |
| 59           | 0101H         | 2           | Multiple sector setting is valid                             |
| 60 to 61     | XXXX          | 4           | Total number of sectors addressable in LBA Mode              |
| 62 to 255    | 0000H         | 388         | Reserved                                                     |

- (6) Idle (code: E3h or 97h): This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.
- (7) Idle Immediate (code: E1h or 95h): This command causes the Card to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.
- (8) Initialize Drive Parameters (code: 91h): This command enables the host to set the number of sectors per track and the number of heads per cylinder.
- (9) Read Buffer (code: E4h): This command enables the host to read the current contents of the card's sector buffer.
- (10) Read Multiple (code: C4h): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.

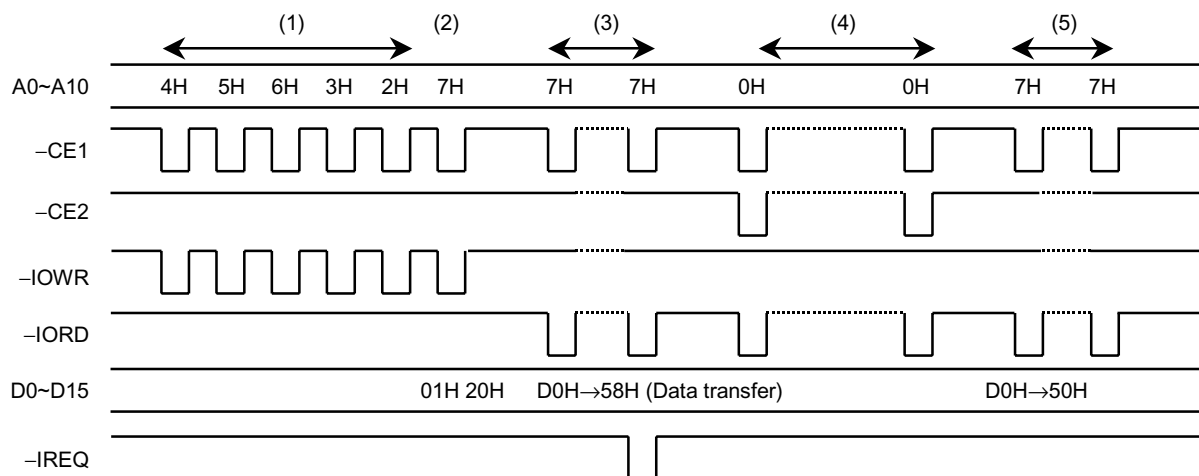
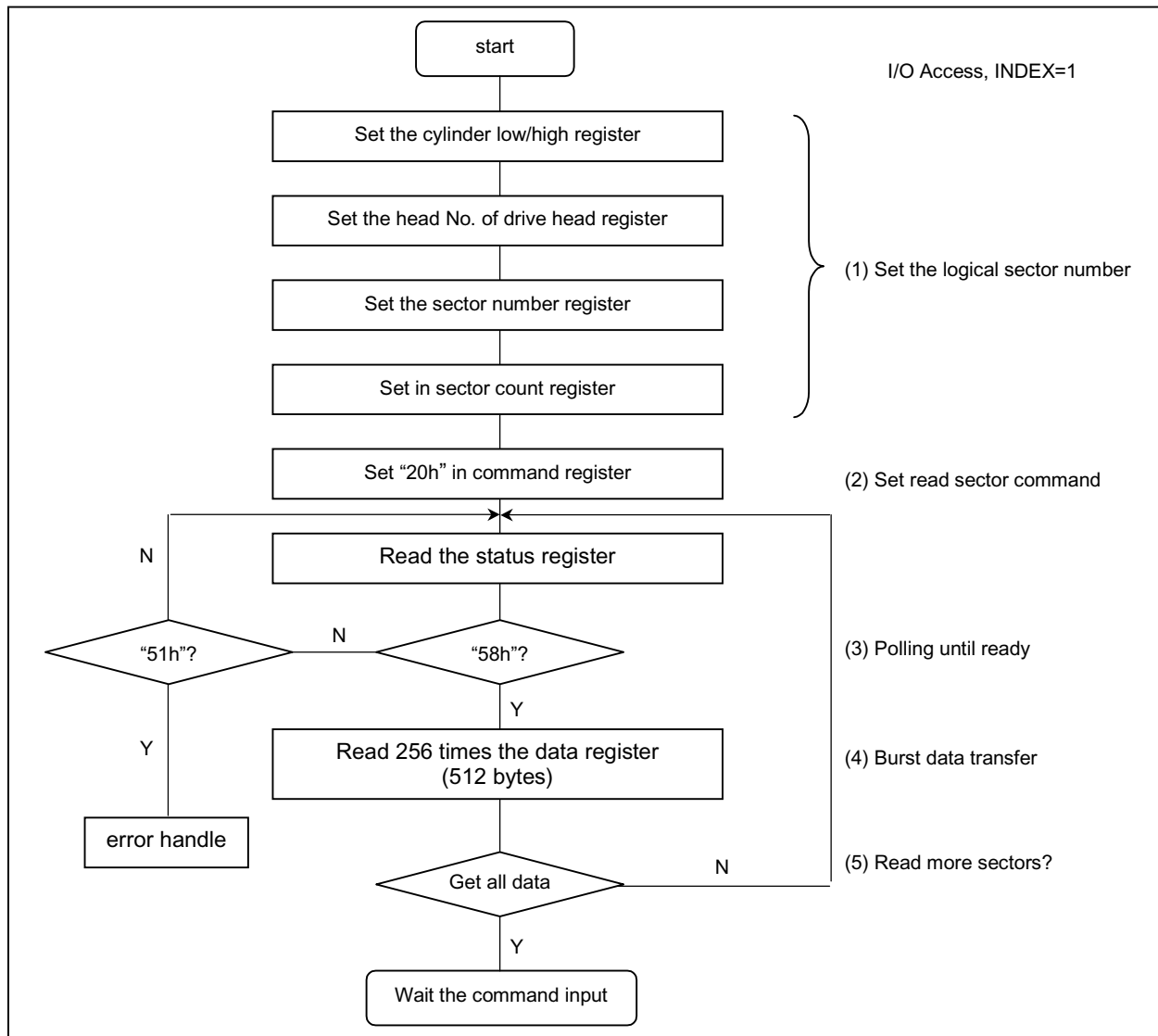
- (11) Read Long Sector (code: 22h or 23h): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
- (12) Read Sector(s) (code: 20h or 21h): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.
- (13) Read Verify Sector(s) (code: 40h or 41h): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
- (14) Recalibrate (code: 1Xh): This command is effectively a NOP command to the Card and is provided for compatibility purposes.
- (15) Request Sense (code: 03h): This command requests an extended error code after command ends with an error.
- (16) Seek (code: 7Xh): This command is effectively a NOP command to the Card although it does perform a range check.
- (17) Set Features (code: EFh): This command is used by the host to establish or select certain features.

| Features | Operation                                                             |
|----------|-----------------------------------------------------------------------|
| 01H      | Enable 8-bit data transfers.                                          |
| 55H      | Disable Read Look Ahead.                                              |
| 66H      | Disable Power on Reset (POR) establishment of defaults at Soft Reset. |
| 81H      | Disable 8-bit data transfers.                                         |
| BBH      | 4 bytes of data apply on Read/Write Long commands.                    |
| CCH      | Enable Power on Reset (POR) establishment of defaults at Soft Reset.  |

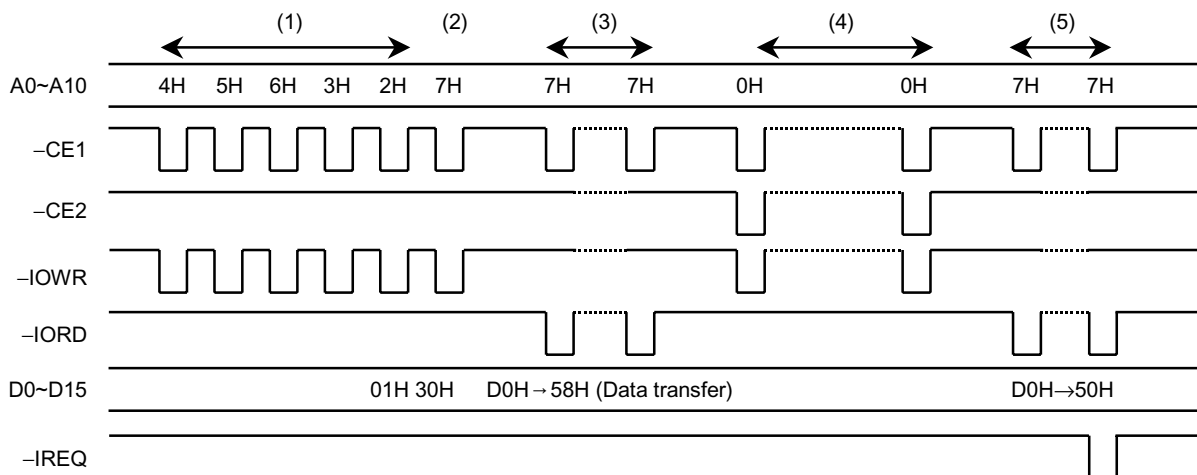
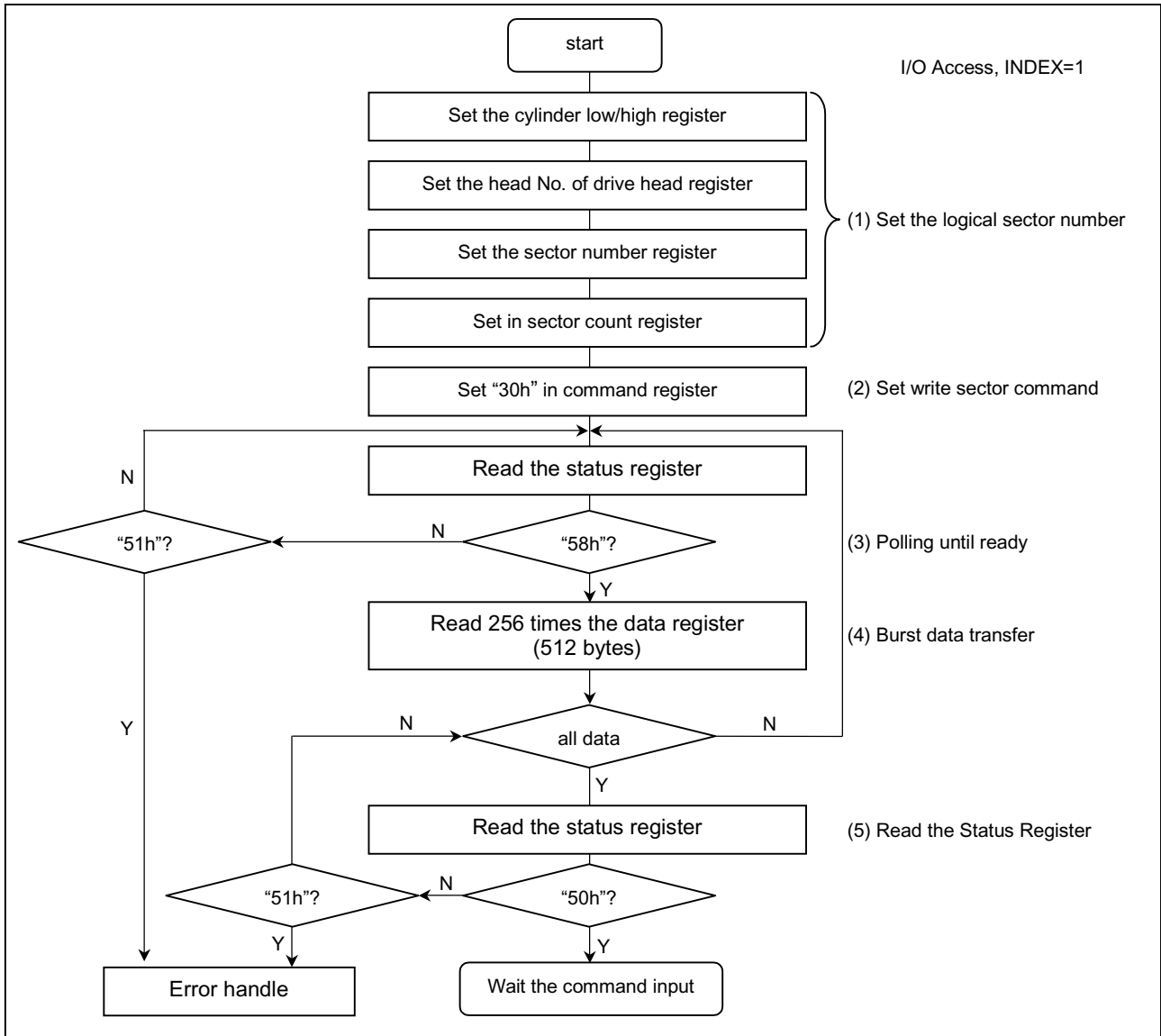
- (18) Set Multiple Mode (code: C6h): This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.
- (19) Set Sleep Mode (code: E6h or 99h): This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.
- (20) Stand By (code: E2h or 96h): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
- (21) Stand By Immediate (code: E0h or 94h): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
- (22) Translate Sector (code: 87h): This command allows the host a method of determining the exact number of times a use sector has been erased and programmed.
- (23) Wear Level (code: F5h): This command effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00h indicating Wear Level is not needed.
- (24) Write Buffer (code: E8h): This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.
- (25) Write Long Sector (code: 32h or 33h): This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
- (26) Write Multiple (code: C5h): This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
- (27) Write Multiple without Erase (code: CDh): This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.
- (28) Write Sector(s): (code: 30h or 31h): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
- (29) Write Sector(s) without Erase (code: 38h): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.
- (30) Write Verify (code: 3Ch): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

### Sector Transfer Protocol

1. Sector read: Sector read procedure after the card configured I/O interface is shown as follows.



2. Sector write: write sector procedure after the card configured I/O interface is shown as follows.



**Card System performance**

| ITEM                                            | Performance                                     |
|-------------------------------------------------|-------------------------------------------------|
| Set up times (Reset to Ready)                   | 400 ms (max.) *1                                |
| Set up times (Sleep to Idle)                    | 100μs (max.)                                    |
| Set up times (Deep Power Down to Idle)          | 4 ms (max.)                                     |
| Data transfer rate to / from host               | 16.6 M byte / s burst (max.), theoretically     |
| Sustained read transfer rate                    | 6.5 M byte / s (max.), actually *2              |
| Sustained write transfer rate                   | 1.5 M byte / s (max.) <8MB~48MB>, actually *2   |
| Sustained write transfer rate                   | 3.2 M byte / s (max.) <64MB~512MB>, actually *2 |
| Controller overhead (Command to DRQ)            | 4 ms (max.)                                     |
| Data transfer cycle end to ready (Sector write) | 500μs (typ.), 50ms (max.)                       |

Notes:

1. This parameter will be changed for different capacity and NAND type flash memory, the typical set up time for 2 Giga Bytes flash card is 325ms
2. The actual transfer rate is measured under ATA PIO mode 4 with single cycle time as 120ns.

**ELECTRICAL SPECIFICATION**

| SYMBOL                             | PARAMETER                                                 | MIN  | MAX                   | TYP | UNIT | NOTES               |
|------------------------------------|-----------------------------------------------------------|------|-----------------------|-----|------|---------------------|
| V <sub>IN</sub> , V <sub>OUT</sub> | All input / output voltage                                | -0.3 | V <sub>CC</sub> + 0.3 | —   | V    |                     |
| V <sub>CC</sub>                    | Power Supply Voltage<br>(Absolute Maximum Ratings)        | -0.6 | 6.0                   | —   | V    |                     |
| V <sub>CC</sub>                    | Power Supply Voltage<br>(Recommended Operation Condition) | 4.5  | 5.5                   | 5.0 | V    |                     |
|                                    |                                                           | 3.0  | 3.6                   | 3.3 | V    |                     |
| T <sub>opr</sub>                   | Operating Temperature                                     | 0    | 70                    | 25  | °C   | Commercial grade *1 |
|                                    |                                                           | -40  | 85                    | —   | °C   | Industrial grade *2 |
| T <sub>stg</sub>                   | Storage Temperature                                       | -20  | 85                    | —   | °C   | Commercial grade *1 |
|                                    |                                                           | -45  | 90                    | —   | °C   | Industrial grade *2 |

Notes:

1. THNCFxxxMBA Series (Commercial grade)
2. THNCFxxxMBAI Series (Industrial grade)

## Input Leakage Current

| Type | SYMBOL | PARAMETER             | CONDIDTION                   | MIN | MAX | TYP | UNIT | NOTES |
|------|--------|-----------------------|------------------------------|-----|-----|-----|------|-------|
| IxZ  | IL     | Input leakage current | $V_{IH}=V_{CC} / V_{IL}=GND$ | -1  | 1   | —   | uA   | *1    |
| IxU  | RPU1   | Pull Up Resistor      | $V_{CC} = 5.0V$              | 50  | 500 | —   | kΩ   | *1    |
| IxD  | RPD1   | Pull Down Resister    | $V_{CC} = 5.0V$              | 50  | 500 | —   |      | *1    |

Notes:

1. x refers to the characteristics described in section “DC Characteristics ( Input Characteristics)”. For example, I1U indicates a pull up resistor with a type 1 input characteristics.

## Output Drive Type

| Type | OUTPUT TYPE           | VALID CONDITIONS    | NOTES |
|------|-----------------------|---------------------|-------|
| OTx  | Totempole             | $I_{OH}$ & $I_{OL}$ | *1    |
| OZx  | Tri-State N-P Channel | $I_{OH}$ & $I_{OL}$ | *1    |
| OPx  | P-Channel only        | $I_{OH}$ Only       | *1    |
| ONx  | N-Channel only        | $I_{OL}$ Only       | *1    |

Notes:

1. x refers to the characteristics described in section “DC Characteristics ( Output Drive Characteristics)”. For example, OT1 refers to Totempole output with a type 1 Output drive characteristics.

**DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$ ,  $V_{CC} = 5\text{ V} \pm 0.5\text{V}$ )

Ta = 0°C~70°C for THNCFxxxMBA (Commercial grade)

Ta = -40°C~85°C for THNCFxxxMBAI (Industrial grade)

| SYMBOL    | PARAMETER                       | MIN | MAX        | TYP.        | UNIT                        | TEST CONDITIONS                                |
|-----------|---------------------------------|-----|------------|-------------|-----------------------------|------------------------------------------------|
| $I_{LI}$  | Input leakage current           | —   | 1          | —           | $\mu\text{A}$               | —                                              |
| $I_{LO}$  | Output leakage current          | —   | 1          |             | $\mu\text{A}$               | $V_{OUT} = \text{high impedance}$              |
| $-I_{PU}$ | Pull-up current (Resistivity)   | —   | —          | 43 (75)     | $\mu\text{A}$ (k $\Omega$ ) | $V_{FORCE} = 3.3\text{V}$                      |
| $-I_{PD}$ | Pull-down current (Resistivity) | —   | —          | -48 / (206) | $\mu\text{A}$ (k $\Omega$ ) | $V_{FORCE} = 0\text{V}$                        |
| $I_{CCS}$ | Sleep mode current              | —   | 1.5<br>2.0 | 1.0<br>1.2  | mA                          | $V_{CC} = 3.3\text{V}$<br>$V_{CC} = 5\text{V}$ |
| $I_{CCO}$ | Operating current @ 3.3V        |     |            |             |                             |                                                |
|           | Write operation                 | —   | —          | 38          | mA                          | $V_{CC} = 3.3\text{V}$ operation               |
|           | Read operation                  | —   | —          | 30          |                             |                                                |
|           | Operating current @ 5V          |     |            |             |                             |                                                |
|           | Write operation                 | —   | —          | 43          | mA                          | $V_{CC} = 5\text{V}$ operation                 |
|           | Read operation                  | —   | —          | 35          |                             |                                                |

## Input Characteristics

| Type | SYMBOL   | PARAMETER                                                        | MIN        | MAX        | TYP.       | UNIT | CONDITION                                        |
|------|----------|------------------------------------------------------------------|------------|------------|------------|------|--------------------------------------------------|
| 1    | $V_{IH}$ | Input High Voltage CMOS<br>(5V Tolerance)                        | 2.0<br>2.0 | —          | —          | V    | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
|      | $V_{IL}$ | Input Low Voltage CMOS<br>(5V Tolerance)                         | —          | 1.0<br>1.0 | —          |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
| 2    | $V_{IH}$ | Input High Voltage<br>(3.3V : CMOS 5V: TTL)                      | 2.0<br>2.0 | —          | —          |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
|      | $V_{IL}$ | Input Low Voltage CMOS<br>(3.3V : CMOS 5V: TTL)                  | —          | 1.0<br>0.8 | —          |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
| 3    | $V_{T+}$ | Input High Voltage CMOS with Schmitt trigger<br>(5V Tolerance)   | —          | 2.5<br>2.5 | 2.1<br>2.1 |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
|      | $V_{T-}$ | Input Low Voltage CMOS with Schmitt trigger<br>(5V Tolerance)    | 0.9<br>0.9 | —          | 1.2<br>1.2 |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
| 4    | $V_{T+}$ | Input High Voltage with Schmitt trigger<br>(3.3V : CMOS 5V: TTL) | —          | 2.3<br>2.0 | 2.1<br>1.8 |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |
|      | $V_{T-}$ | Input Low Voltage with Schmitt trigger<br>(3.3V : CMOS 5V: TTL)  | 1.0<br>0.8 | —          | 1.2<br>1.1 |      | $V_{CC} = 3.3\text{ V}$<br>$V_{CC} = 5\text{ V}$ |

## Output Drive Characteristics

| Type | SYMBOL   | PARAMETER           | MIN            | MAX       | TYP. | UNIT | CONDITION              |
|------|----------|---------------------|----------------|-----------|------|------|------------------------|
| 1    | $V_{OH}$ | Output High Voltage | $V_{CC} - 0.8$ | —         | —    | V    | $I_{OH} = -4\text{mA}$ |
|      | $V_{OL}$ | Output Low Voltage  | —              | Gnd + 0.4 | —    |      | $I_{OL} = 4\text{mA}$  |

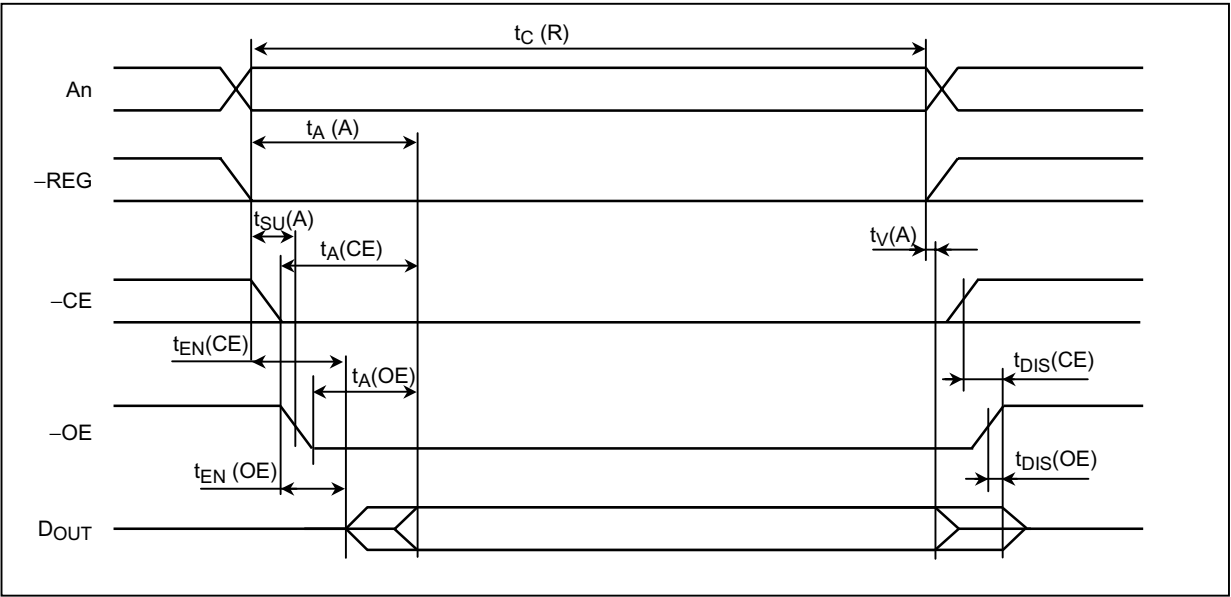
**AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$ ,  $V_{CC} = 5\text{ V} \pm 0.5\text{V}$ )

Ta = 0°C~70°C for THNCFxxxMBA (Commercial grade)  
Ta = -40°C~85°C for THNCFxxxMBAI (Industrial grade)

Attribute Memory Read AC Characteristics

| SYMBOL                | PARAMETER                 | MIN | MAX | TYP | UNIT | NOTES |
|-----------------------|---------------------------|-----|-----|-----|------|-------|
| t <sub>CR</sub>       | Read cycle time           | 250 | —   | —   | ns   |       |
| t <sub>A</sub> (A)    | Address access time       | —   | 250 | —   |      |       |
| t <sub>A</sub> (CE)   | –CE access time           | —   | 250 | —   |      |       |
| t <sub>A</sub> (OE)   | –OE access time           | —   | 125 | —   |      |       |
| t <sub>DIS</sub> (CE) | Output disable time (–CE) | —   | 100 | —   |      |       |
| t <sub>DIS</sub> (OE) | Output disable time (–OE) | —   | 100 | —   |      |       |
| t <sub>EN</sub> (CE)  | Output enable time (–CE)  | 5   | —   | —   |      |       |
| t <sub>EN</sub> (OE)  | Output enable time (–OE)  | 5   | —   | —   |      |       |
| t <sub>V</sub> (A)    | Data valid time (A)       | 0   | —   | —   |      |       |
| t <sub>SU</sub> (A)   | Address setup time        | 30  | —   | —   |      |       |

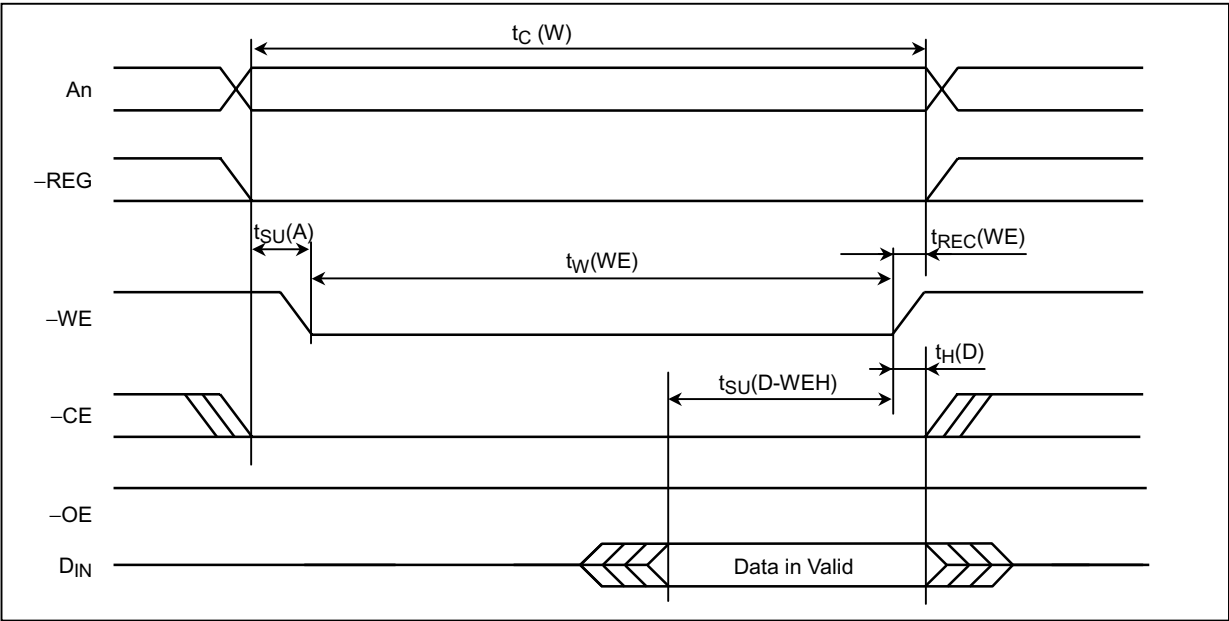
Attribute Memory Read Timing



Attribute Memory Write AC Characteristics

| SYMBOL           | PARAMETER             | MIN | MAX | TYP | UNIT | NOTES |
|------------------|-----------------------|-----|-----|-----|------|-------|
| $t_{CW}$         | Write cycle time      | 250 | —   | —   | ns   |       |
| $t_W$ (WE)       | Write pulse time      | 150 | —   | —   |      |       |
| $t_{SU}$ (A)     | Address setup time    | 30  | —   | —   |      |       |
| $t_{SU}$ (D-WEH) | Data setup time (–WE) | 80  | —   | —   |      |       |
| $t_H$ (D)        | Data hold time        | 30  | —   | —   |      |       |
| $t_{REC}$ (WE)   | Write recover time    | 30  | —   | —   |      |       |

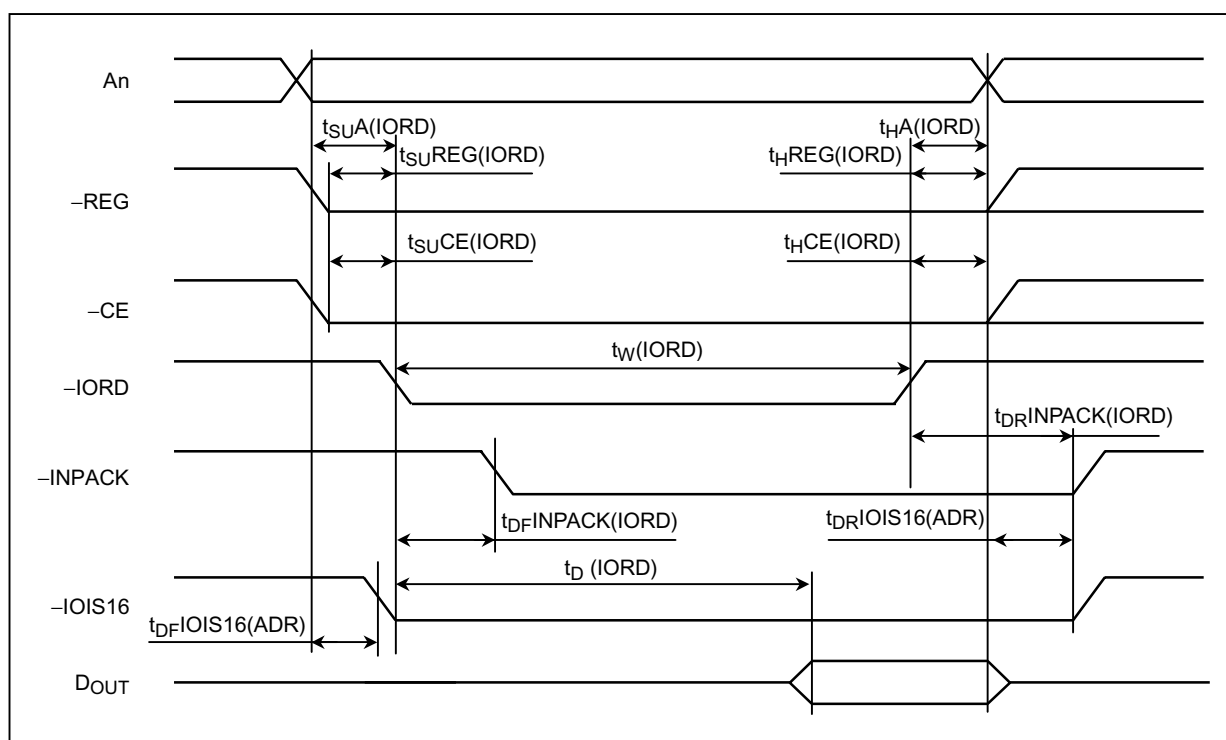
Attribute Memory Read Timing



## I/O Access Read AC Characteristics

| SYMBOL                 | PARAMETER                                    | MIN | MAX | TYP | UNIT | NOTES |
|------------------------|----------------------------------------------|-----|-----|-----|------|-------|
| $t_D$ (IORD)           | Data delay after $\neg$ IORD                 | —   | 100 | —   | ns   |       |
| $t_H$ (IORD)           | Data hold following $\neg$ IORD              | 0   | —   | —   |      |       |
| $t_W$ (IORD)           | $\neg$ IORD pulse width                      | 165 | —   | —   |      |       |
| $t_{SU A}$ (IORD)      | Address setup before $\neg$ IORD             | 70  | —   | —   |      |       |
| $t_{H A}$ (IORD)       | Address hold following $\neg$ IORD           | 20  | —   | —   |      |       |
| $t_{SU CE}$ (IORD)     | $\neg$ CE setup before $\neg$ IORD           | 5   | —   | —   |      |       |
| $t_{H CE}$ (IORD)      | $\neg$ CE hold following $\neg$ IORD         | 20  | —   | —   |      |       |
| $t_{SU REG}$ (IORD)    | $\neg$ REG setup before $\neg$ IORD          | 5   | —   | —   |      |       |
| $t_{H REG}$ (IORD)     | $\neg$ REG hold following $\neg$ IORD        | 0   | —   | —   |      |       |
| $t_{DF INPACK}$ (IORD) | $\neg$ INPACK delay falling from $\neg$ IORD | 0   | 45  | —   |      |       |
| $t_{DR INPACK}$ (IORD) | $\neg$ INPACK delay rising from $\neg$ IORD  | —   | 45  | —   |      |       |
| $t_{DF IOIS16}$ (ADR)  | $\neg$ IOIS16 delay falling from address     | —   | 35  | —   |      |       |
| $t_{DR IOIS16}$ (ADR)  | $\neg$ IOIS16 delay rising from address      | —   | 35  | —   |      |       |

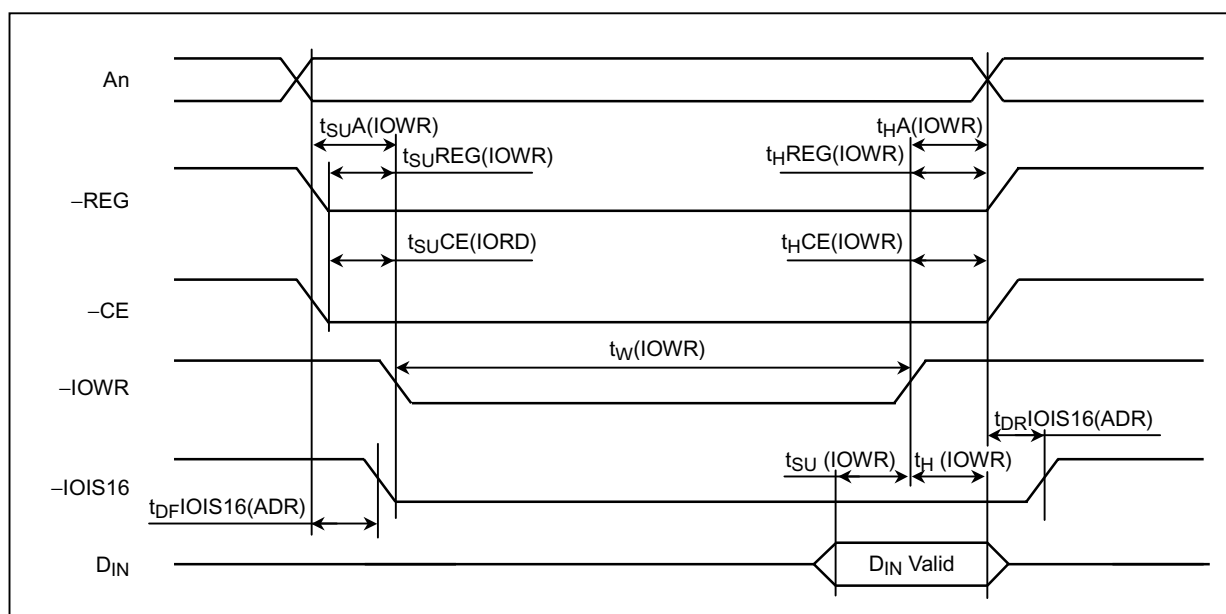
## I/O Access Read Timing



## I/O Access Write AC Characteristics

| SYMBOL                      | PARAMETER                                     | MIN | MAX | TYP | UNIT | NOTES |
|-----------------------------|-----------------------------------------------|-----|-----|-----|------|-------|
| $t_{SU}(\text{IOWR})$       | Data setup before $\text{--IOWR}$             | 60  | —   | —   | ns   |       |
| $t_H(\text{IOWR})$          | Data hold following $\text{--IOWR}$           | 30  | —   | —   |      |       |
| $t_W(\text{IOWR})$          | $\text{--IOWR}$ pulse width                   | 165 | —   | —   |      |       |
| $t_{SU A}(\text{IOWR})$     | Address setup before $\text{--IOWR}$          | 70  | —   | —   |      |       |
| $t_{H A}(\text{IOWR})$      | Address hold following $\text{--IOWR}$        | 20  | —   | —   |      |       |
| $t_{SU CE}(\text{IOWR})$    | $\text{--CE}$ setup before $\text{--IOWR}$    | 5   | —   | —   |      |       |
| $t_{H CE}(\text{IOWR})$     | $\text{--CE}$ hold following $\text{--IOWR}$  | 20  | —   | —   |      |       |
| $t_{SU REG}(\text{IORD})$   | $\text{--REG}$ setup before $\text{--IOWR}$   | 5   | —   | —   |      |       |
| $t_{H REG}(\text{IOWR})$    | $\text{--REG}$ hold following $\text{--IOWR}$ | 0   | —   | —   |      |       |
| $t_{DF IOIS16}(\text{ADR})$ | $\text{--IOIS16}$ delay falling from address  | —   | 35  | —   |      |       |
| $t_{DR IOIS16}(\text{ADR})$ | $\text{--IOIS16}$ delay rising from address   | —   | 35  | —   |      |       |

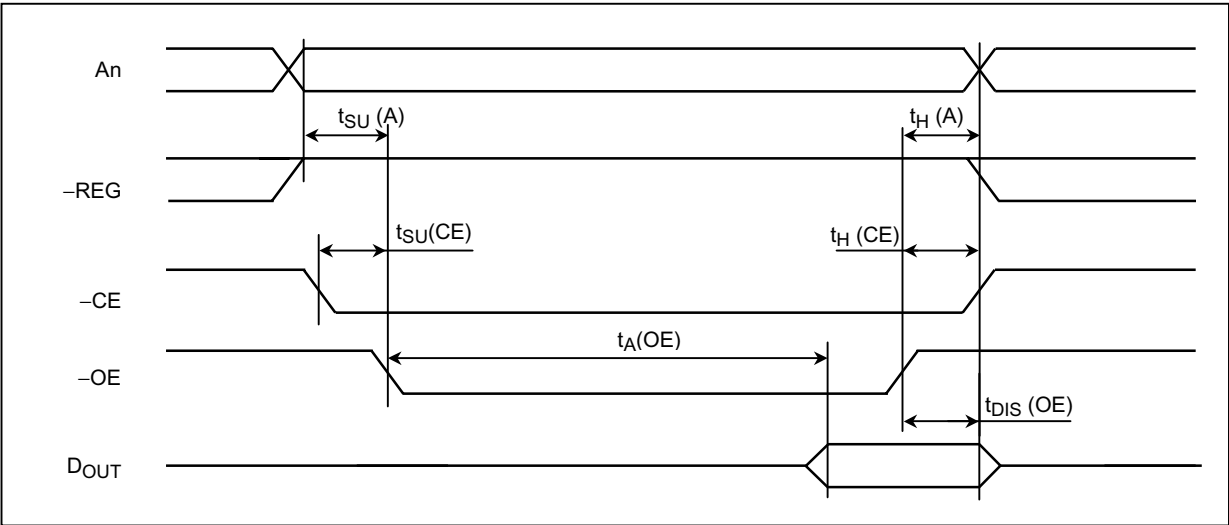
## I/O Access Write Timing



Common Memory Access Read AC Characteristics

| SYMBOL         | PARAMETER                 | MIN | MAX | TYP | UNIT | NOTES |
|----------------|---------------------------|-----|-----|-----|------|-------|
| $t_A$ (OE)     | –OE access time           | —   | 125 | —   | ns   |       |
| $t_{DIS}$ (OE) | Output disable time (–OE) | —   | 100 | —   |      |       |
| $t_{SU}$ (A)   | Address setup time        | 30  | —   | —   |      |       |
| $t_H$ (A)      | Address hold time         | 20  | —   | —   |      |       |
| $t_{SU}$ (CE)  | –CE setup time            | 0   | —   | —   |      |       |
| $t_H$ (CE)     | –OE hold time             | 20  | —   | —   |      |       |

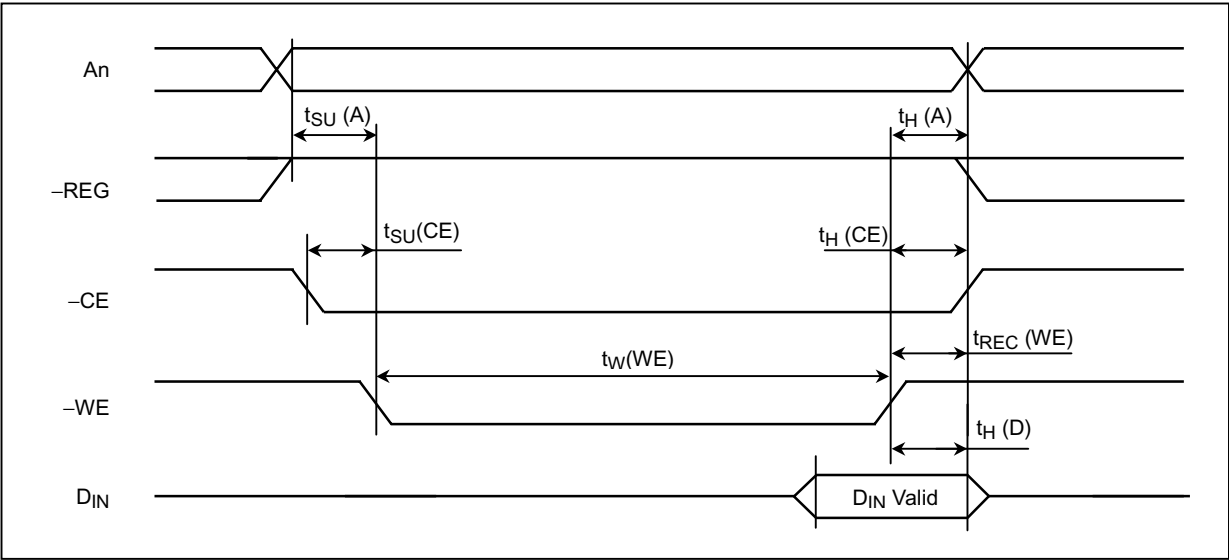
Common Memory Access Read Timing



Common Memory Access Write AC Characteristics

| SYMBOL           | PARAMETER                  | MIN | MAX | TYP | UNIT | NOTES |
|------------------|----------------------------|-----|-----|-----|------|-------|
| $t_{SU} (D-WEH)$ | Data setup time ( $-WE$ )  | 80  | —   | —   | ns   |       |
| $t_H (D)$        | Data hold time             | 30  | —   | —   |      |       |
| $t_W (WE)$       | Write pulse time           | 150 | —   | —   |      |       |
| $t_H (A)$        | Address hold time          | 20  | —   | —   |      |       |
| $t_{SU} (A)$     | Address setup time         | 30  | —   | —   |      |       |
| $t_{SU} (CE)$    | $-CE$ setup time           | 0   | —   | —   |      |       |
| $t_{REC} (WE)$   | Write recover time         | 30  | —   | —   |      |       |
| $t_H (CE)$       | $-CE$ hold following $-WE$ | 20  | —   | —   |      |       |

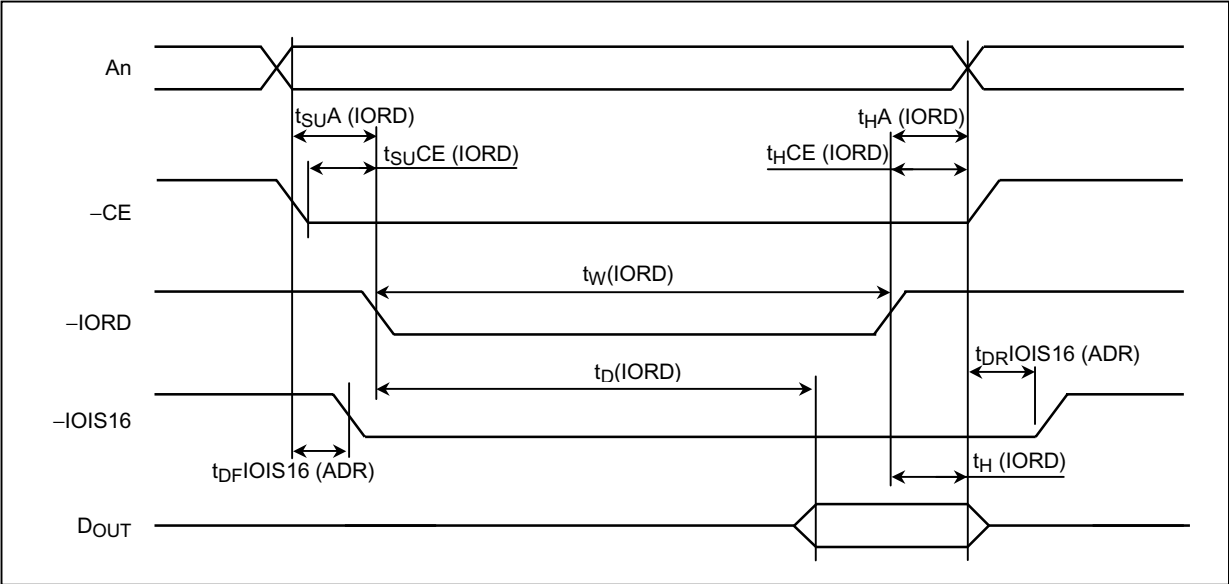
Common Memory Access Write Timing



True IDE Mode Access Read AC Characteristics

| SYMBOL               | PARAMETER                                | MIN | MAX | TYP | UNIT | NOTES |
|----------------------|------------------------------------------|-----|-----|-----|------|-------|
| $t_D$ (IORD)         | Data delay after $\neg$ IORD             | —   | 100 | —   | ns   |       |
| $t_H$ (IORD)         | Data hold following $\neg$ IORD          | 0   | —   | —   |      |       |
| $t_W$ (IORD)         | $\neg$ IORD width time                   | 165 | —   | —   |      |       |
| $t_{SUA}$ (IORD)     | Address setup before $\neg$ IORD         | 70  | —   | —   |      |       |
| $t_{HA}$ (IORD)      | Address hold following $\neg$ IORD       | 20  | —   | —   |      |       |
| $t_{SUC E}$ (IORD)   | $\neg$ CE setup before $\neg$ IORD       | 5   | —   | —   |      |       |
| $t_{HCE}$ (IORD)     | $\neg$ CE hold following $\neg$ IORD     | 20  | —   | —   |      |       |
| $t_{DFIOIS16}$ (ADR) | $\neg$ IOIS16 delay falling from address | —   | 35  | —   |      |       |
| $t_{SFIOIS16}$ (ADR) | $\neg$ IOIS16 delay rising from address  | —   | 35  | —   |      |       |

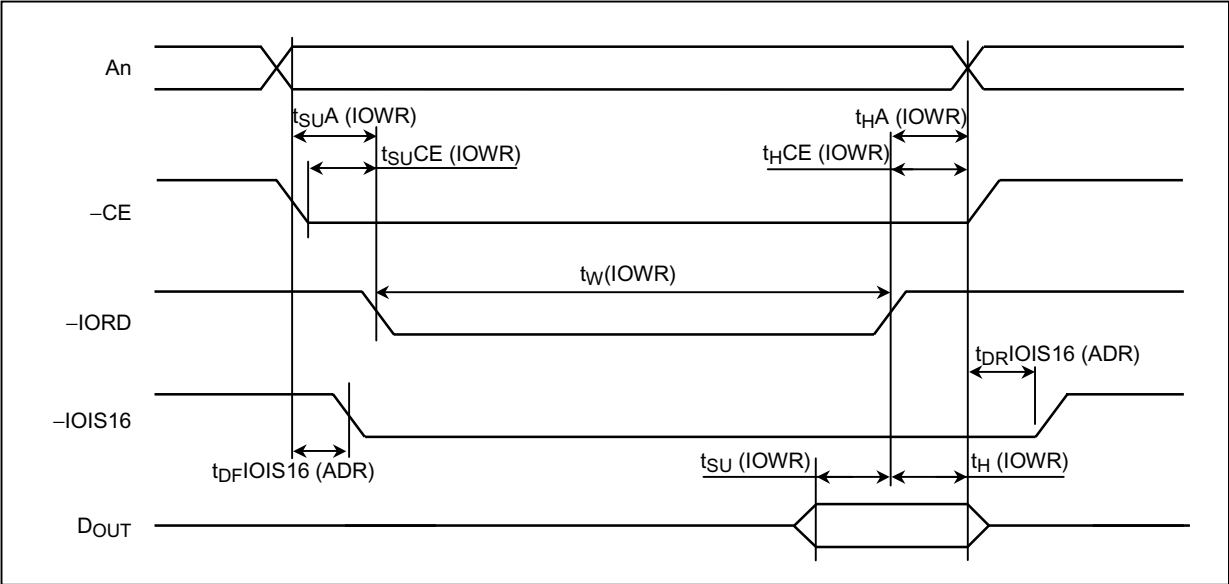
True IDE Mode Access Read Timing



True IDE Mode Access Write AC Characteristics

| SYMBOL               | PARAMETER                                | MIN | MAX | TYP | UNIT | NOTES |
|----------------------|------------------------------------------|-----|-----|-----|------|-------|
| $t_{SU} (IOWR)$      | Data setup before $\neg IOWR$            | 60  | —   | —   | ns   |       |
| $t_H (IOWR)$         | Data hold following $\neg IOWR$          | 30  | —   | —   |      |       |
| $t_W (IOWR)$         | $\neg IOWR$ width time                   | 165 | —   | —   |      |       |
| $t_{SUA} (IOWR)$     | Address setup before $\neg IOWR$         | 70  | —   | —   |      |       |
| $t_{HA} (IOWR)$      | Address hold following $\neg IOWR$       | 20  | —   | —   |      |       |
| $t_{SUC E} (IOWR)$   | $\neg CE$ setup before $\neg IOWR$       | 5   | —   | —   |      |       |
| $t_{HCE} (IOWR)$     | $\neg CE$ hold following $\neg IOWR$     | 20  | —   | —   |      |       |
| $t_{DFIOIS16} (ADR)$ | $\neg IOIS16$ delay falling from address | —   | 35  | —   |      |       |
| $t_{SFIOIS16} (ADR)$ | $\neg IOIS16$ delay rising from address  | —   | 35  | —   |      |       |

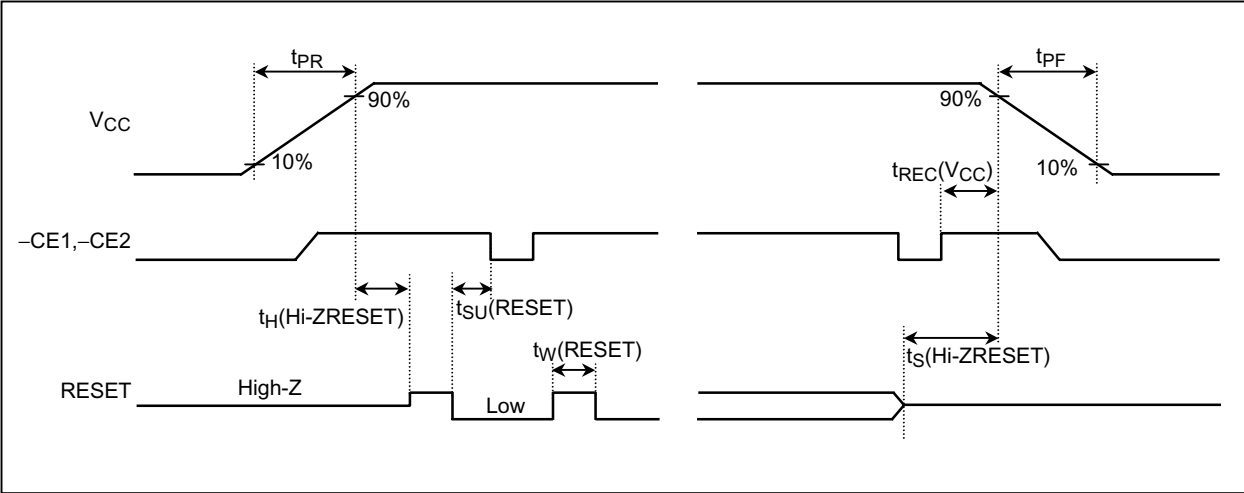
True IDE Mode Access Write Timing



Reset Characteristics (only Memory Card Mode or I/O Card Mode)

| SYMBOL            | PARAMETER             | MIN | MAX | TYP | UNIT    | NOTES |
|-------------------|-----------------------|-----|-----|-----|---------|-------|
| $t_{SU}$ (RESET)  | Reset setup time      | 100 | —   | —   | ms      |       |
| $t_{REC}$ (VCC)   | –CE recover time      | 1   | —   | —   | $\mu$ s |       |
| $t_{PR}$          | VCC rising up time    | 0.1 | 100 | —   | ms      |       |
| $t_{PF}$          | VCC falling down time | 3   | 300 | —   | ms      |       |
| $t_W$ (RESET)     | Reset pulse width     | 10  | —   | —   | $\mu$ s |       |
| $t_H$ (Hi-ZRESET) |                       | 1   | —   | —   | ms      |       |
| $t_S$ (Hi-ZRESET) |                       | 0   | —   | —   | ms      |       |

Hardware Reset Timing

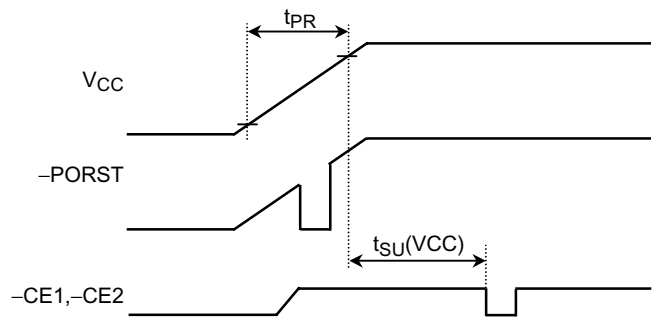


Power on Reset Characteristics

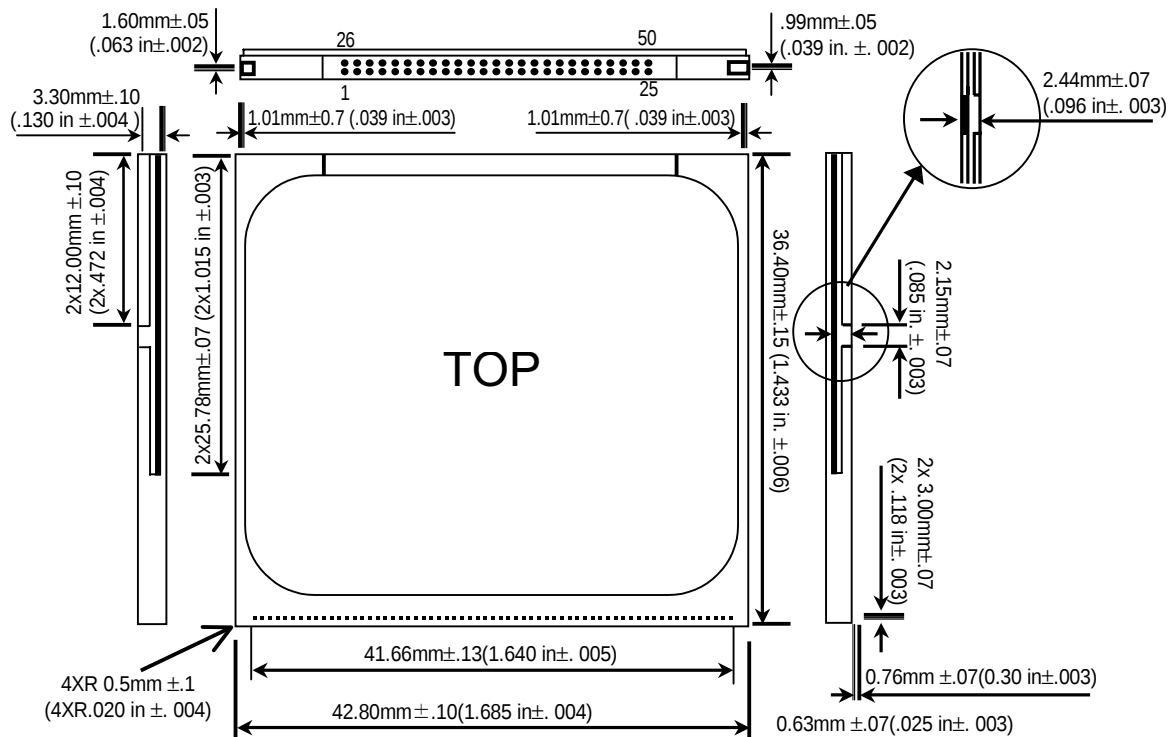
Power on reset sequence must need by  $\text{-PORST}$  at the rising of  $V_{CC}$ .

| SYMBOL           | PARAMETER               | MIN | MAX | TYP | UNIT | NOTES |
|------------------|-------------------------|-----|-----|-----|------|-------|
| $t_{SU}(V_{CC})$ | $\text{-CE}$ setup time | 100 | —   | —   | ms   |       |
| $t_{PR}$         | $V_{CC}$ rising up time | 0.1 | 100 | —   | ms   |       |

Power on Reset Timing



### Package Dimensions



Note: The optional notched configuration was shown in the CF Specification Rev.1.0. In Specification Rev. 1.2. The notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

### Type CompactFlash Storage Card Dimensions

**Attention for Card Use**

- In the reset or power off, the information of all registers is cleared.
- Notice that the card insertion/removal should not be executed during host is active, if the card is used in True IDE mode.
- After the card hard reset, soft reset, or power on reset, ATA reset, command applied the card cannot access during +RDY / -BSY pin is "low" level. Flash card can't be operated in this case.
- Before the card insertion VCC cannot be supplied to the card. After confirmation that -CD1, -CD2 pins are inserted, supply VCC to the card.
- -OE must be kept at the VCC level during power on reset in memory card mode and I/O card mode. OE must be kept constantly at the GND level in True IDE mode.
- Do not turn off the power or remove THNCFxxxMBA/BAI Series from the slot before read/write operation is complete. Avoid using THNCFxxxMBA/BAI Series when the battery is low. Power shortage, power failure and/or removal of THNCFxxxMBA/BAI Series from the slot before read/write operation is complete may cause malfunction of THNCFxxxMBA/BAI Series, data loss and/or damage to data.
- Routine performance of backing-up data (or taking back-up of data) is strongly recommended.

**RESTRICTIONS ON PRODUCT USE**

000707EBA

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