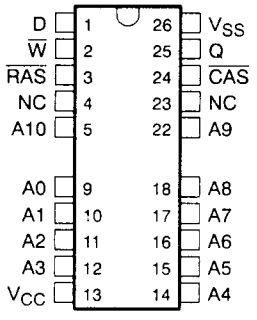
This Data Sheet is Applicable to All TMS44101s Symbolized with Revision "B" and Subsequent Revisions as Described on Page 5-124.

- **Organization . . . 4 194 304 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

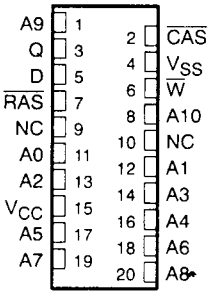
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44101-60	60 ns	15 ns	30 ns	110 ns
TMS44101-70	70 ns	18 ns	35 ns	130 ns
TMS44101-80	80 ns	20 ns	40 ns	150 ns
TMS44101-10	100 ns	25 ns	45 ns	180 ns

- **4-Bit Nibble Mode Operation**
  - **— Four Sequential Single-Bit Access Within a Row by Toggling $\overline{CAS}$**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**

DM and DJ Packages† (Top View)



SD Package† (Top View)



†The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0-A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

- **High-Reliability Plastic 300-mil and 350-mil 20/26-Lead Surface Mount (SOJ) Packages and a 20-Pin Zig-Zag In-line Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

description

The TMS44101 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 360 mW operating and 6 mW standby.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

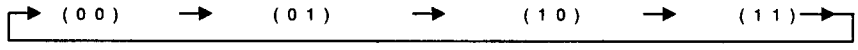
The TMS44101 is offered in a 350-mil 20/26-lead plastic surface mount SOJ package (DM suffix), a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), and a 20-pin plastic ZIP package (SD suffix). All packages are guaranteed for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

nibble mode

Nibble-mode operation allows high-speed read, write, or read-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at t_{CAC} as long as t_{RAC} and t_{AA} are satisfied. The next sequential bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Row A10 and column A10 provide the two binary bits for initial selection, with row A10 being the least-significant address and column A10 being the most significant. Therefore, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence



Data written in a sequence of more than 4 consecutive cycles shall be capable of being read back without exiting from the nibble mode. In a sequence of consecutive nibble-mode cycles the control of the high-impedance state for the data out (Q) pin is determined by each individual cycle. This facilitates fully mixed nibble-mode cycles (e.g., read/write/read-write, etc.)

address (A0 through A10)

Twenty address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

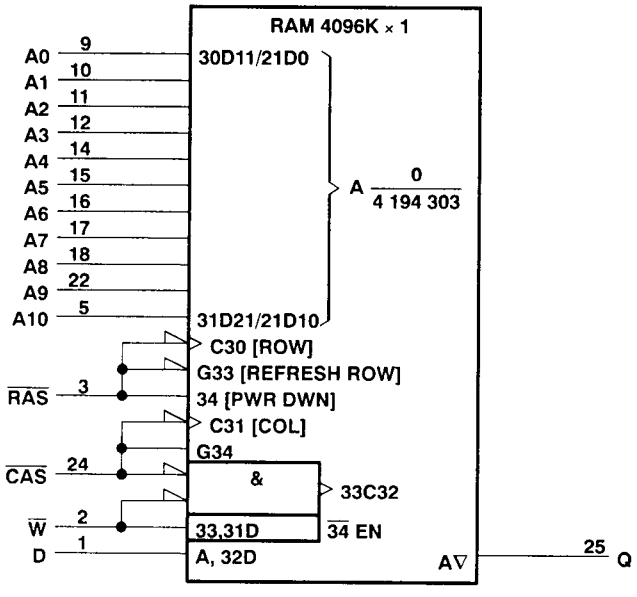
power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

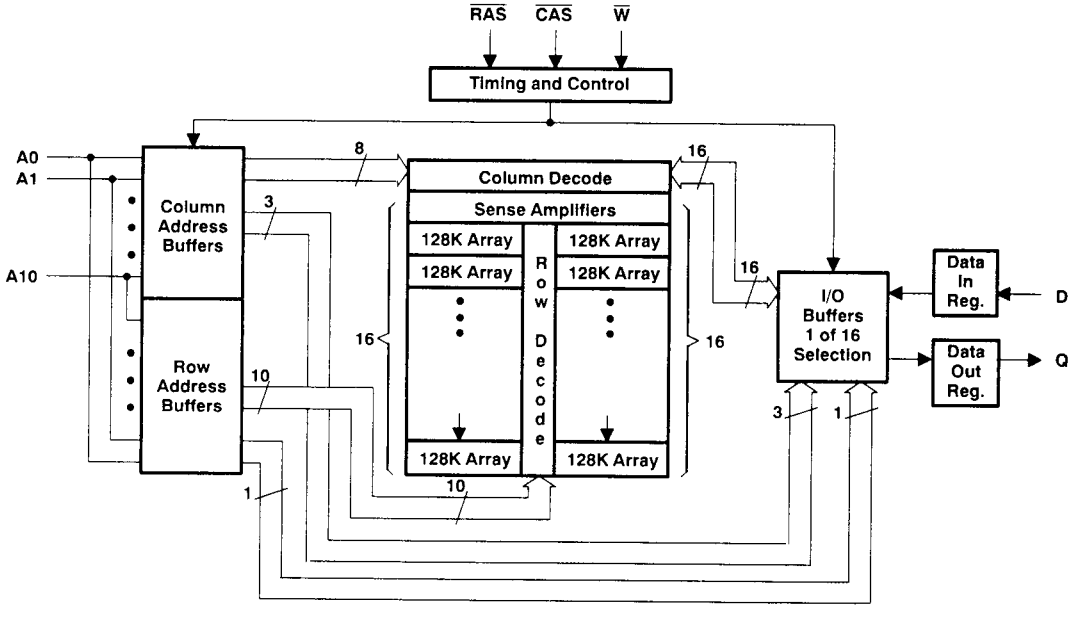
An industry standard Design For Test (DFT) mode is incorporated in the TMS44101. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter the test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	μA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	μA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		95		85		75		65	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V		1		1		1		1	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		95		85		75		65	mA
I_{CC5}	Average nibble mode current‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50		40	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTE 3: Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{NCAC}	Access time from $\overline{CAS}$ low (nibble operation)		15		18		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	0	25	ns

NOTE 5: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 6)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{NC}	Nibble-mode read or write cycle time	35		38		40		45		ns
t_{NRWC}	Nibble-mode read-write cycle time	55		61		65		75		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low (see Note 7)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 8)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 9)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns

Continued next page.

NOTES: 6. All cycle times assume t_T = 5 ns.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS44101-60		TMS44101-70		TMS44101-80		TMS44101-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{DHR}	Data hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{DH}	Data hold time (see Note 9)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$-low (Read-write operation only)	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$-low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$-low (Read-write operation only)	60		70		80		100		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval		16		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

NOTES: 9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to guarantee access time.

PARAMETER MEASUREMENT INFORMATION

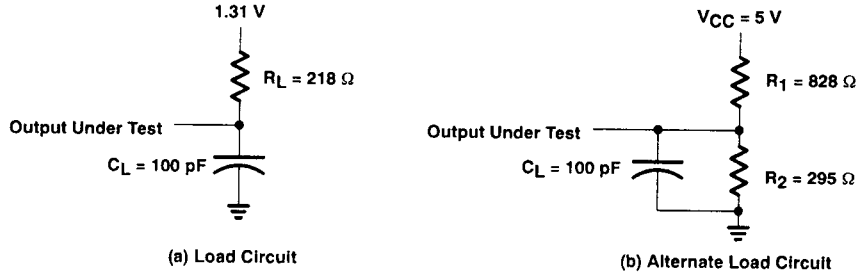
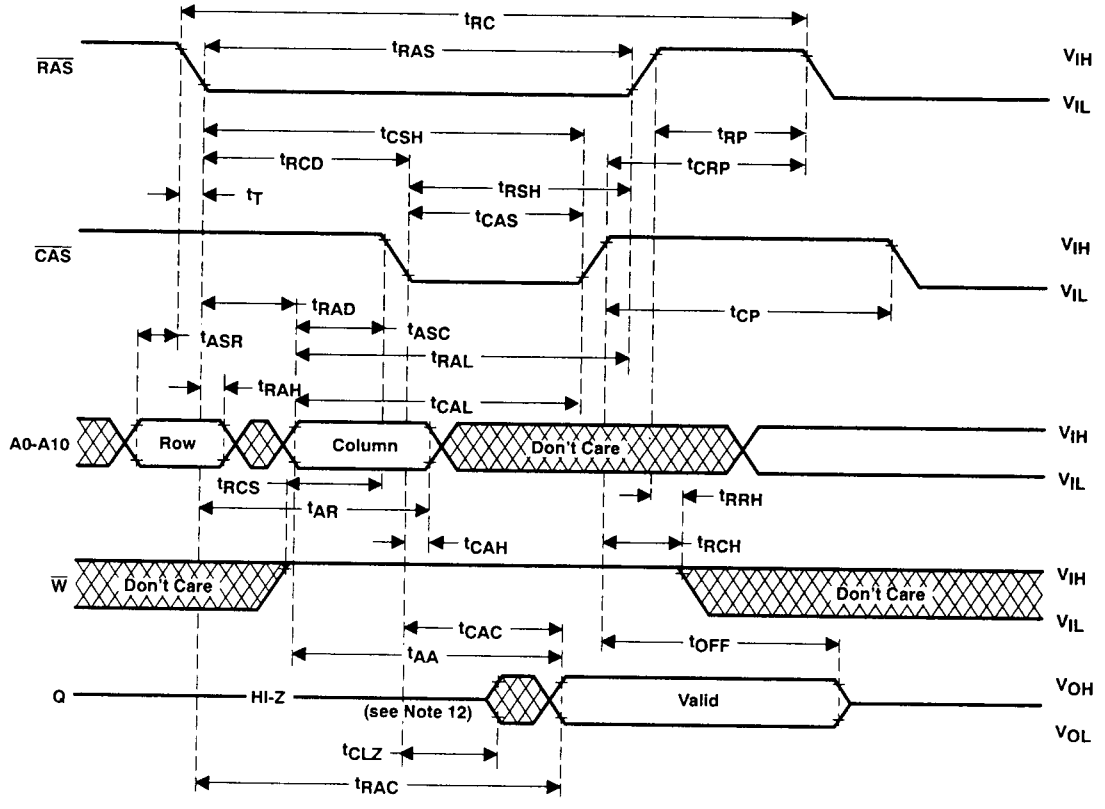


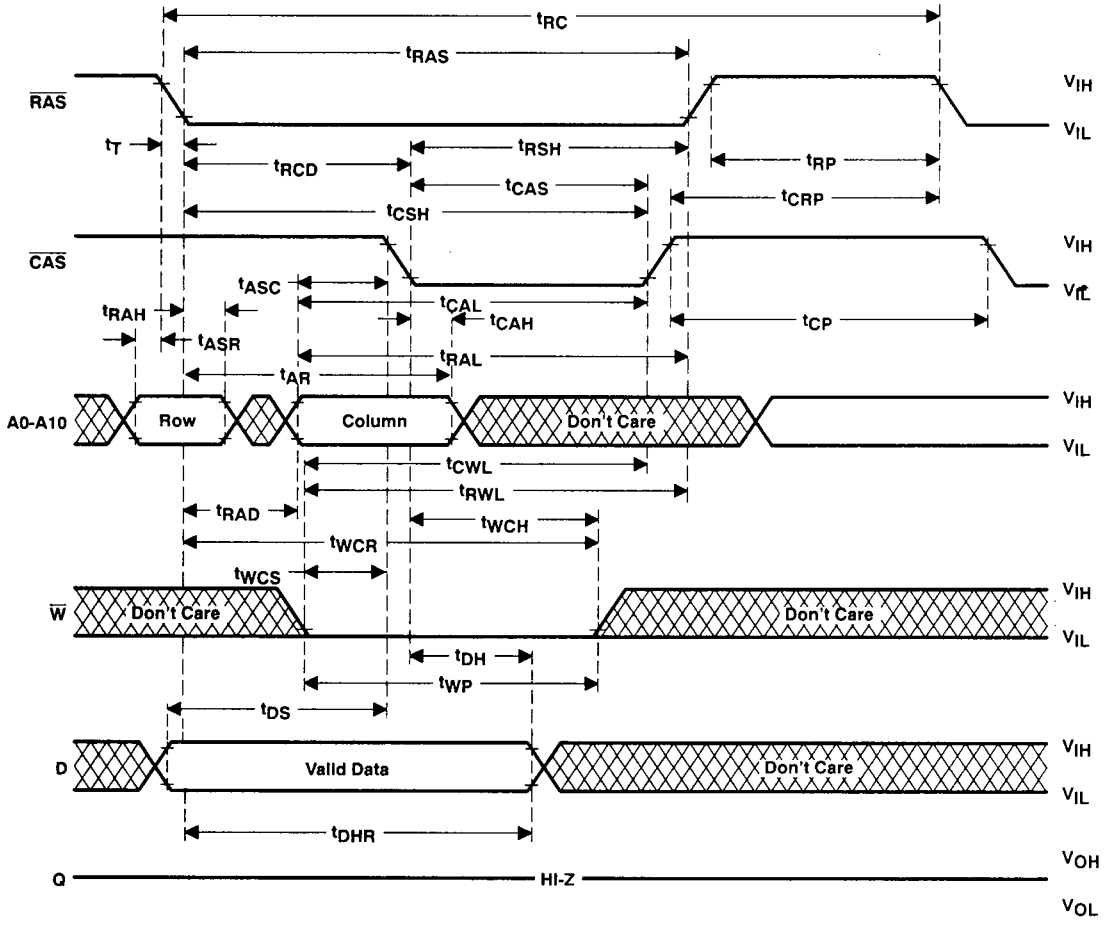
Figure 1. Load Circuits for Timing Parameters

read cycle timing

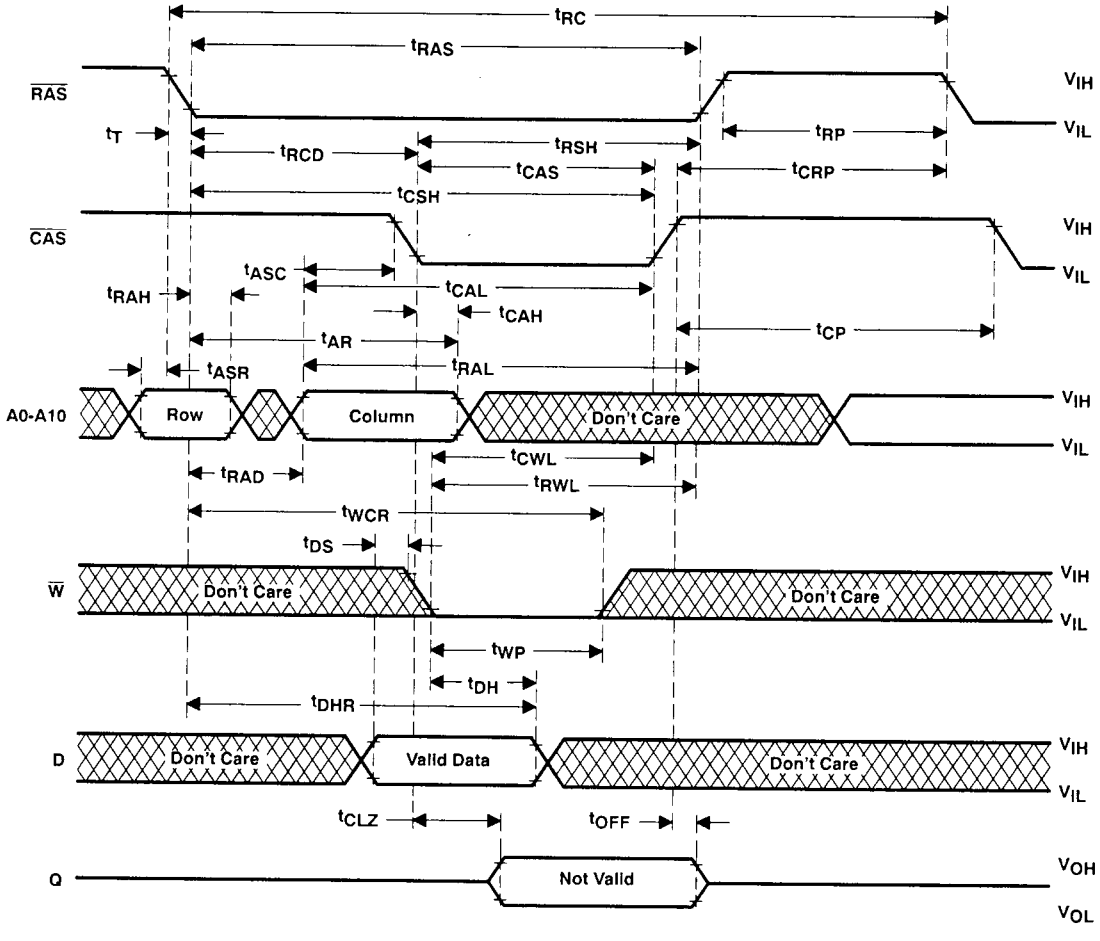


NOTE 12: Output may go from three-state to an invalid data state prior to the specified access time.

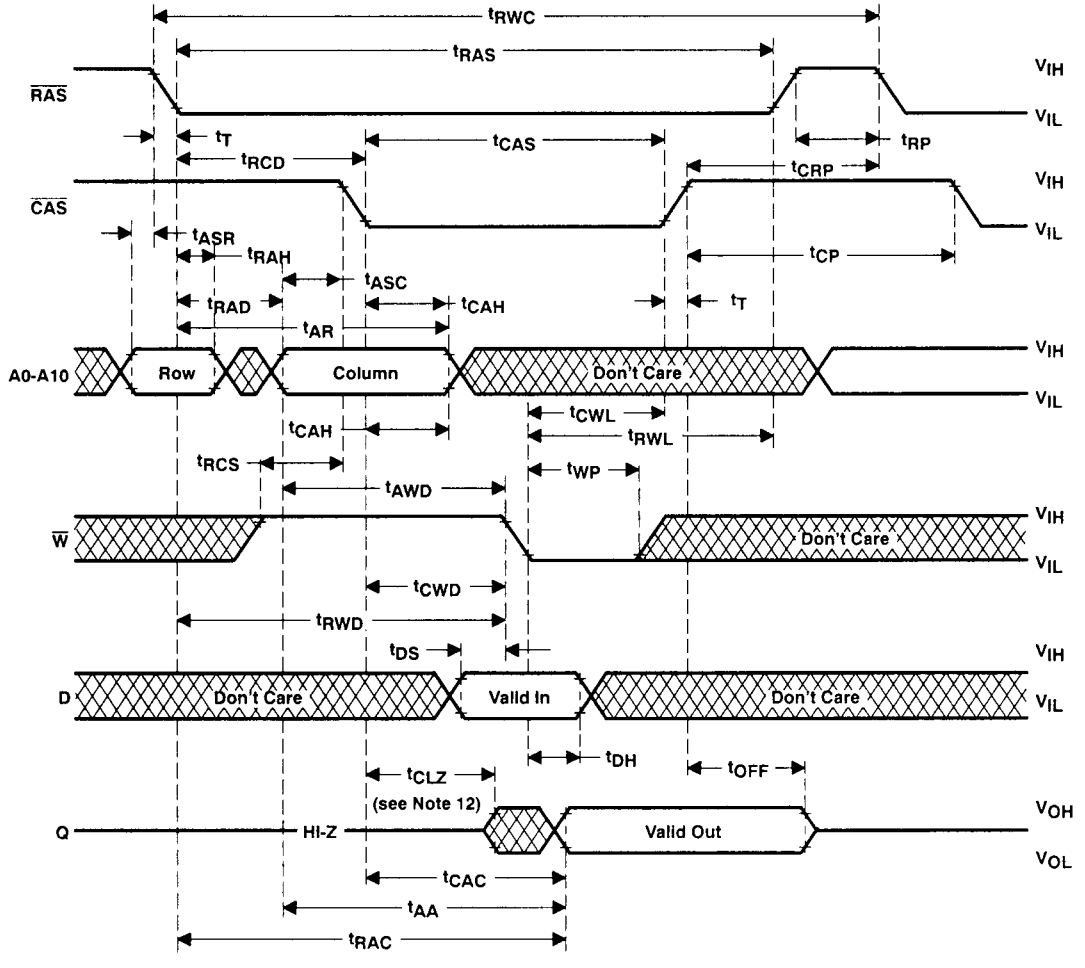
early write cycle timing



write cycle timing

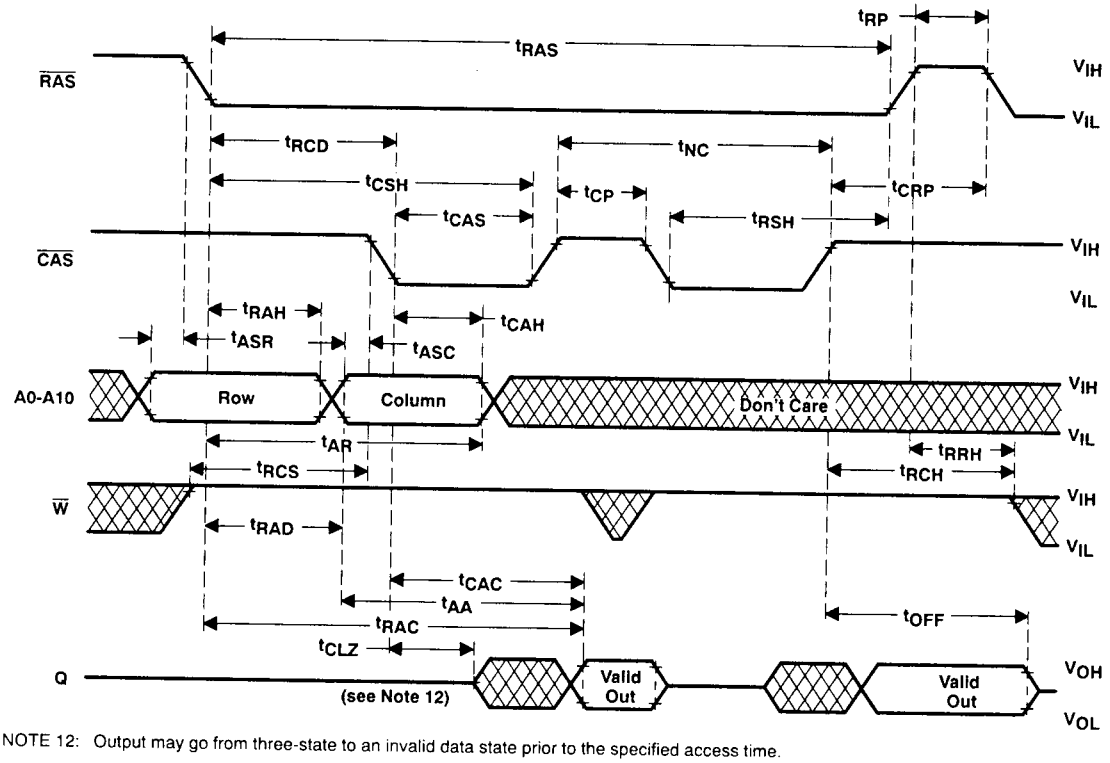


read-write cycle timing



NOTE 12: Output may go from three-state to an invalid data state prior to the specified access time.

nibble-mode read cycle timing



NOTE 12: Output may go from three-state to an invalid data state prior to the specified access time.

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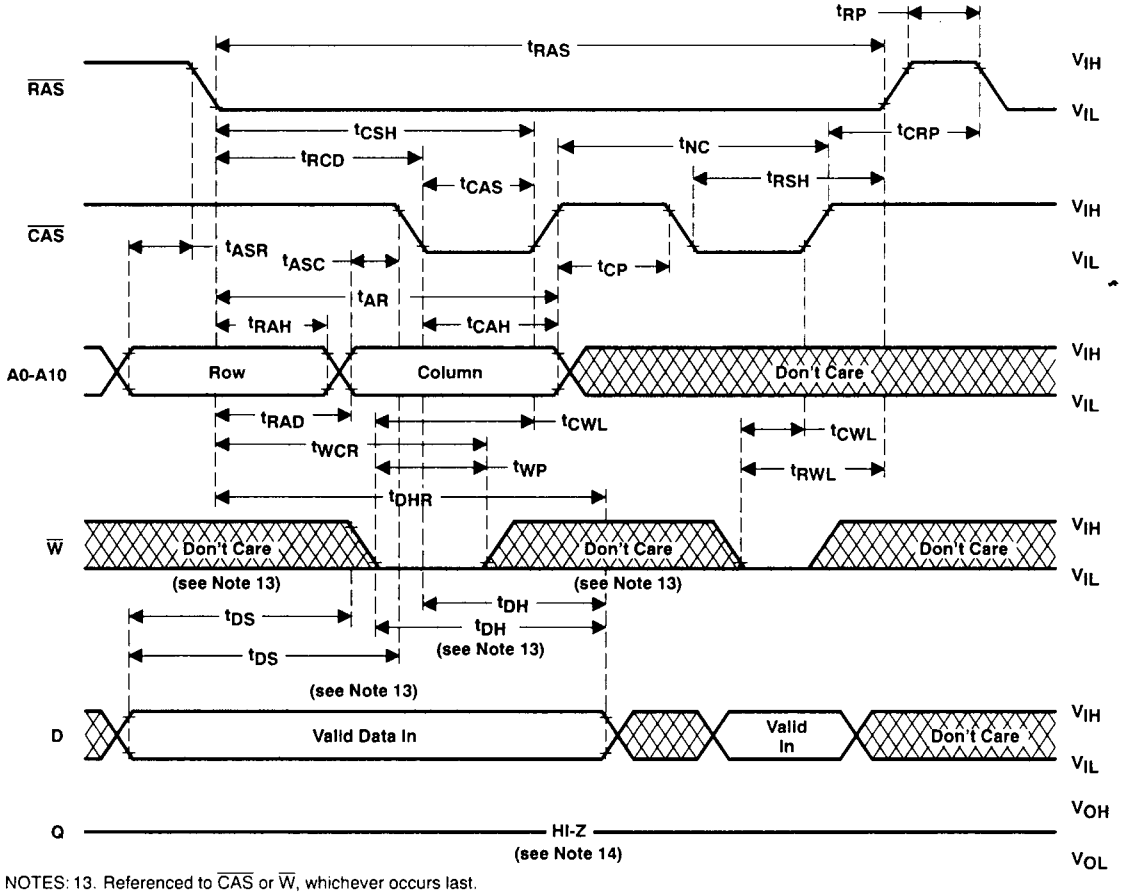
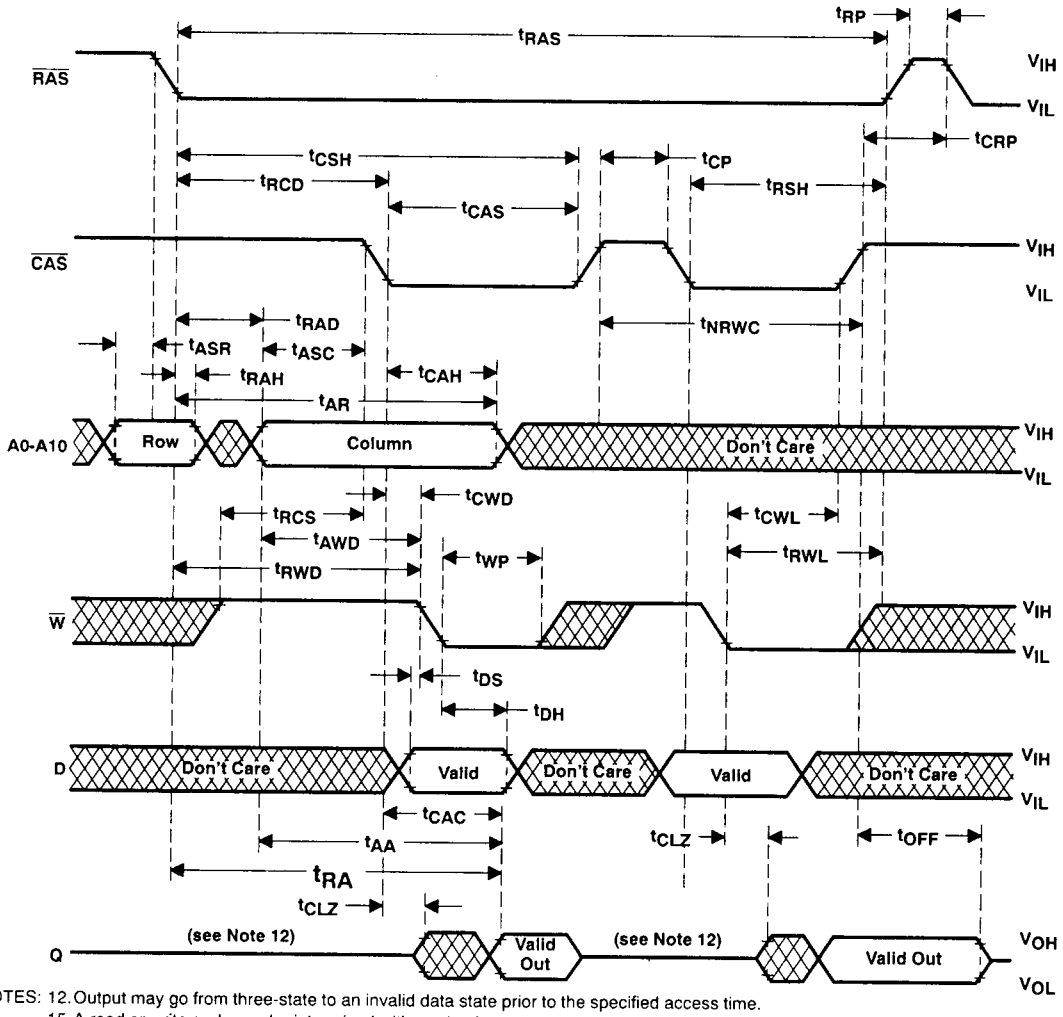
nibble-mode write cycle timing



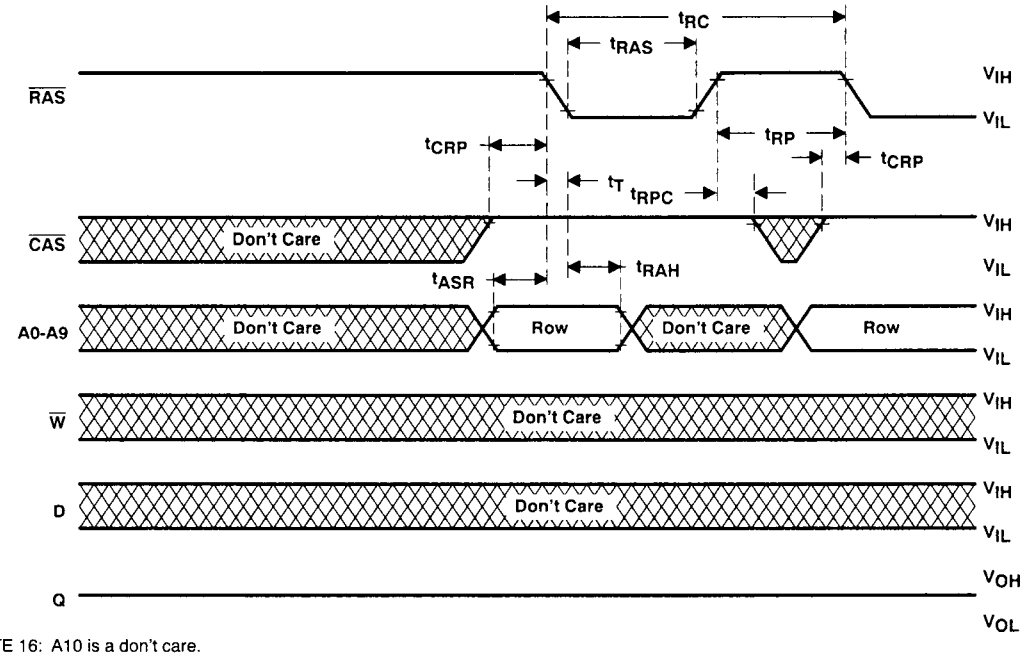
NOTES: 13. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
14. The output may go to an invalid state if a late write is completed.

nibble-mode read-write cycle timing



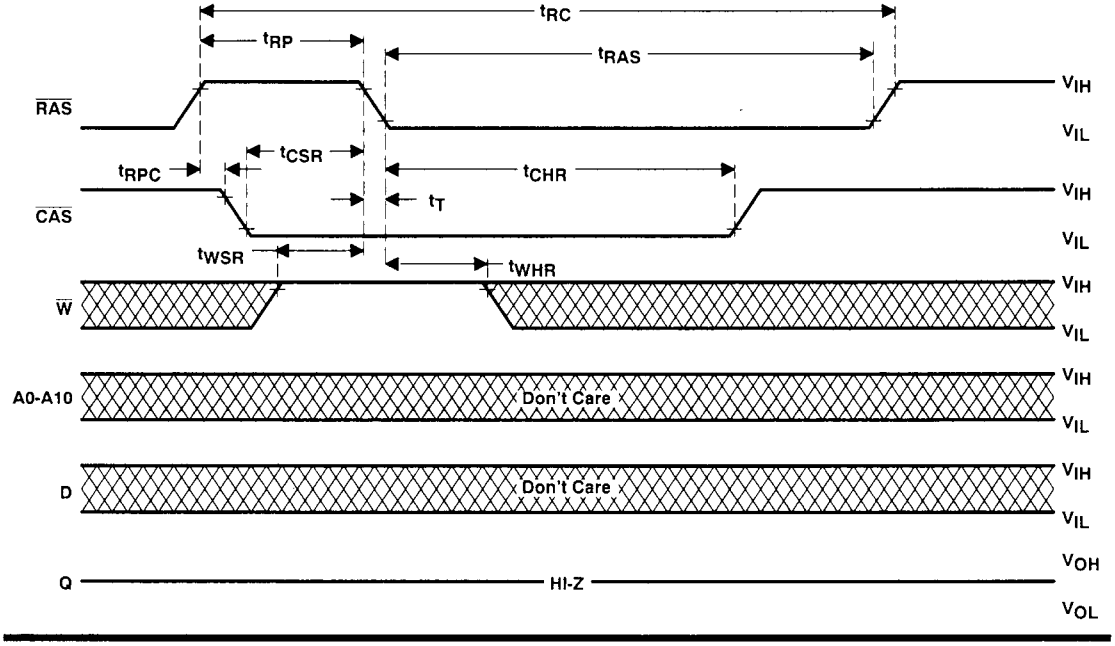
NOTES: 12. Output may go from three-state to an invalid data state prior to the specified access time.
15. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

RAS-only refresh timing

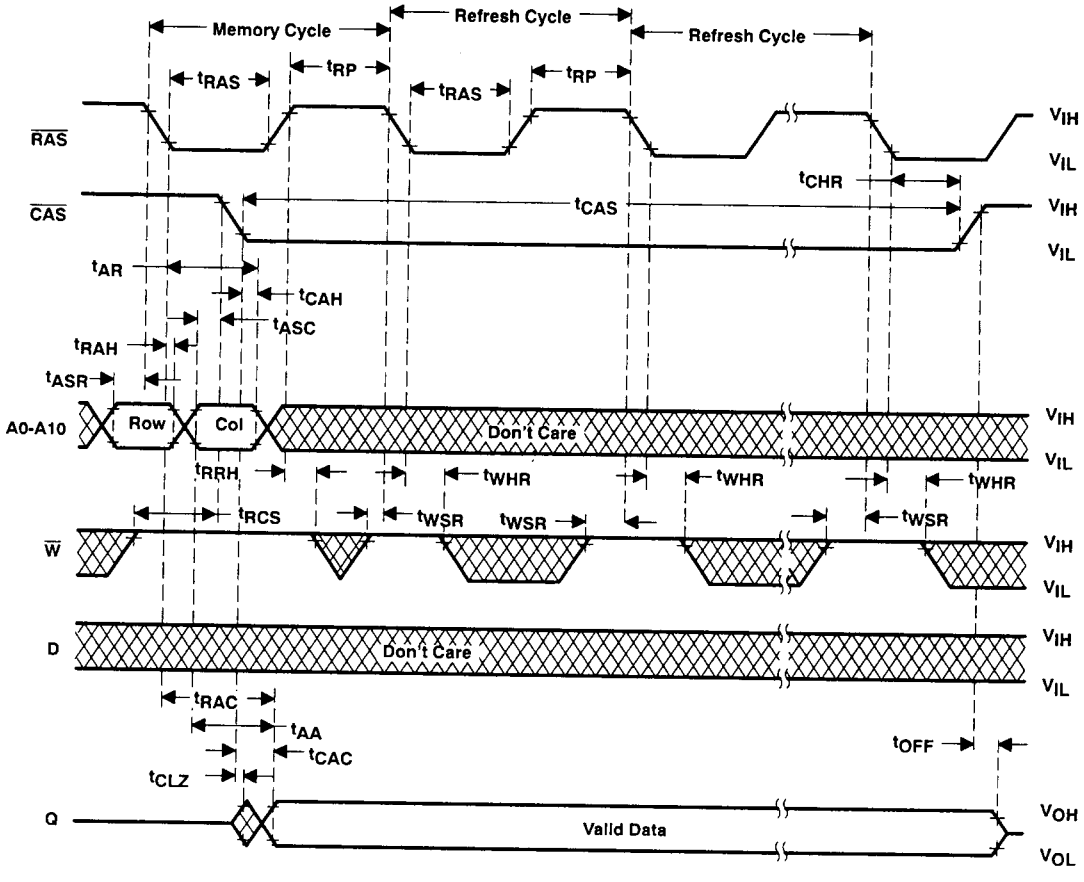


NOTE 16: A10 is a don't care.

automatic (CAS-before-RAS) refresh cycle timing



hidden refresh cycle (read)



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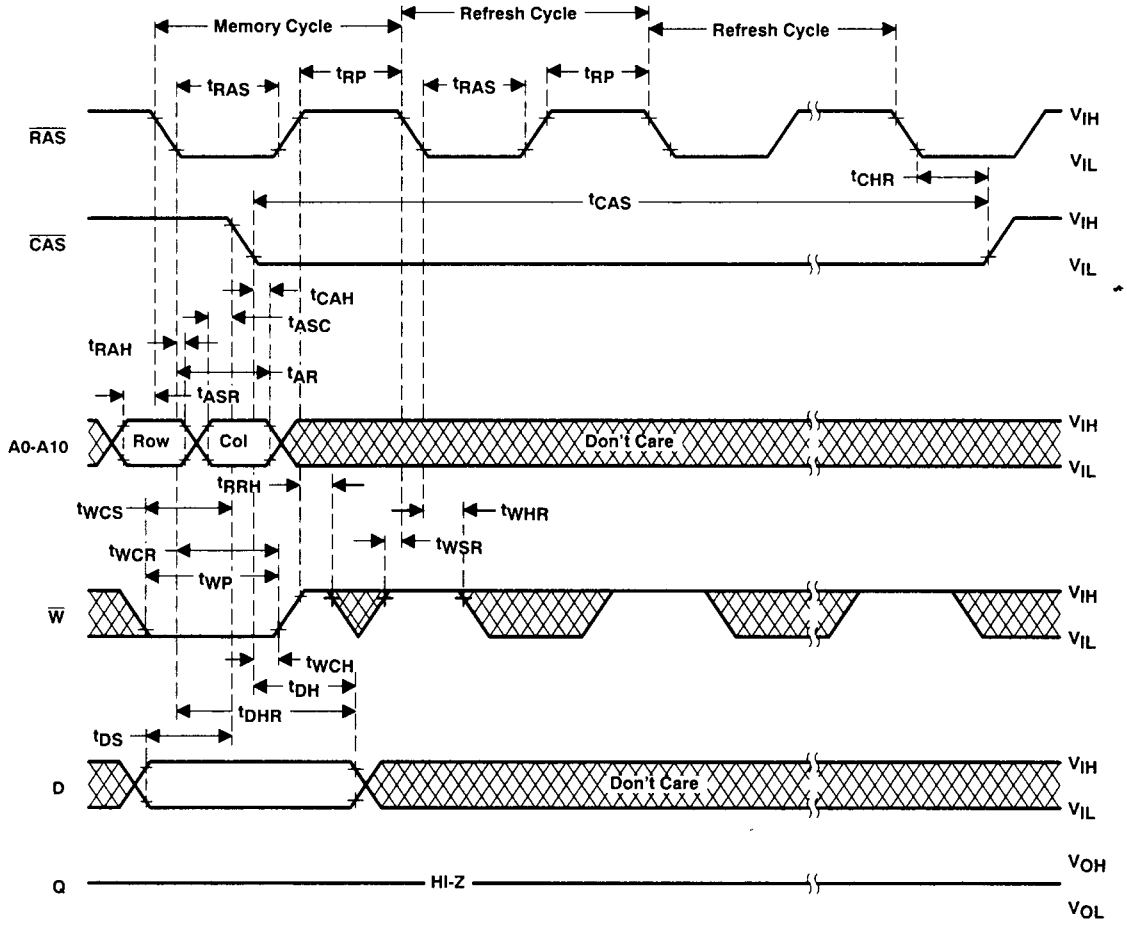
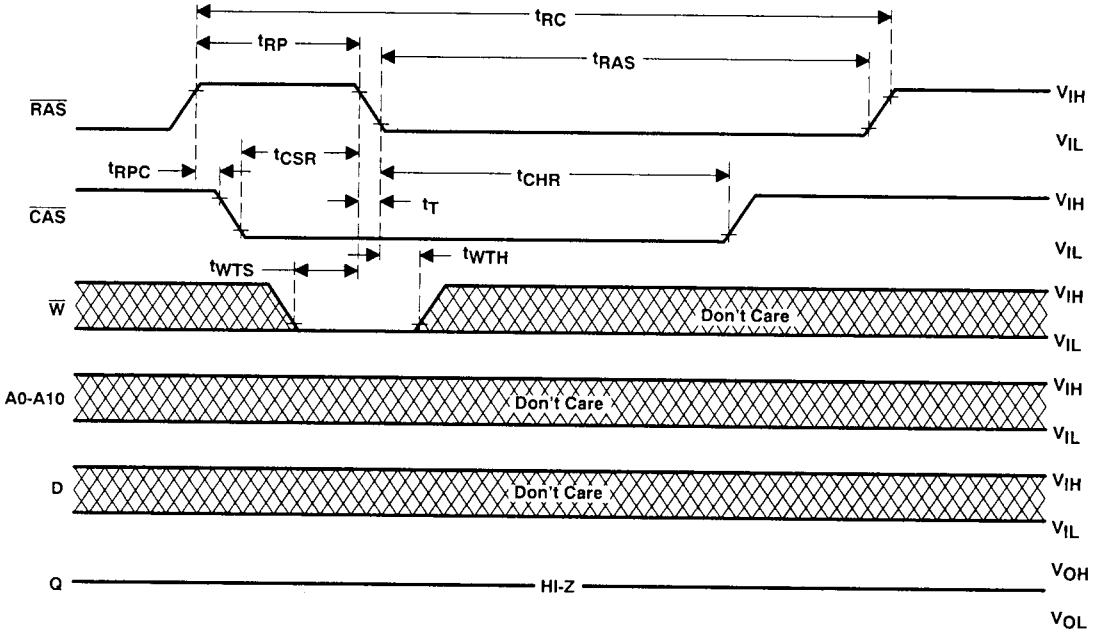
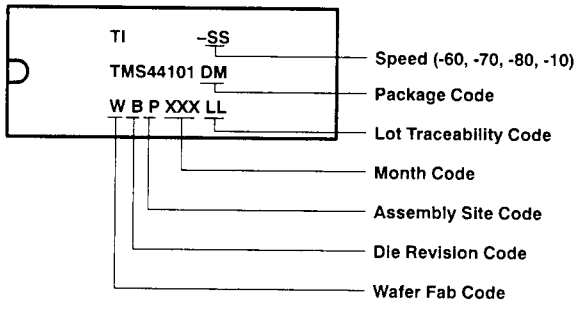
hidden refresh cycle (write)



test mode entry cycle



device symbolization



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