

CFA0010A

## 4-Bit Microprocessor Slice

DESCRIPTION: CFA0010A is designed to be functionally identical to the AM2901, although the I/Os are different (see page 6 of 7 for a description of the enhancements to the AM2901). The 2901 is a 4-bit slice consisting of a register file (16x4 dual port RAM), the ALU, the Q register, and the necessary control logic. The 2901 is expandable in 4-bit increments. For a detailed functional description and truth table, see the AMD 2900 data book.

## RAM

The RAM is addressed by two 4-bit address fields that cause the data to appear at the A or B (internal) ports. Four address bits (A0~A3, B0~B3) are used for a 16 deep RAM. If the A and B addresses are the same, the data at the A and B ports are identical. New data are written into the RAM location specified by the B address when the RAM write enable (RAM EN) is active and the clock input is low.

Each of the four RAM data inputs is driven by a 3-input multiplexer that allows the outputs of the ALU to be shifted one bit to the left or to the right, or not shifted at all. The other inputs to the multiplexer are from the RAMI3 and RAMI0 inputs. For a shift left (up) operation, the RAMO3 output and the RAMI0 multiplexer input are used. For a shift right (down) operation, the RAMO0 output and the RAMI3 multiplexer input are used. The outputs of the RAM A and B ports drive separate 4-bit latches that are transparent when the clock is high (follow the RAM data). The outputs of the A latches go to three multiplexers whose outputs drive the two inputs to the ALU (R and S) and the cell outputs (Y).

## ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on two 4-Bit input words, R and S. The R inputs are driven from a 4-bit 2-to-1 multiplexer whose inputs are from either the RAM A-port or the external data (D) inputs. The S inputs are driven from a 4-bit 3-to-1 multiplexer whose inputs are from A-Port, B-Port, or the Q register. Both multiplexers are controlled by the I0, I1, and I2 inputs. This configuration of multiplexers on the ALU R and S inputs enables you to select eight pairs of combinations of A, B, D, Q, and "0" inputs as 4-bit operands to the ALU. The ALU has a carry-in (CN) input, and carry-propagate (PN), carry-generate (GN), carry-out (CN4), and overflow (OVR) outputs to enable you to speed up arithmetic operations implementing carry look-ahead logic and determining if an arithmetic overflow has occurred. The ALU Data outputs (F) are routed to the RAM, the Q register inputs, and the Y outputs, which are controlled by the I6, I7, and I8 control signal inputs. In addition, the MSB of the ALU is output as F3 so that you can examine the sign bit. The FEQ0 output, which is high when F0=F1=F2=F3=0, allows you to determine when the ALU output is zero.

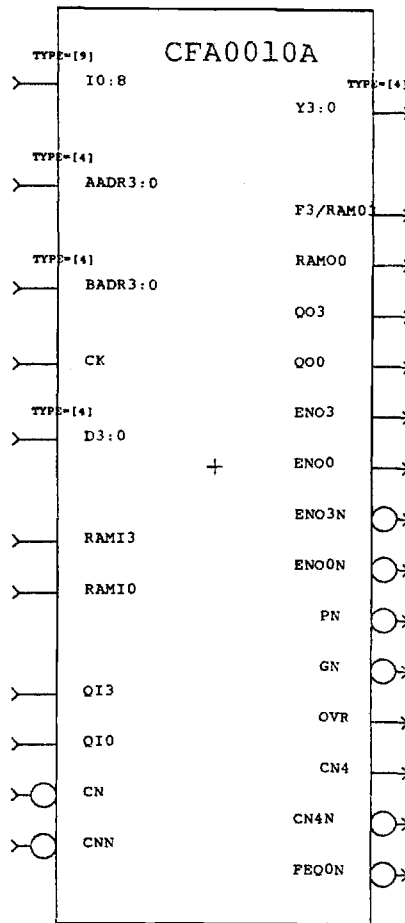
### Q Register

The Q register functions as an accumulator or temporary storage register. Physically, it is a 4-bit register implemented with master-slave latches. The inputs to the Q register are driven by the outputs from a 4-bit 3-to-1 multiplexer under control of the I6, I7, and I8 inputs. The Q0 and Q3 input and output pins function in a manner similar to that of the RAM0 and RAM3 pins. The other inputs to the multiplexer enable the contents of the Q register to be shifted up or down, or the outputs of the ALU to be entered into the master latches. Data is entered into the master latches when the clock is low and transferred from master to slave (output) when the clock changes from low to high.

### ALU Source Operand and ALU Functions

The I0, I1, and I2 lines select eight pairs of source operands; and the I3, I4, and I5 lines select the operation to be performed. The carry-in (CN) signal affects the arithmetic result and the internal flags, not the logical operations.

LOGIC SYMBOL:



INPUTS (LOADING IN TRANSISTOR PAIRS)

IO(3.5), I1(3.5), I2(4.5), I3(4.0), I4(4.0), I5(2.5), I6(2.5),  
 I7(5.5), I8(5.5), AADR3(3.5), AADR2(3.5), AADR1(3.5),  
 AADR0(5.0), BADR3(3.5), BADR2(3.5), BADR1(7.0), BADR0(8.5),  
 CK(13), D3(1.0), D2(1.0), D1(1.0), D0(1.0), RAMI3(1.0),  
 RAMI0(1.0), QI3(1.0), QI0(1.0), CN(2.0), CNN(2.5)

OUTPUTS (DRIVE IN (#P, #N))

Y3(2,1), Y2(2,1), Y1(2,1), Y0(2,1), RAMO3(2,2), RAMO0(2,2),  
 QO3(1,1), QO0(1,1), ENO3(2,1), ENO0(2,1), ENO3N(1,0.5),  
 ENO0N(1,0.5), PN(1,0.25), GN(2,1), OVR(2,2), CN4(1,0.5),  
 CN4N(2,1), FEQON(1,0.5)

GATE COUNT:

GATES USED = 900  
 AREA USED = 1190

CFA0010A

AC CHARACTERISTICS:

| TO<br>FROM            | Y    | F3<br>RAMO3<br>RAMO0 | CN4  | CN4N | GN   | PN   | FEQON | OVR  | QO0<br>QO3 |
|-----------------------|------|----------------------|------|------|------|------|-------|------|------------|
| A, B ADDRESS          | 23.1 | 20.3                 | 18.9 | 19.6 | 18.2 | 16.1 | 21.7  | 21   | —          |
| D                     | 16.1 | 12.6                 | 11.9 | 13.3 | 11.2 | 9.1  | 14.7  | 14.7 | —          |
| CN                    | 9.1  | 5.6                  | 2.1  | 2.8  | —    | —    | 8.4   | 5.6  | —          |
| CNN                   | 10.5 | —                    | —    | —    | —    | —    | 9.8   | —    | —          |
| I0, I1, I2            | 18.9 | 15.4                 | 13.3 | 14.7 | 12.6 | 11.2 | 17.5  | 16.1 | —          |
| I3, I4, I5            | 16.1 | 12.6                 | 11.2 | 11.9 | 10.5 | 8.4  | 15.4  | 14   | —          |
| I6, I7, I8            | 9.1  | —                    | —    | —    | —    | —    | —     | —    | —          |
| A BYPASS ALU<br>I=2XX | 11.9 | —                    | —    | —    | —    | —    | —     | —    | —          |
| CLOCK                 | 21.7 | 17.5                 | 16.1 | 16.8 | 15.4 | 14   | 20.3  | 18.9 | 7          |

SET UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT:

| INPUT              | CP<br>SET-UP TIME<br>BEFORE H → L | HOLD TIME<br>AFTER H → L | SET-UP TIME<br>BEFORE L → H | HOLD TIME<br>AFTER L → H |
|--------------------|-----------------------------------|--------------------------|-----------------------------|--------------------------|
| A, B SOURCE ADDR   | 6.3                               | 0                        | 22.4                        | 0                        |
| B DESTINATION ADDR | 1.4                               | DO NOT CHANGE            |                             | 0                        |
| D                  |                                   |                          | 15.4                        | 0                        |
| CN                 |                                   |                          | 9.1                         |                          |
| CNN                |                                   |                          | 10.5                        | 0                        |
| I0, I1, I2         |                                   |                          | 18.2                        | 0                        |
| I3, I4, I5         |                                   |                          | 16.1                        | 0                        |
| I6, I7, I8         | 5.6                               | DO NOT CHANGE            |                             | 0                        |
| RAMI0,3, QI0,3     |                                   |                          | 3.5                         | 0                        |

ALL TIMES ARE IN NSEC AND ARE TYPICAL (10K TECHNOLOGY)  
 MINIMUM CLOCK PERIOD (TYP.) = 25.9 NS  
 MAXIMUM FREQUENCY WCCOM = 10.5 MHZ  
                                   WCMIL = 8.4 MHZ  
 MINIMUM CLOCK LOW TIME = 12.6 NS  
 MINIMUM CLOCK HIGH TIME = 12.6 NS

CFA0010A

PIN DESCRIPTION:

IO - I8 THE NINE INSTRUCTION CONTROL SIGNALS USED TO DETERMINE WHERE THE OPERANDS OF THE ALU ARE COMING FROM (I0-I2), WHAT FUNCTION THE ALU IS GOING TO PERFORM (I3-I5), AND WHAT KIND OF DATA THE RAM AND Q REG ARE STORING (I6-I8).

AADR0 - AADR3 THE FOUR ADDRESS LINES WHICH SELECT A REGISTER FROM THE REGISTER STACK AND DISPLAY IT THROUGH THE A PORT.

BADR0 - BADR3 THE FOUR ADDRESS LINES USED TO CONTROL WHICH REGISTER IS TO BE READ FROM OR WRITTEN INTO THROUGH THE B PORT. WRITING TAKES PLACE WHEN THE CLOCK GOES LOW.

CK THE CLOCK INPUT. WHEN IT GOES FROM LOW TO HIGH, Q REG AND THE OUTPUTS OF THE REGISTER STACK CHANGE.

D0 - D3 DATA INPUTS. CAN BE SELECTED AS A DIRECT OPERAND INPUT TO THE ALU.

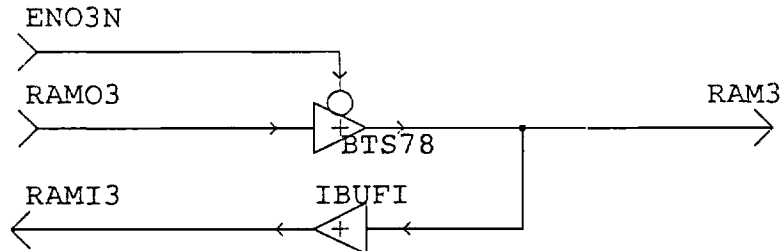
RMAI3, QI3 THE MSB INPUTS TO THE REGISTER STACK AND THE Q REGISTER. THEY ARE USED DURING A LEFT SHIFT OPERATION.

RAMI0, QI0 THE LSB INPUTS TO THE REGISTER STACK AND THE Q REGISTER. THEY ARE USED DURING A RIGHT SHIFT OPERATION.

CN, CNN COMPLEMENTARY CARRY-IN INPUTS TO THE ALU.

Y0 - Y3 THE FOUR DATA OUTPUTS WHICH DISPLAY EITHER THE ALU RESULT OR THE OUTPUTS FROM THE A PORT OF THE REGISTER STAC.

RAMO3, QO3 THE OUTPUTS OF THE MSBS OF THE ALU AND THE Q REG RESPECTIVELY. WHEN USED TOGETHER WITH ENO3N OR ENO3 SIGNAL, THEY CAN GENERATE THE EQUIVALENT BIDIRECT PINS AS THE RAM3 AND Q3 IN AM2901.



CFA0010A

RAM00, Q00            THE OUTPUTS OF THE LSBS OF THE ALU AND Q REG  
                          RESPECTIVELY. AS IN THE CASE OF RAM03 AND Q03, THESE  
                          TWO SIGNALS CAN BE MADE TO BE EQUIVALENT TO RAM0  
                          AND Q0 IN AM2901 WHEN USED WITH EN00N OR EN00 AND  
                          A BI-DIRECT DRIVER.

PN, GN                THE CARRY PROPAGATE AND CARRY GENERATE OUTPUTS OF  
                          THE ALU. SHOULD BE USED FOR MORE THAN 16 BIT FOR  
                          CARRY LOOK-AHEAD INPUTS.

OVR                    AN OVERFLOW INDICATION OF A TWO'S COMPLEMENT  
                          ARITHMETIC OPERATION INTO THE SIGN BIT. IT IS  
                          ACTIVE HIGH.

CN4, CN4N            THE COMPLEMENTARY CARRY-OUT OF THE ALU. THEY ARE  
                          NORMALLY USED TO FEED INTO THE CN AND CNN INPUTS OF  
                          THE NEXT HIGHER 4 BIT CFA0010A DURING CASCADING.

FEQ0N                THE ACTIVE LOW SIGNAL WHICH INDICATES ALL OUTPUTS  
                          (F0-F3) OF THE ALU ARE LOW.

DIFFERENCES AND ENHANCEMENT FROM/TO AM2901:

Although the CFA0010A is designed to be functionally identical to the AM2901, its I/Os are not exactly the same. Each of the bidirectional pins of the AM2901 becomes three pins in the CFA0010A. One pin is for the input, and the second and third pins are for the output and output enable. The advantage of this I/O scheme is that you can gain performance if bidirectional signals are not required (mostly true when the CFA0010A is used inside a large chip). However, if a direct macro is needed, the figure on the next page shows an easy way to create it.

