NEC

MOS INTEGRATED CIRCUIT

MC-454BA80

4 M-WORD BY 80-BIT SYNCHRONOUS DYNAMIC RAM MODULE BUFFERED TYPE

Description

The MC-454BA80 is a 4,194,304 words by 80 bits synchronous dynamic RAM module on which 20 pieces of 16 M SDRAM : μPD4516421 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 80 bits organization
- Clock frequency and Burst cycle time

	Family	Clock frequency (MAX.)	Burst cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
★	MC-454BA80-A10	100 MHz	10 ns	9.72 W	144 mW
★	MC-454BA80-A12	83 MHz	12 ns	8.28 W	(CMOS level input)

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- ★ Single +3.3 +0.3/–0.15 V power supply
- LVTTL compatible
- 2,048 refresh cycles/32 ms
- Burst termination by Burst Stop command and Precharge command
- 200-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Buffered type

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The mark ★ shows major revised points.

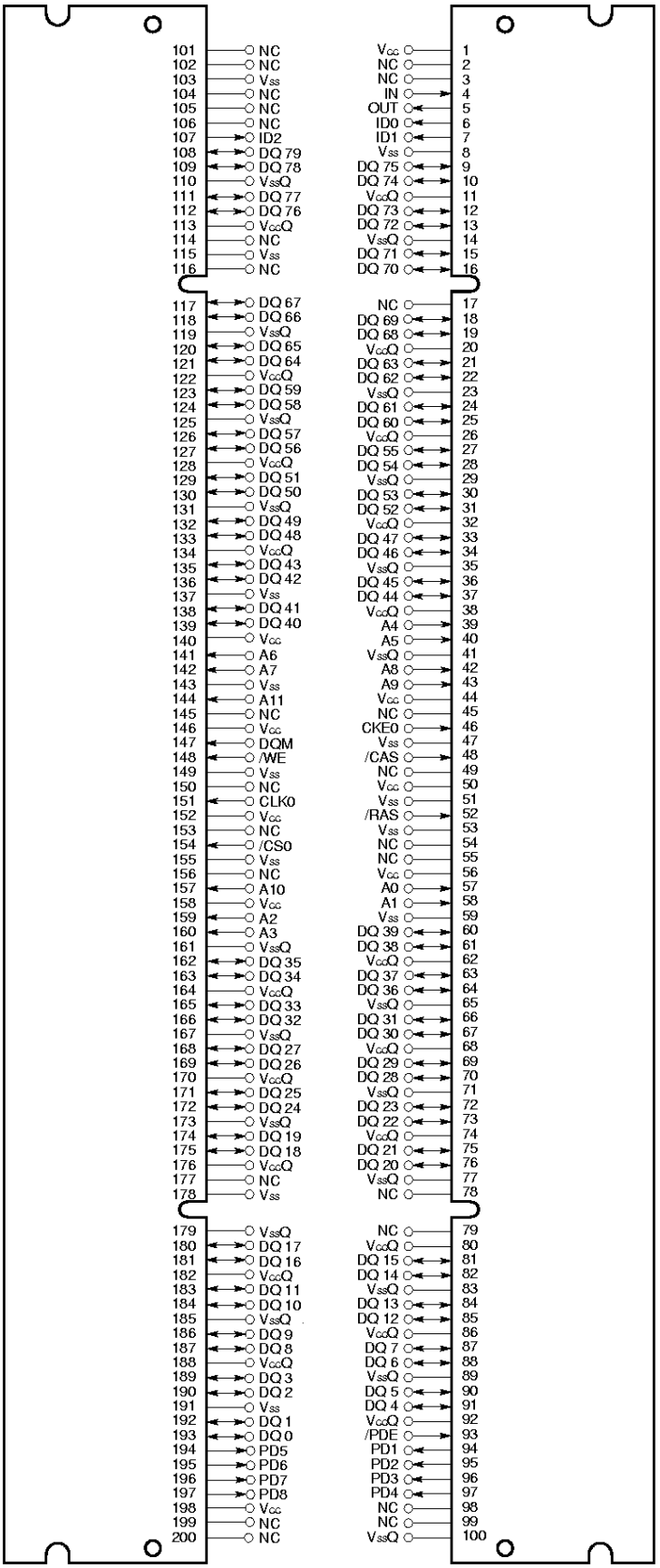
Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-454BA80F-A10	100 MHz	200-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated	20 pieces of 16M SDRAM : μPD4516421G5 (400 mil TSOP (II)) [Double side]
MC-454BA80F-A12	83 MHz		

Pin Configuration

200-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

[MC-454BA80F]



PD and ID Table

Pin name	Pin No.	Speed	
		10 ns	12 ns
PD1	94	L	L
PD2	95	H	H
PD3	96	L	L
PD4	97	H	H
PD5	194	H	L
PD6	195	L	H
PD7	196	H	H
PD8	197	H	H
ID0	6	H	H
ID1	7	L	L
ID2	107	L	L

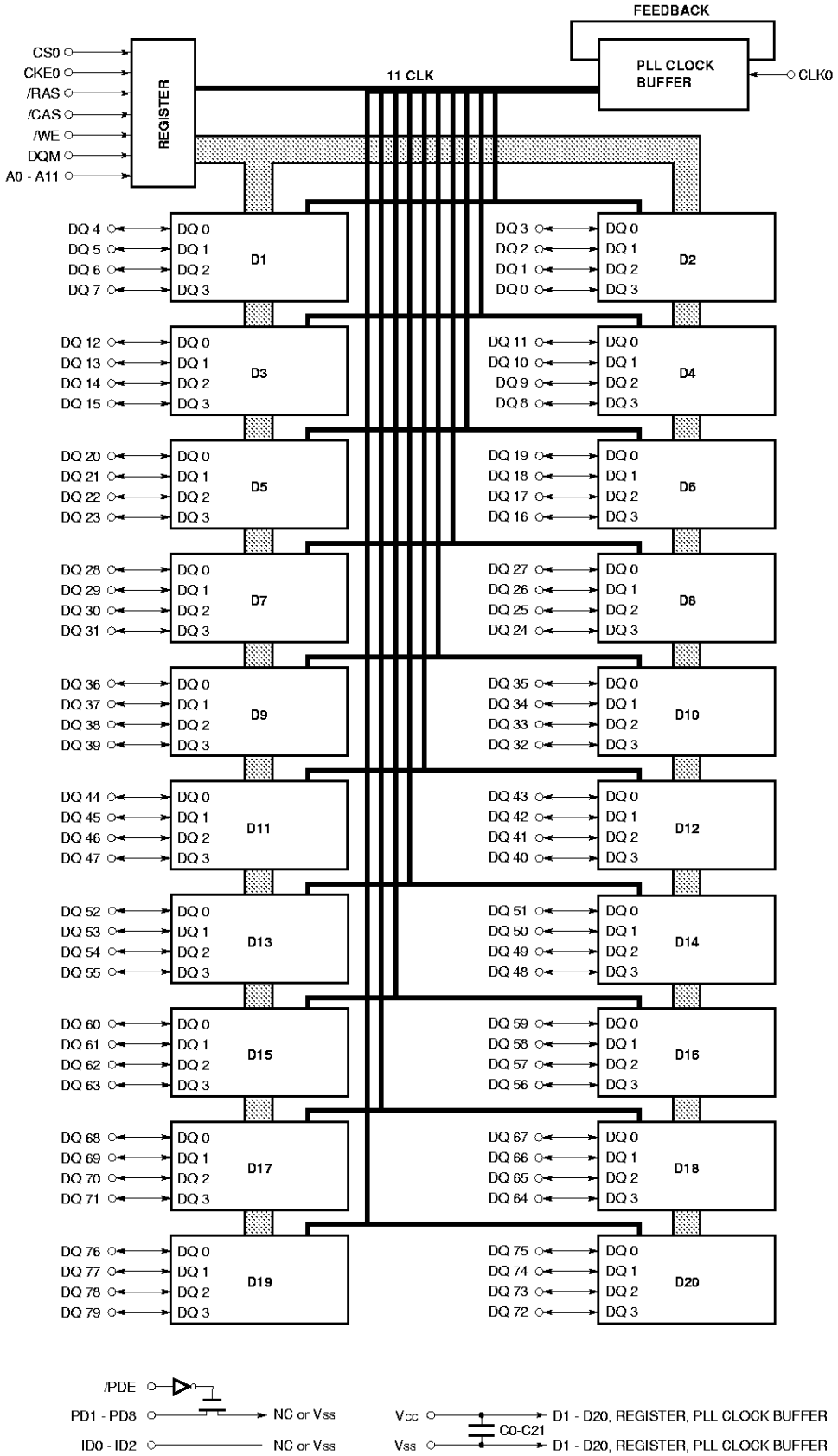
Remark

PD : PD and ID must each be pulled up through a resistor to V_{CC} at the next higher level assembly. PDs will either be open (NC) or driven to V_{SS} via on-board buffer circuits.

ID : IDs will either be open(NC) or connected directly to V_{SS} without a buffer.

A0 - A11 : Address Inputs
[Row : A0 - A10, Column : A0 - A9]
DQ0 - DQ79 : Data Inputs/Outputs
CLK0 : Clock Input
CKE0 : Clock Enable Input
/CS0 : Chip Select Input
/RAS : Row Address Strobe
/CAS : Column Address Strobe
/WE : Write Enable
DQM : DQ Mask Enable
/PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0 - ID2 : Identify Pins
IN, OUT : Unbuffered Physical Detect Input/Output (separate)
Vcc : Power Supply
VccQ : Power Supply for Data Input/Output
Vss : Ground
VssQ : Ground for Data Input/Output
NC : No Connection

Block Diagram



Remarks 1. A 10Ω ± 5 % resistor shall be wired in series with DQ0 - DQ79 near the card edge connector. All clock line outputs from the PLL CLOCK BUFFER shall be equal length.

2. D1 - D20 : μPD4516421 (2M words × 4 bits × 2 banks)

Electrical Specifications (Preliminary)

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–1.0 to +4.6	V
Voltage on input pin relative to GND	V_T		–1.0 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		22	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Supply voltage	V_{CC}		3.15	3.3	3.6	V
High level input voltage	V_{IH}		2.0		4.6	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, CKE0, /CS0, /RAS, /CAS, /WE, DQM			15	pF
	C_{I2}	CLK0			8	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ79			15	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC(MIN.)}$, I_O = 0 mA	/CAS latency = 2			1,800	mA	1
			/CAS latency = 3			1,900		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				60	mA	2
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX.)}$, $t_{CK} = \infty$				40		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				500	mA	2
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} = \infty$ Input signals are stable.				120		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				60	mA	2
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, $t_{CK} = \infty$				40		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				560	mA	2
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} = \infty$ Input signals are stable.				200		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$ I_O = 0 mA	/CAS latency = 2	-A10		2,100	mA	3
				-A12		1,700		
			/CAS latency = 3	-A10		2,700		
				-A12		2,300		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$				2,100	mA	4
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				40	mA	2
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V			−10	+10	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V			−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

2. V_{CC} − 0.2 V ≤ $V_{IH(CLK)}$ ≤ $V_{IH(MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V

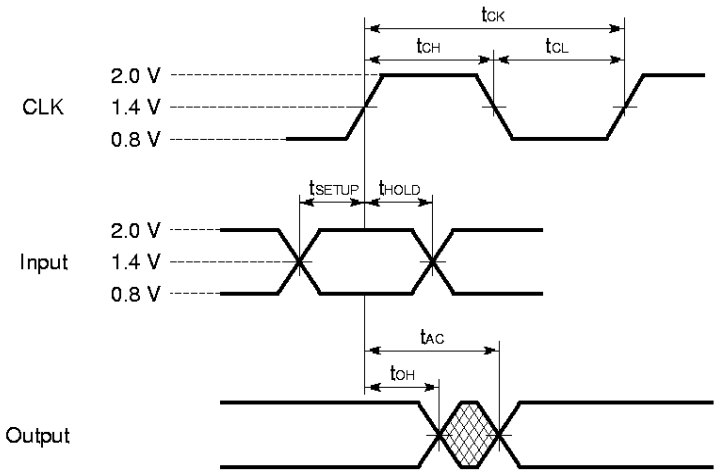
3. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

4. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

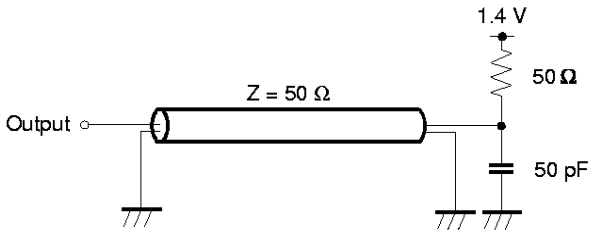
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

	Parameter		Symbol	-A10		-A12		Unit	Note
				MIN.	MAX.	MIN.	MAX.		
	Clock cycle time	/CAS latency = 3	t_{CK3}	10	(100 MHz)	12	(83 MHz)	ns	
		/CAS latency = 2	t_{CK2}	15	(67 MHz)	18	(55 MHz)	ns	
	Access time from CLK	/CAS latency = 3	t_{AC3}		8.5		9.5	ns	1
★		/CAS latency = 2	t_{AC2}		9.5		12.5	ns	1
	Input CLK duty cycle			40	60	40	60	%	
	Data-out hold time		t_{OH}	3.5		3.5		ns	1
	Data-out low-impedance time		t_{LZ}	0		0		ns	
	Data-out high-impedance time		t_{HZ}	3.5	8	3.5	8	ns	
	Data-in setup time		t_{DS}	3.0		3.5		ns	
	Data-in hold time		t_{DH}	1.5		2.0		ns	
	Address setup time		t_{AS}	3.5		3.5		ns	
	Address hold time		t_{AH}	0.5		0.5		ns	
	CKE setup time		t_{CKS}	3.5		3.5		ns	
	CKE hold time		t_{CKH}	0.5		0.5		ns	
	CKE setup time (Power down exit)		t_{CKSP}	3.0		3.5		ns	
	Command (/CS0, /RAS, /CAS, /WE, DQM) setup time		t_{CMS}	3.5		3.5		ns	
	Command (/CS0, /RAS, /CAS, /WE, DQM) hold time		t_{CMH}	0.5		0.5		ns	

Note 1. Output load



Asynchronous Characteristics

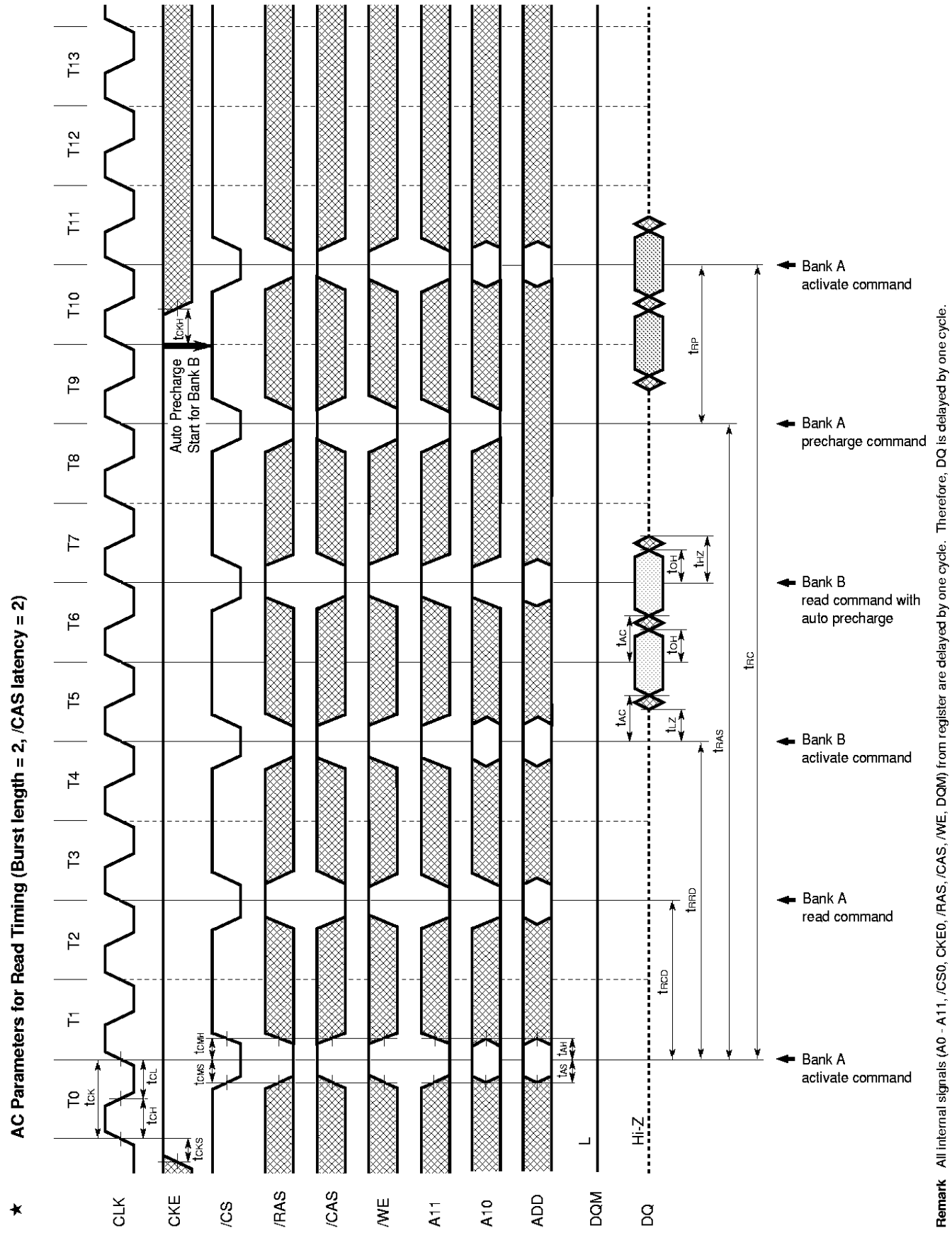
	Parameter		Symbol	-A10		-A12		Unit	Note
				MIN.	MAX.	MIN.	MAX.		
	REF to REF/ACT command period		t_{RC}	100		102		ns	
	ACT to PRE command period		t_{RAS}	60	120,000	72	120,000	ns	
	PRE to ACT command period		t_{RP}	30		30		ns	
	Delay time ACT to READ/WRITE command		t_{RCD}	30		30		ns	
	ACT(one) to ACT(another) command period		t_{RRD}	20		24		ns	
★	Data-in to PRE command period		t_{DPL}	–1CLK + 10		–1CLK + 12		ns	
★	Data-in to ACT(REF) command	/CAS latency = 3	t_{DAL3}	1CLK + 30		1CLK + 30		ns	
★	period (Auto precharge)	/CAS latency = 2	t_{DAL2}	30		30		ns	
	Mode register set cycle time		t_{RSC}	20		20		ns	
	Transition time		t_T	1	30	1	30	ns	
	Refresh time		t_{REF}		32		32	ms	

Relationship between Frequency and Latency

Speed version	-A10		-A12	
Clock cycle time [ns]	10	15	12	18
Frequency [MHz]	100	67	83	55
/CAS latency + 1 cycle	3 + 1	2 + 1	3 + 1	2 + 1
[t_{RCD}]	3	2	3	2
/RAS latency (/CAS latency + [t_{RCD}])	7	5	7	5
[t_{RC}]	10	7	9	6
[t_{RAS}]	6	4	6	4
[t_{RRD}]	2	2	2	2
[t_{RP}]	3	2	3	2
★ [t_{DPL}]	0	0	0	0
★ [t_{DAL}]	4	2	4	2

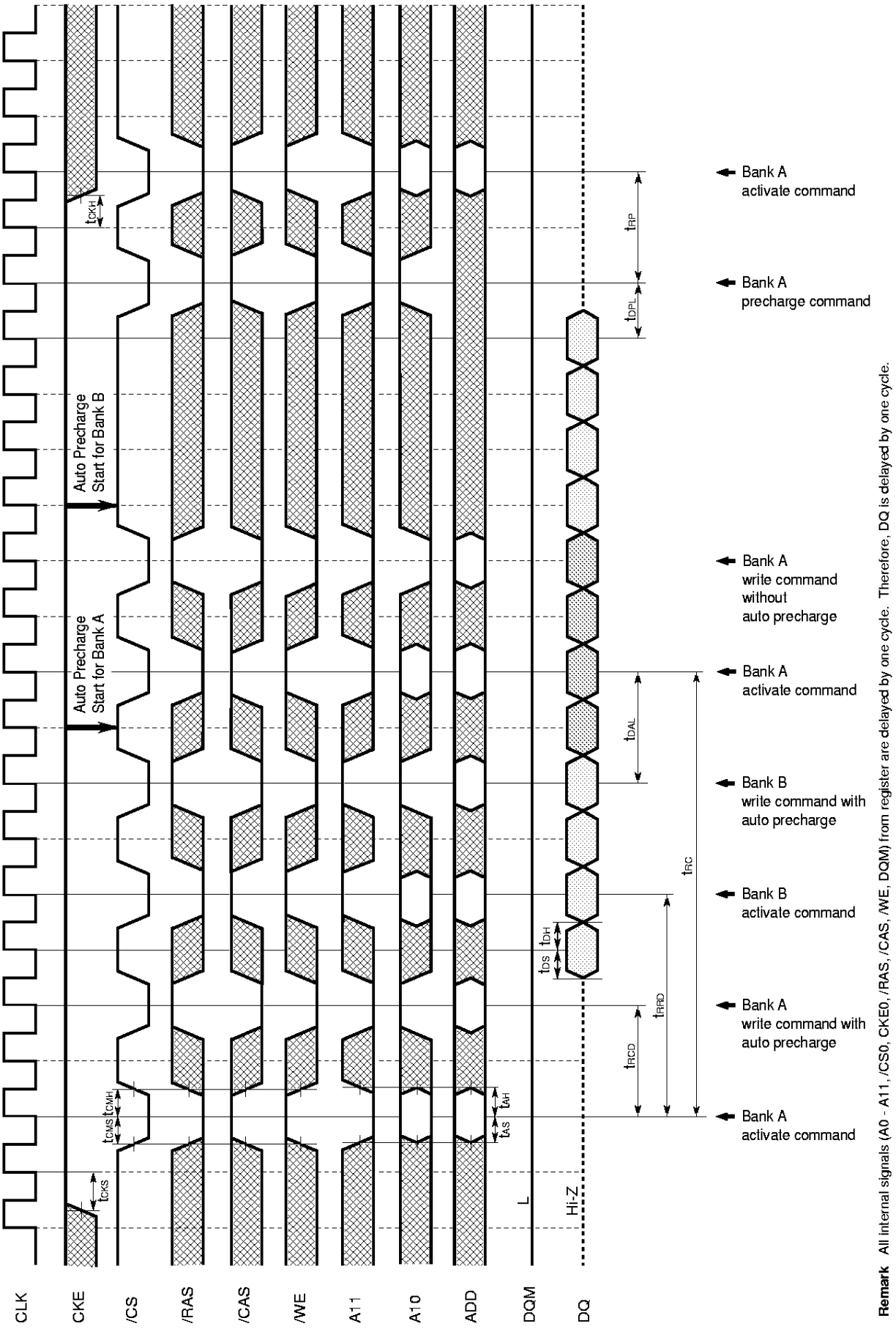
Remark All internal signals (A0 - A11, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

★ **AC Parameters for Read Timing (Burst length = 2, /CAS latency = 2)**



Remark All internal signals (A0 - A11, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

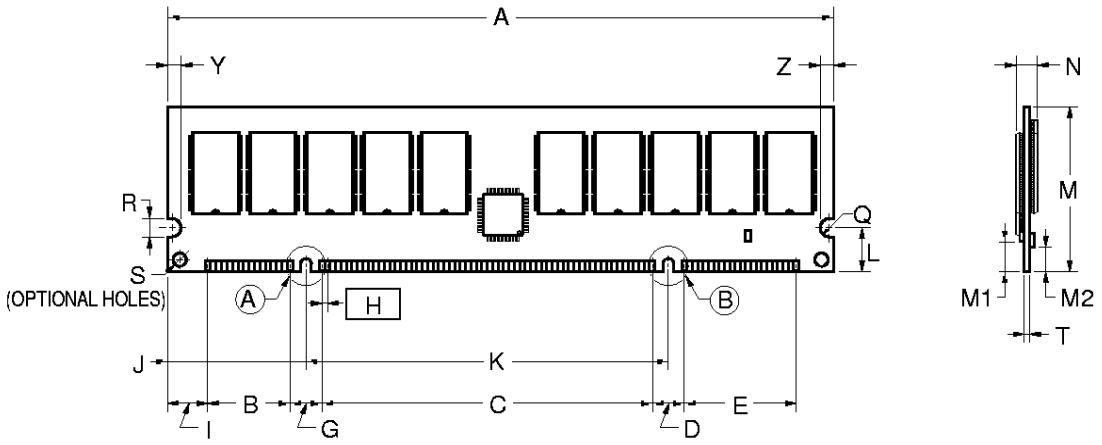
★ AC Parameters for Write Timing (Burst length = 4, /CAS latency = 2)

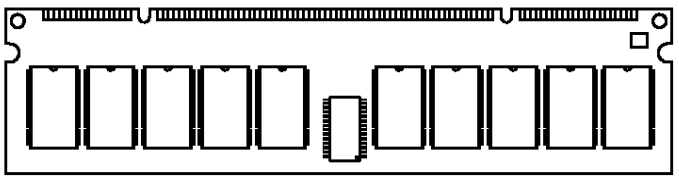


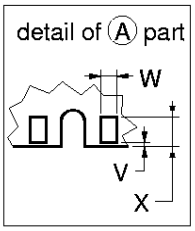
Remark All internal signals (A0 - A11, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

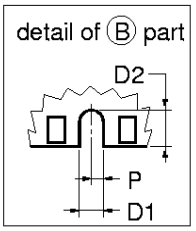
Package Drawing

200 PIN DUAL IN-LINE MODULE (SOKET TYPE)









ITEM	MILLIMETERS	INCHES
A	153.7±0.13	$6.051^{+0.006}_{-0.005}$
B	19.05	0.750
C	77.47	3.050
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	26.67	1.050
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.91	0.351
J	31.130	1.226
K	83.82	3.300
L	10.0	0.394
M	38.1±0.13	1.500±0.006
M1	6.52 MIN.	0.256 MIN.
M2	5.30 MIN.	0.208 MIN.
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.00±0.10	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS device must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]