FEATURES

- 1 GHz CLOCK FREQUENCY
  - 0 TO OVER 400 MHz OUTPUT FREQUENCY (STANDARD OPERATING CONDITIONS)
- LOWER COST 600 MHz CLOCK FREQUENCY VERSION AVAILABLE
- 32-BIT FREQUENCY RESOLUTION
  - 0.23 Hz @ 1 GHz CLOCK
- 2-BIT PHASE MODULATION (BPSK AND QPSK)
- 8-BIT PARALLEL SINE OUTPUT
  - 2 DEVICES CAN BE USED TO GENERATE QUADRATURE OUTPUT SIGNALS
- PHASE COHERENT INSTANTANEOUS FREQUENCY SWITCHING
- UP TO 62.5 MHz FREQUENCY HOPPING
- ECL INPUTS AND OUTPUTS FOR CONVENIENT INTERFACING
- 50Ω OUTPUTS
- 132-PIN CERAMIC FLATPACK

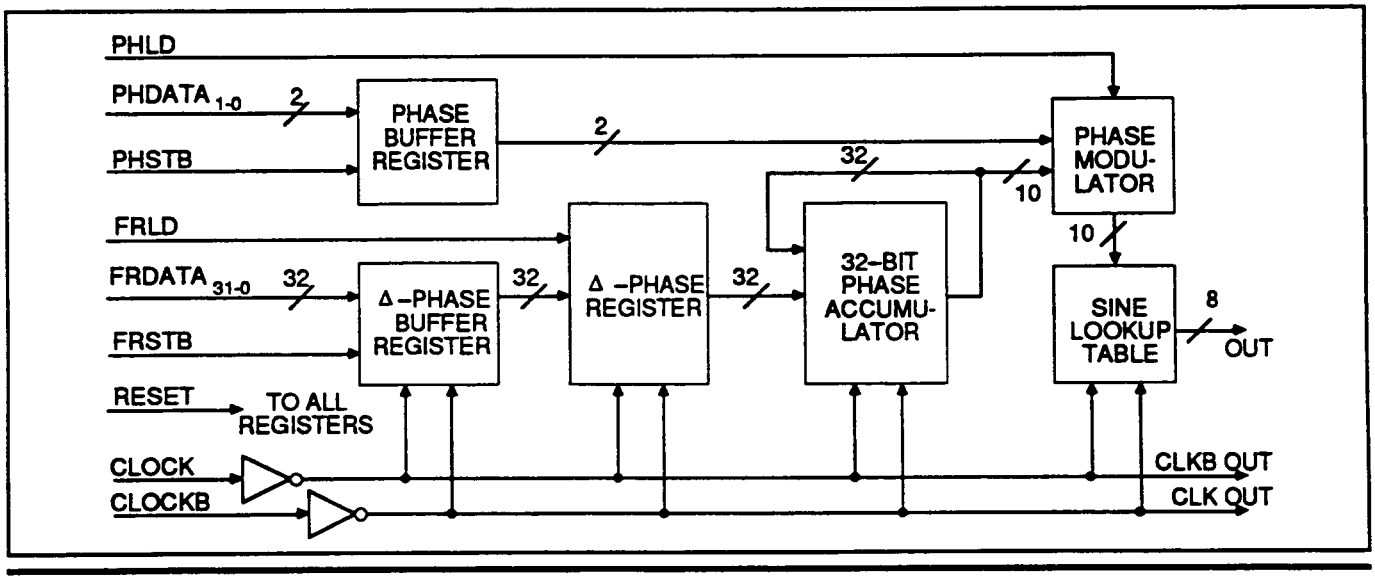
FUNCTIONAL DESCRIPTION

The STEL-2173 is a GaAs Modulated Numerically Controlled Oscillator (MNCO) which operates at clock frequencies up to 1 GHz and uses digital techniques to provide a cost-effective solution for precision very high frequency signal sources. This monolithic device is ideal for use in frequency synthesizers, frequency hoppers, and other precision frequency sources. It has a frequency resolution of 32 bits, making it possible to generate signals from 0 to more than 400 MHz with a resolution of 0.23 Hz. The device provides an 8-bit digitized sine wave output, making it possible to generate sine waves with better than 55 dB purity. The device also incorporates a 2-bit phase modulator, allowing it to be used to generate BPSK, and QPSK signals. In addition, two STEL-2173 NCOs can be used to generate quadrature signals by setting the phase modulation to 0° on one device and 90° on the other. Both the phase and frequency can be updated as rapidly as every sixteenth clock cycle, making this a very versatile device for hopped frequency and spread-spectrum applications. A lower cost version of the device operating at up to 600 MHz is also available

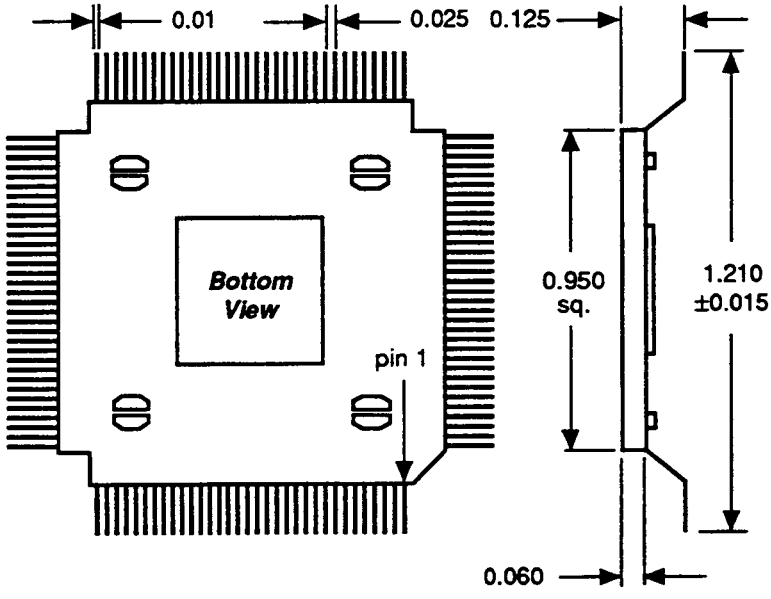
TYPICAL APPLICATIONS

- VHF/UHF FREQUENCY SYNTHESIZERS
- CHIRP GENERATORS
- VERY HIGH SPEED FREQUENCY HOPPED SOURCES

BLOCK DIAGRAM



PACKAGE SPECIFICATIONS



Note: Pin numbers increase in clockwise direction when package is viewed from bottom, as shown.

Materials:		
	Body	96% alumina ceramic
	Leads	Kovar
	Metallization	Tungsten/nickel/gold

Thermal Coefficient, θ_{jc} 7.5°C/watt

POWER DECOUPLING

The 8 pads on the back surface of the package are connected to the power supply pins and provide means to decouple the supply lines very close to the chip itself. It is recommended that 1000pF NPO chip capacitors be mounted directly on these pads to decouple V_{EE} to V_{SS}.

ORDERING INFORMATION

STEL-2713+X/CP Commercial grade (0° to +70° C), 132-pin CQFP Package
STEL-2713+X/CB Commercial grade (0° to +70° C), Unpackaged Die
STEL-2173+X/MP MIL STD 883C grade (–55° to +125° C), 132-pin CQFP Package
STEL-2173+X/MP (–55° to +125° C), Unpackaged Die with MIL-STD-883C Visual Inspection

Specify: X = 6 for 600 MHz speed option
X = 10 for 1000 MHz (1 GHz) speed option

e.g. STEL-2173+10/CP: Commercial grade, packaged, 1 GHz speed grade

PIN CONNECTIONS

1	V_{EE}	34	V_{EE}	67	V_{EE}	100	V_{EE}
2	N.C.	35	N.C.	68	N.C.	101	N.C.
3	$FRDATA_8$	36	$FRDATA_{24}$	69	N.C.	102	OUT_5
4	V_{SS}	37	V_{SS}	70	V_{SS}	103	V_{SS}
5	$FRDATA_9$	38	$FRDATA_{25}$	71	N.C.	104	OUT_4
6	$FRDATA_{10}$	39	$FRDATA_{26}$	72	$PHDATA_0$	105	OUT_3
7	V_{SS}	40	V_{SS}	73	V_{SS}	106	V_{SS}
8	$FRDATA_{11}$	41	$FRDATA_{27}$	74	N.C.	107	OUT_2
9	$FRDATA_{12}$	42	$FRDATA_{28}$	75	$PHDATA_1$	108	OUT_1
10	V_{SS}	43	V_{SS}	76	V_{SS}	109	V_{SS}
11	$FRDATA_{13}$	44	$FRDATA_{29}$	77	PHSTB	110	$OUT_{0(LSB)}$
12	$FRDATA_{14}$	45	$FRDATA_{30}$	78	PHLD	111	FRLD
13	V_{SS}	46	V_{SS}	79	V_{SS}	112	V_{SS}
14	$FRDATA_{15}$	47	$FRDATA_{31}$	80	N.C.	113	FRSTB
15	N.C.	48	N.C.	81	N.C.	114	N.C.
16	V_{SS}	49	V_{SS}	82	V_{SS}	115	V_{SS}
17	N.C.	50	N.C.	83	N.C.	116	N.C.
18	V_{SS}	51	V_{SS}	84	V_{SS}	117	V_{SS}
19	N.C.	52	N.C.	85	N.C.	118	N.C.
20	$FRDATA_{16}$	53	N.C.	86	VREF	119	$FRDATA_0$
21	V_{SS}	54	V_{SS}	87	V_{SS}	120	V_{SS}
22	$FRDATA_{17}$	55	VREF	88	CLOCKB	121	$FRDATA_1$
23	$FRDATA_{18}$	56	N.C.	89	CLOCK	122	$FRDATA_2$
24	V_{SS}	57	V_{SS}	90	V_{SS}	123	V_{SS}
25	$FRDATA_{19}$	58	N.C.	91	RESET	124	$FRDATA_3$
26	$FRDATA_{20}$	59	N.C.	92	N.C.	125	$FRDATA_4$
27	V_{SS}	60	V_{SS}	93	V_{SS}	126	V_{SS}
28	$FRDATA_{21}$	61	N.C.	94	CLK OUT	127	$FRDATA_5$
29	$FRDATA_{22}$	62	N.C.	95	CLKB OUT	128	$FRDATA_6$
30	V_{SS}	63	V_{SS}	96	V_{SS}	129	V_{SS}
31	$FRDATA_{23}$	64	N.C.	97	OUT_7	130	$FRDATA_7$
32	N.C.	65	N.C.	98	OUT_6	131	N.C.
33	V_{EE}	66	V_{EE}	99	V_{EE}	132	V_{EE}

Note: N.C. denotes No Connection.

CIRCUIT DESCRIPTION

The NCO maintains a record of phase which is accurate to 32 bits. At each clock cycle the number stored in the 32-bit Δ-Phase Register is added to the previous value of the Phase Accumulator. The number in the Phase Accumulator represents the current phase of the synthesized sine and cosine functions. The number in the Δ-Phase Register represents the phase change for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{32}}$$

where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

The sine functions are generated from the ten most significant bits of the phase accumulator.

The NCO generates a sampled sine wave where the sampling function is the clock. The practical upper limit of the NCO output frequency is about 40% of the clock frequency due to spurious components that are created by sampling. Those components are at frequencies greater than half the clock frequency, and become more difficult to remove by filtering as the output frequency approaches half the clock frequency.

The phase noise of the NCO output signal may be determined from the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 23 clock cycles. The pipeline delay associated with the phase modulator is only 7 clock cycles, since the phase modulating function is at the output of the accumulator. Note that when a phase or frequency change occurs at the output the change is instantaneous, i.e., it occurs in one clock cycle, with complete phase coherence.

FUNCTION BLOCK DESCRIPTION

Δ-PHASE BUFFER REGISTER BLOCK

The Δ-Phase Buffer Register is used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously on the rising edge of **FRSTB**. The data is transferred from this register into the Δ-Phase Register after a falling edge on the **FRLD** input.

PHASE BUFFER REGISTER BLOCK

The Phase Buffer Register is used to temporarily store the Phase data written into the device. This allows the data to be written asynchronously on the rising edge of **PHSTB**. The data is transferred from this register into the Phase ALU after a falling edge on the **PHLD** input.

Δ-PHASE REGISTER BLOCK

This block controls the updating of the Δ-Phase word used in the Accumulator. The frequency data from the Δ-Phase Buffer Register is loaded into this block after a falling edge on the **FRLD** input.

PHASE ACCUMULATOR BLOCK

This block forms the core of the NCO function. It is a high-speed, pipelined, 32-bit parallel accumulator, generating a new sum in every clock cycle. The overflow signal is discarded, since the required output is the modulo(2^{32}) sum only. This represents the modulo(2π) phase angle.

PHASE ALU BLOCK

The Phase ALU performs the addition of the PM data to the Phase Accumulator output. The PM data word is 2 bits wide, and this is added to the 2 most significant bits of the Phase Accumulator output to form the modulated phase used to address the look-up table.

SINE LOOK-UP TABLE BLOCK

This block is the sine memory. The 10 bits from the Phase ALU are used to address this memory to generate the 8-bit $OUT_{7:0}$ outputs.

INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 1 nsec, and normal operation will resume after this signal returns high. The data on the OUT_{7-0} bus will then be invalid for 5 clock cycles, and thereafter will remain at the value corresponding to zero phase until new frequency or phase modulation data is loaded with the **FRLD** or **PHLD** inputs after the **RESET** returns high.

CLOCK and CLOCKB
All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 600/800/1000 MHz, depending on speed grade. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 400 picoseconds. **CLOCKB** is the inverse phase clock input.

$FRDATA_{31}$ through $FRDATA_0$
The 32-bit $FRDATA_{31-0}$ bus is used to program the 32-bit Δ-Phase Buffer Register. $FRDATA_0$ is the least significant bit of the bus. The data programmed into the Δ-Phase Register in this way determines the output frequency of the NCO.

FRSTB
The Frequency Strobe input is used to latch the data on the $FRDATA_{31-0}$ bus into the device. On the rising edge of the **FRSTB** input, the information on the 32-bit data bus is transferred to the Δ-Phase Buffer Register.

FRLD
The Frequency Load input is used to control the transfer of the data from the Δ-Phase Buffer Register to the Δ-Phase Register. The data at the output of the Δ-Phase Buffer Register must be valid during the clock cycle following the falling edge of **FRLD**. The data is then transferred during the subsequent cycle. The frequency of the NCO output will change 24 clock cycles after the falling edge of **FRLD**, due to pipelining delays.

$PHDATA_1$ through $PHDATA_0$
The 2-bit $PHDATA_{1-0}$ bus is used to program the 2-bit Phase Buffer Register. $PHDATA_0$ is the least significant bit of the bus. The data programmed into the Phase ALU in this way determines the output phase of the NCO relative to the zero offset sine output.

PHSTB
The Phase Strobe input is used to latch the data on the $PHDATA_{1-0}$ bus into the device. On the rising edge of the **PHSTB** input, the information on the 2-bit data bus is transferred to the Phase Buffer Register.

PHLD
The Phase Load input is used to control the transfer of the data from the Phase Buffer Register to the Phase ALU. The data at the output of the Phase Buffer Register must be valid during the clock cycle following the falling edge of **PHLD**. The phase of the NCO output will change 8 clock cycles after the falling edge of **PHLD**, due to pipelining delays.

OUTPUT SIGNALS

OUT_{7-0}
The signal appearing on the OUT_{7-0} output bus is derived from the 10 most significant bits of the Phase Accumulator. The 8-bit sine function is presented in offset binary format. The value of the output for a given phase value follows the relationship:

$$OUT_{7-0}=127 \times \sin(360 \times (phase+0.5)/1024)^\circ+128$$

The result is accurate to within 1 LSB. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 129 (81_H).

CLK OUT and CLKB OUT
The clock signals used to latch the output data into the output registers are brought out on the **CLK OUT** and **CLKB OUT** pins. **CLKB OUT** is the inverse phase clock. The output data changes on the rising edges of **CLK OUT**.

VREF
An internal reference generator provides a –1.3 volt reference for the ECL input comparators. The output of this reference generator is available at the **VREF** pins. Since the generator has a high output impedance this voltage can be modified by connecting a different voltage source to these pins.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–55 to +125	°C
V_{EEmax}	Supply voltage on V_{EE}	0 to –7	volts
$V_{I(max)}$	Input voltage	0.5 to V_{EE}–0.5	volts
$V_{O(max)}$	Output voltage	0.5 to V_{EE}–0.5	volts
I_I	DC input current	± 1	mA
I_O	DC output current	40	mA

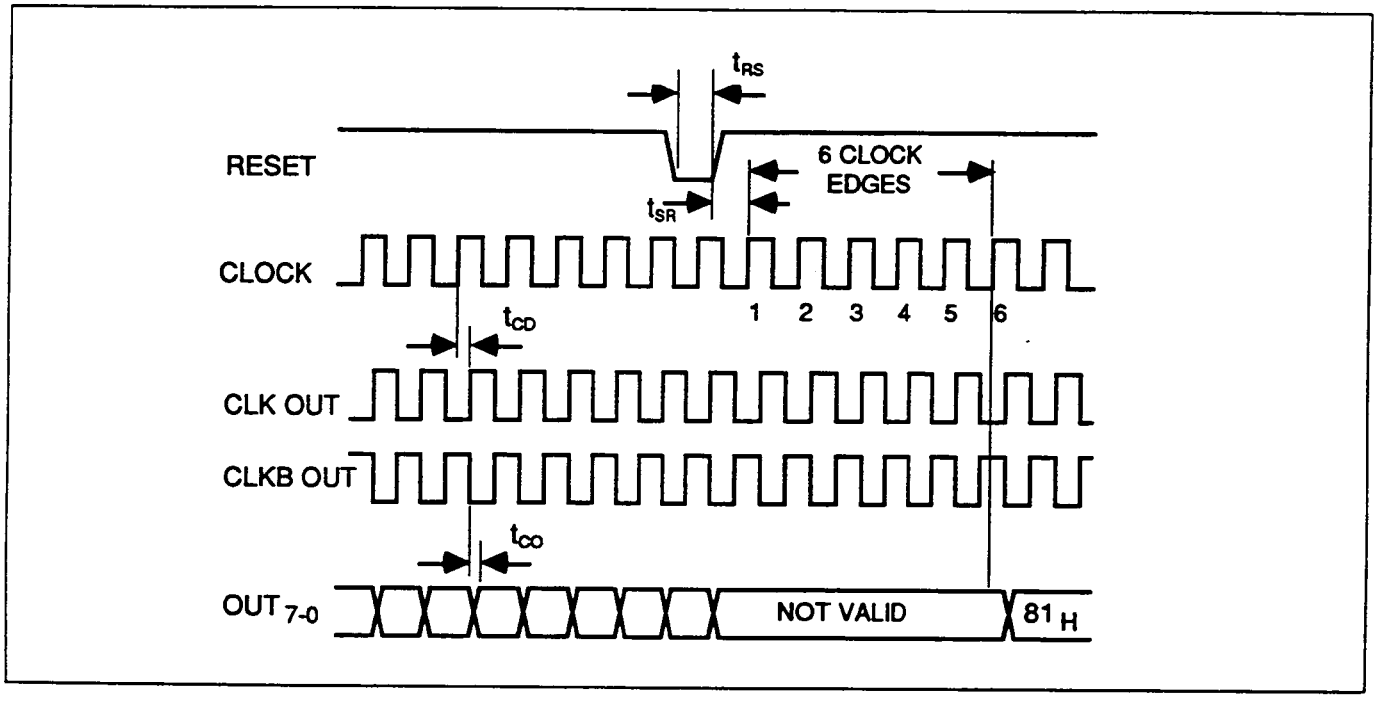
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{EE}	Supply Voltage	–5 ± 5%	Volts (Commercial Conditions)
		–5 ± 10%	Volts (Military Conditions)
T_c	Operating Temperature (Case)	0 to +70	°C (Commercial Conditions)
		–55 to +125	°C (Military Conditions)

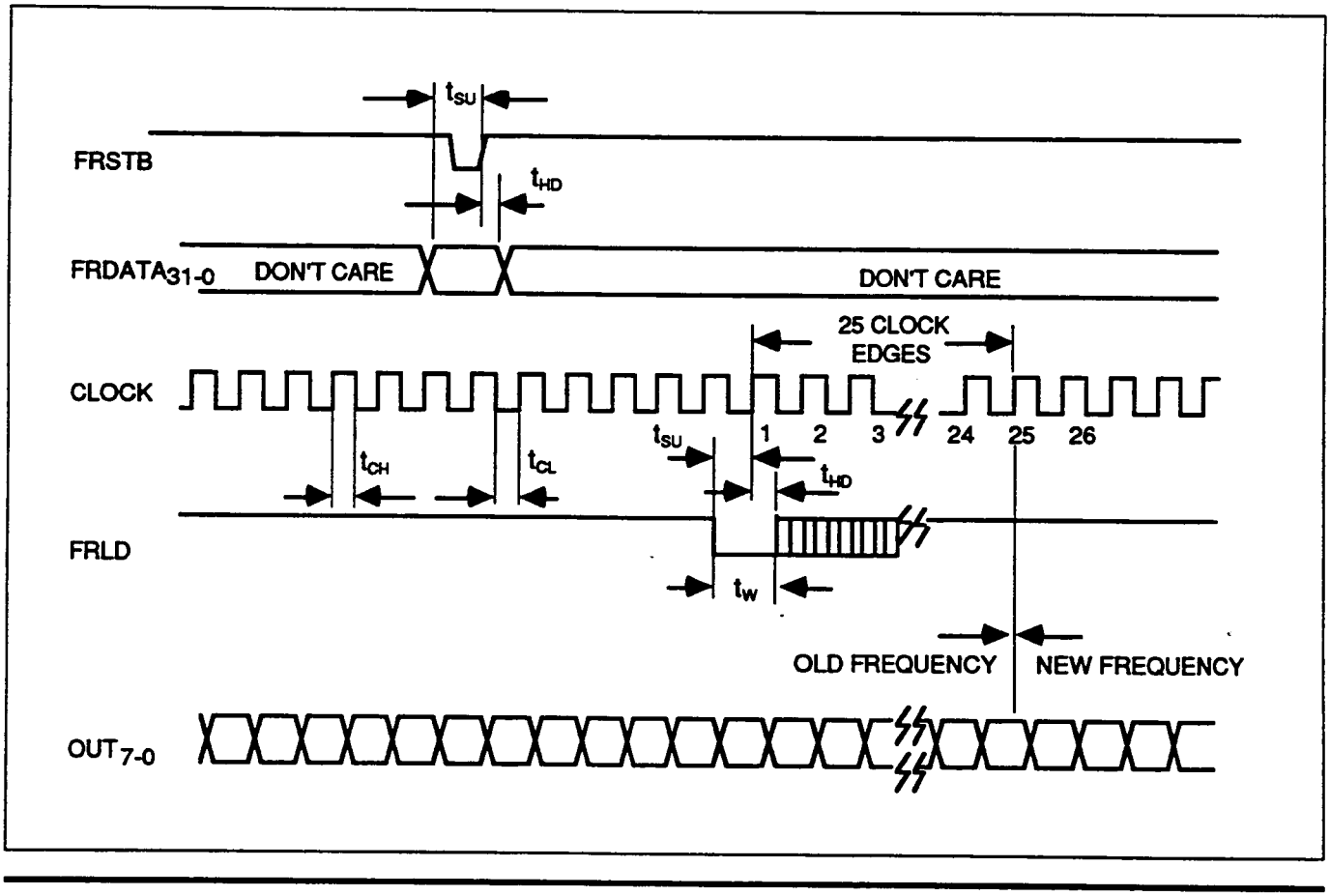
D.C. CHARACTERISTICS (Operating Conditions: V_{EE}= –5.0 V ±5%, V_{SS}=0 V, T_c= 0° to 70° C, Commercial
V_{EE}= –5.0 V ±10%, V_{SS}=0 V, T_c=–55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{EE}	Supply Current, Operational		1.2		A	f_{CLK} = 1 GHz
$V_{IH(min)}$	High Level Input Voltage					
	Extended Operating Conditions	–1.1		0	volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage	-2.0		–1.5	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current			10	µA	V_I = 0 volts
$I_{IL(max)}$	Low Level Input Current			–10	µA	V_I = –2.0 volts
$V_{OH(min)}$	High Level Output Voltage	–1.0		–0.5	volts	R_L = 50Ω to –2.0 volts
$V_{OL(max)}$	Low Level Output Voltage	–2.0		–1.6	volts	R_L = 50Ω to –2.0 volts
$I_{OH(min)}$	High Level Output Current	20	23	30	mA	R_L = 50Ω to –2.0 volts
$I_{OL(max)}$	Low Level Output Current	0	5	8	mA	R_L = 50Ω to –2.0 volts
	($I_{OH(min)}$ and $I_{OL(max)}$ are not tested.)					
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

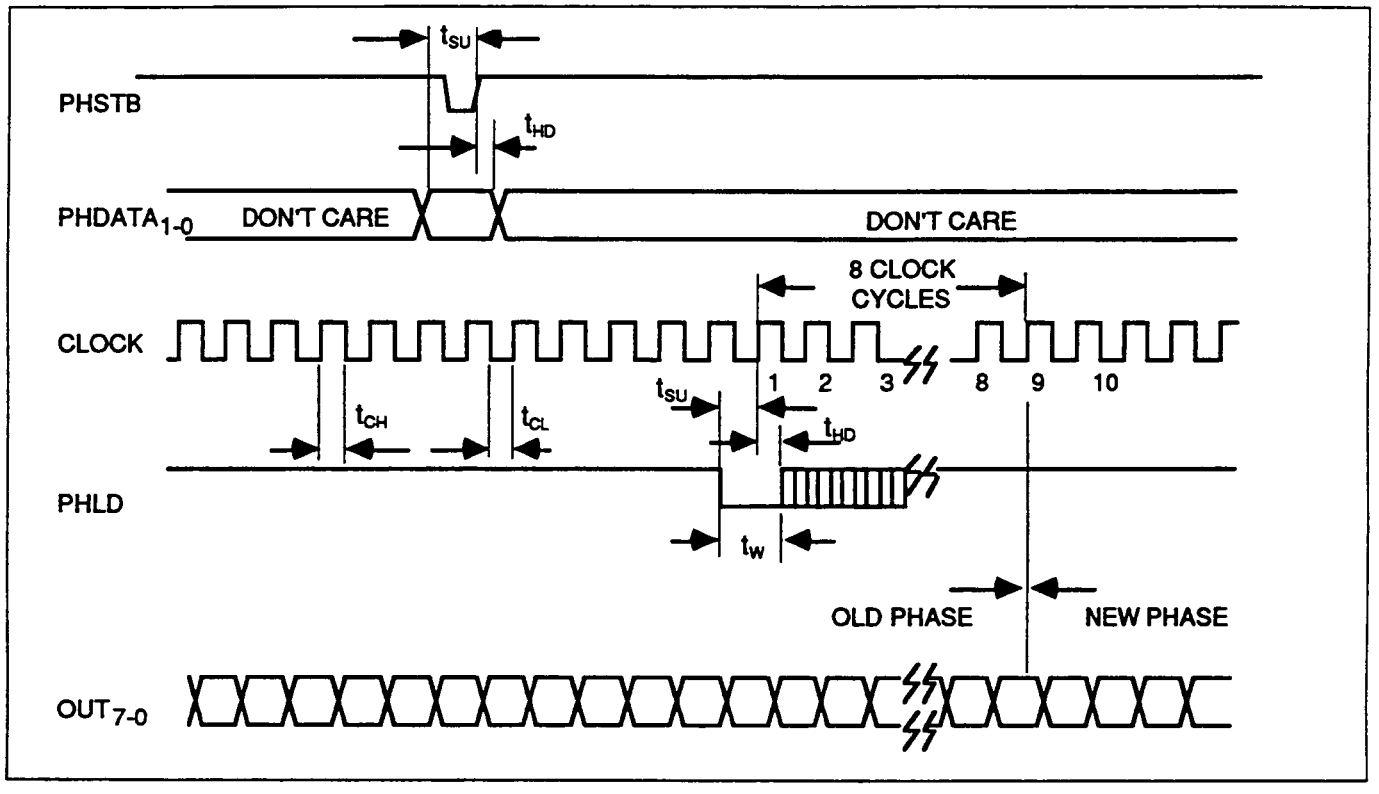
NCO RESET SEQUENCE



NCO FREQUENCY CHANGE SEQUENCE



NCO PHASE CHANGE SEQUENCE

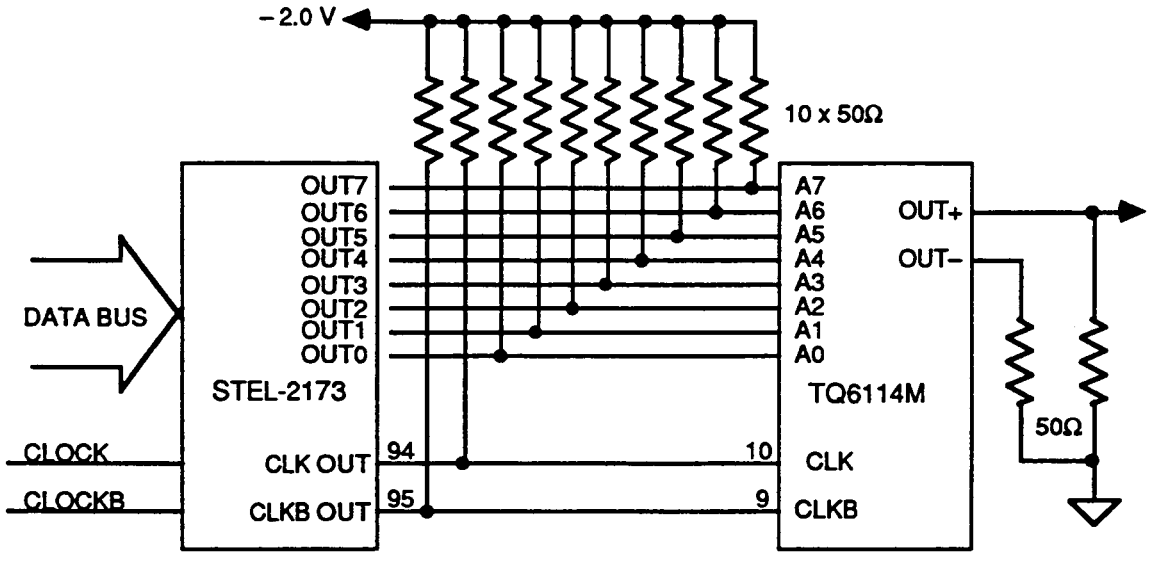


ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS (Operating Conditions: V_{EE}= –5.0 V ± 5%, V_{SS}=0 V, T_c= 0° to 70° C, Commercial
V_{EE}= –5.0 V ± 10%, V_{SS}=0 V, T_c=–55° to 125° C, Military)

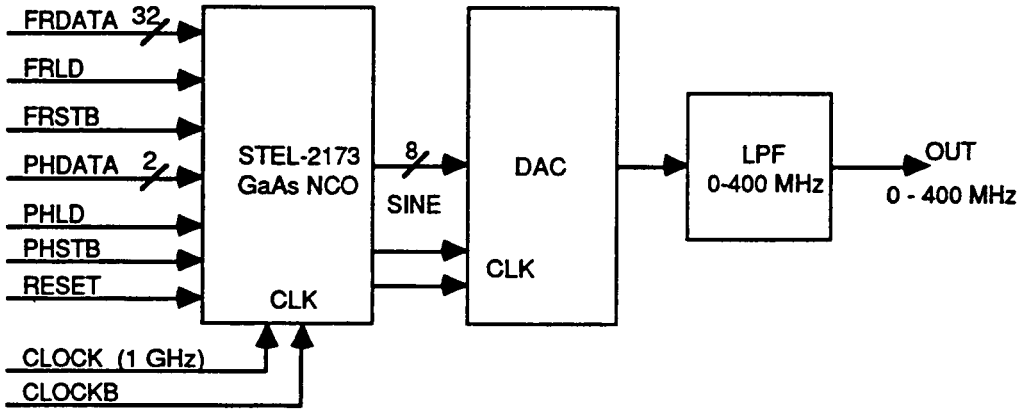
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{RS}	**RESET** pulse width	750			psec.	
t_{SR}	**RESET** to **CLOCK** Setup	750			psec.	
t_{SU}	**FRDATA**, or **PHDATA** to **FRSTB** or **PHSTB** Setup, and **FRLD** or **PHLD** to **CLOCK** Setup		100		psec.	
t_{HD}	**FDATA**, or **PHDATA** to **FRSTB** or **PHSTB** Hold, and **FRLD** or **PHLD** to **CLOCK** Hold		50		psec.	
t_{CH}	**CLOCK** high	400			psec.	f_{CLK} = 1 GHz
t_{CL}	**CLOCK** low	400			psec.	f_{CLK} = 1 GHz
t_W	**FRSTB**, **PHSTB**, **FRLD** or **PHLD** pulse width		1000		psec.	
t_{CD}	**CLOCK** to **CLK OUT** delay		1500		psec.	Load = 15 pF max.
t_{CO}	**CLK OUT** to output delay (All outputs)		300		psec.	Load = 15 pF max.

INTERFACING THE STEL-2173 TO THE TQ6114 DAC



Care must be taken when using the STEL-2173 with a Digital to Analog converter because of the high frequencies involved. Great care must be taken to ensure that the power supplies are properly decoupled, especially the –5 volt supply. The preferred practice is to use a 4 layer printed circuit board, using one layer as a ground plane and another as a –5 volt supply plane. In this way the transients in the ground plane can be minimized, and the analog output purity maximized. It is recommended that four 1000pF chip capacitors be connected between the supply lines and ground at every one of the supply pins.

TYPICAL APPLICATION
A FAST SWITCHING DC TO 400 MHz SYNTHESIZER



If the output of the STEL-2173 is fed into a high-speed D-to-A converter, such as the TriQuint TQ6112, a phase coherent, fast switching frequency synthesizer may be realized. The spurious components at the output of the low-pass filter will be about 55 dB below the primary ouput component. If the clock frequency is set to 858.9935 MHz (0.2 x 2^{32} Hz), the frequency steps obtainable will be exactly 0.2 Hz. Similarly, if the clock frequency is set to 1073.7418 MHz (0.25 x 2^{32} Hz), the frequency steps obtainable will be exactly 0.25 Hz. The output frequency may be programmed from DC to over 400 MHz, the limit depending on the sharpness of the low-pass filter. In order to keep the sampling components above the Nyquist frequency at a level compatible with the other spurious components, the low-pass filter will need to have at least 55 dB of attenuation above $f_c - f_o$, where f_c is the clock frequency and f_o is the highest output frequency desired.

SPECTRAL PURITY

In many applications, the STEL-2173 GaAs-NCO is used with a digital-to-analog converter to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables, including phase quantization, amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the D/A converter.

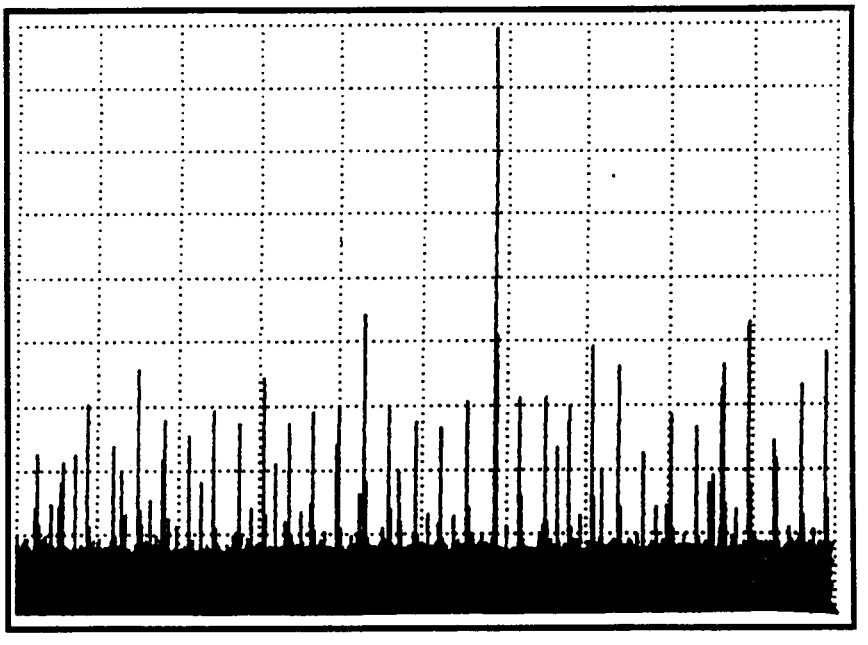
The sine function produced by the STEL-2173 has 8-bit amplitude quantization and 10-bit phase quantization which result in spurious levels which are theoretically about –55dBc. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), so spurious components which occur at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency of the STEL-2173 approaches $f_c/2$, an "image" spurious component also approaches $f_c/2$ from above. If the programmed output frequency is only slightly below $f_c/2$, it is virtually impossible to remove the "image" spurious component just above $f_c/2$ by filtering. For this reason, the maximum practical output frequency of the STEL-2173 should be limited to about 40% of the clock frequency.

Probably the most significant contribution to spectral purity is the dynamic performance of the D/A converter (DAC). To minimize these effects, connections between the DAC and STEL-2173 should be kept equal length using transmission line techniques. The analog output of the DAC should be isolated from the clock signal and other digital signals as much as possible. Grounding and decoupling should be done with the objective of optimizing the step response of the DAC.

A spectral plot of the NCO output after conversion with a DAC (Tri-Quint TQ6114) is shown below. In this case, the clock frequency is 1 GHz and the output frequency is programmed to 234.567 MHz. The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –44 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to obtain a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Frequency Span:	0 – 400 MHz
Reference Level:	+0 dBm
Resolution Bandwidth:	10 KHz
Scale:	Log, 10 dB/div
Output frequency:	234.567 MHz
Clock frequency:	1 GHz



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