MH2M32EJ-6,-7,-8/
MH2M32SEJ-6,-7,-8

FAST PAGE MODE 67108864-BIT(2097152-WORD BY 32-BIT)DYNAMIC RAM

DESCRIPTION

The MH2M32EJ/SEJ is 2097152-word × 32-bit dynamic RAM. This consists of sixteen industry standard 1M × 4 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module, suitable for easy interchange or addition of modules.

FEATURES

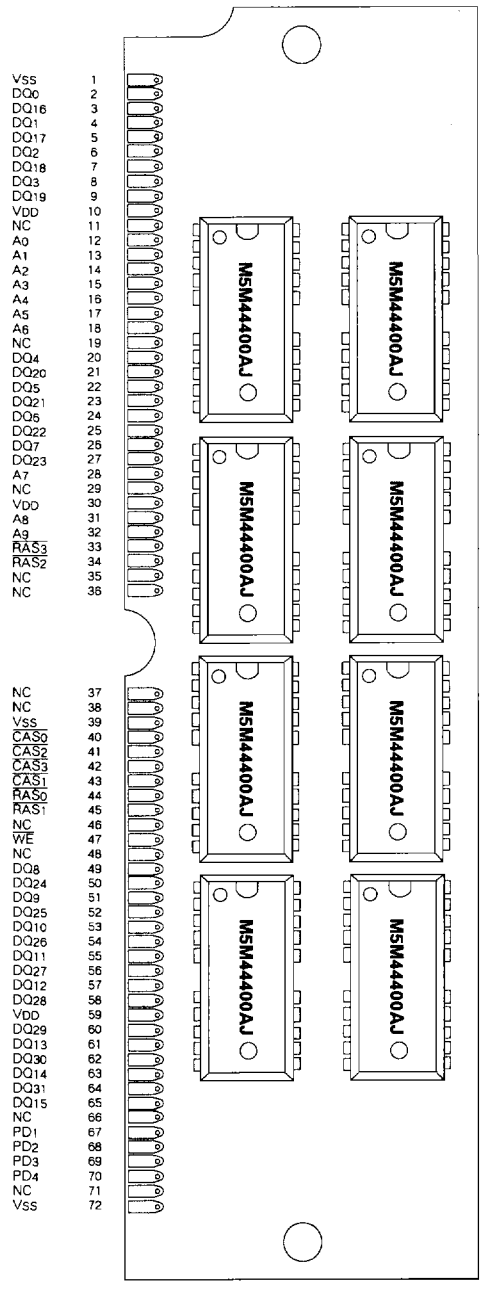
Type name	$\overline{RAS}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (Typ.mW)	PCB's contacts
MH2M32EJ-6	60	120	3240	Gold plating
MH2M32EJ-7	70	140	2840	
MH2M32EJ-8	80	160	2440	
MH2M32SEJ-6	60	120	3240	Solder plating
MH2M32SEJ-7	70	140	2840	
MH2M32SEJ-8	80	160	2440	

- Utilizes industry standard 1M × 4 RAMs in SOJ
- Single 5V ± 10% supply
- Low stand-by power dissipation
  88mW (max) ·····CMOS Input level
- Low operating power dissipation
  MH2M32EJ/SEJ-6·····4444mW (max)
  MH2M32EJ/SEJ-7·····3784mW (max)
  MH2M32EJ/SEJ-8·····3344mW (max)
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 72-pins single in-line package
- Includes decoupling capacitors (0.22 μF × 16)
- Fast page mode capability

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW) [Both side]



	-6	-7	-8
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	GND	NC
PD4	NC	NC	GND

Outline 72N9J

NC : NO CONNECTION

FUNCTION

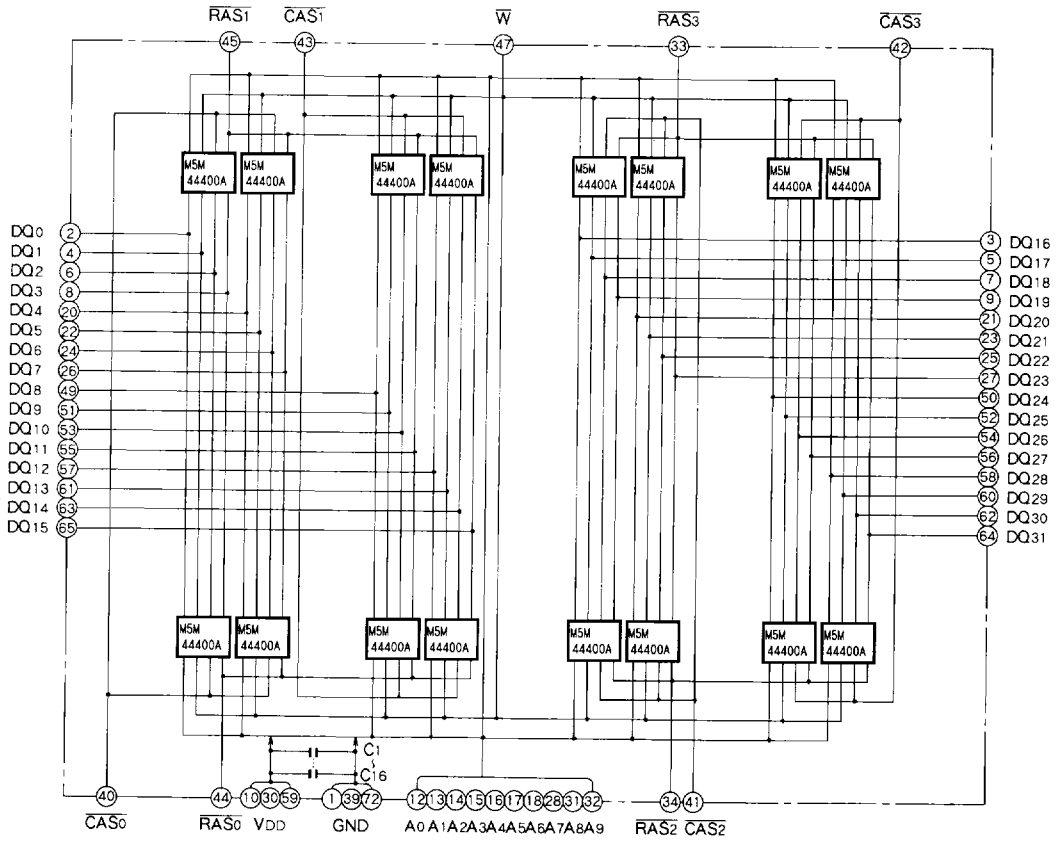
The MH2M32EJ/SEJ provide, in addition to normal read, and write operations, a number of other functions, e.g., Fast page mode, $\overline{RAS}$ only refresh. The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	− 1~7	V
V_I	Input voltage		− 1~7	V
V_O	Output voltage		− 1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	16	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 40~125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	− 2.0		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = − 5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	− 20		20	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	− 10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	MH2M32EJ, SEJ-6	$\overline{RAS}$, $\overline{CAS}$ cycling			816	mA
		MH2M32EJ, SEJ-7	t_{RC} = t_{WC} = min.			696	
		MH2M32EJ, SEJ-8	output open			616	
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by (Note 5)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			32	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5, output open			16	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	MH2M32EJ, SEJ-6	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}			816	mA
		MH2M32EJ, SEJ-7	t_{RC} = min.			696	
		MH2M32EJ, SEJ-8	output open			616	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	MH2M32EJ, SEJ-6	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling			816	mA
		MH2M32EJ, SEJ-7	t_{PC} = min.			696	
		MH2M32EJ, SEJ-8	output open			616	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH2M32EJ, SEJ-6	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			696	mA
		MH2M32EJ, SEJ-7	t_{RC} = min.			616	
		MH2M32EJ, SEJ-8	output open			536	

Note 2 : Current flowing into an IC is positive, out is negative.
3 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = V_{SS} f = 1MHz V_i = 25mVrms			140	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				140	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				70	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				50	pF
C_O	Output capacitance	V_O = V_{SS}, f = 1MHz, V_i = 25mVrms			25	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter	Limits						Unit
		MH2M32EJ, SEJ-6		MH2M32EJ, SEJ-7		MH2M32EJ, SEJ-8		
		Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 6, 7)		15		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 6, 8)		60		70		80	ns
t_{AA}	Column address access time (Note 6, 9)		30		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 6, 10)		35		40		45	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 11)	0	15	0	20	0	20	ns

Note 5 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6 : Measured with a load circuit equivalent to 2TTL loads and 100pF.
7 : Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).
8 : Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
9 : Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max).
10 : Assumes that $t_{CP} \leq t_{CP}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).
11 : t_{OFF} (max) defines the time at which the output achieves the high impedance state ($I_{out} \leq | \pm 10\ \mu A |$) and is not reference to V_{OH} (min) or V_{OL} (max).

TIMING REQUIREMENTS (For Read, Write, Refresh, and Fast-Page Mode Cycles)
(T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 12, 13)

Symbol	Parameter	Limits						Unit
		MH2M32EJ, SEJ-6		MH2M32EJ, SEJ-7		MH2M32EJ, SEJ-8		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		16.4		16.4		16.4	ms
t_{RP}	$\overline{RAS}$ high pulse width	50		60		70		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 14)	20	45	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 15)	15	30	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 16)	0	10	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		15		ns
t_T	Transition time (Note 17)	1	50	1	50	1	50	ns

Note 12 : The timing requirements are assumed t_T = 5ns.
13 : V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
14 : t_{RCD} (max) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max), access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC} or t_{AA}. t_{RCD} (min) is specified as t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min).
15 : t_{RAD} (max) is specified as a reference point only. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max), access time is controlled exclusively by t_{AA}.
16 : t_{ASC} (max) is specified as a reference point only. If $t_{RCD} \geq t_{RCD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max), access time is controlled exclusively by t_{CAC}.
17 : t_T is measured between V_{IH} (min) and V_{IL} (max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH2M32EJ, SEJ-6		MH2M32EJ, SEJ-7		MH2M32EJ, SEJ-8		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	120		140		160		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 18)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		40		ns

Note 18 : Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write Cycles)

Symbol	Parameter	Limits						Unit
		MH2M32EJ, SEJ-6		MH2M32EJ, SEJ-7		MH2M32EJ, SEJ-8		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	120		140		160		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 21)	0		0		0		ns
tWP	Write pulse width	10		15		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		15		ns

Fast Page Mode Cycle (Read, Write Cycles) (Note 22)

Symbol	Parameter	Limits						Unit
		MH2M32EJ, SEJ-6		MH2M32EJ, SEJ-7		MH2M32EJ, SEJ-8		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		50		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 23)	105	200000	115	200000	130	200000	ns
tCP	$\overline{CAS}$ high pulse width (Note 24)	10	15	10	20	10	20	ns

Note 22 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
23 : tRAS (min) is specified as two cycles of $\overline{CAS}$ input are performed.
24 : tCP (max) is specified as a reference point only.

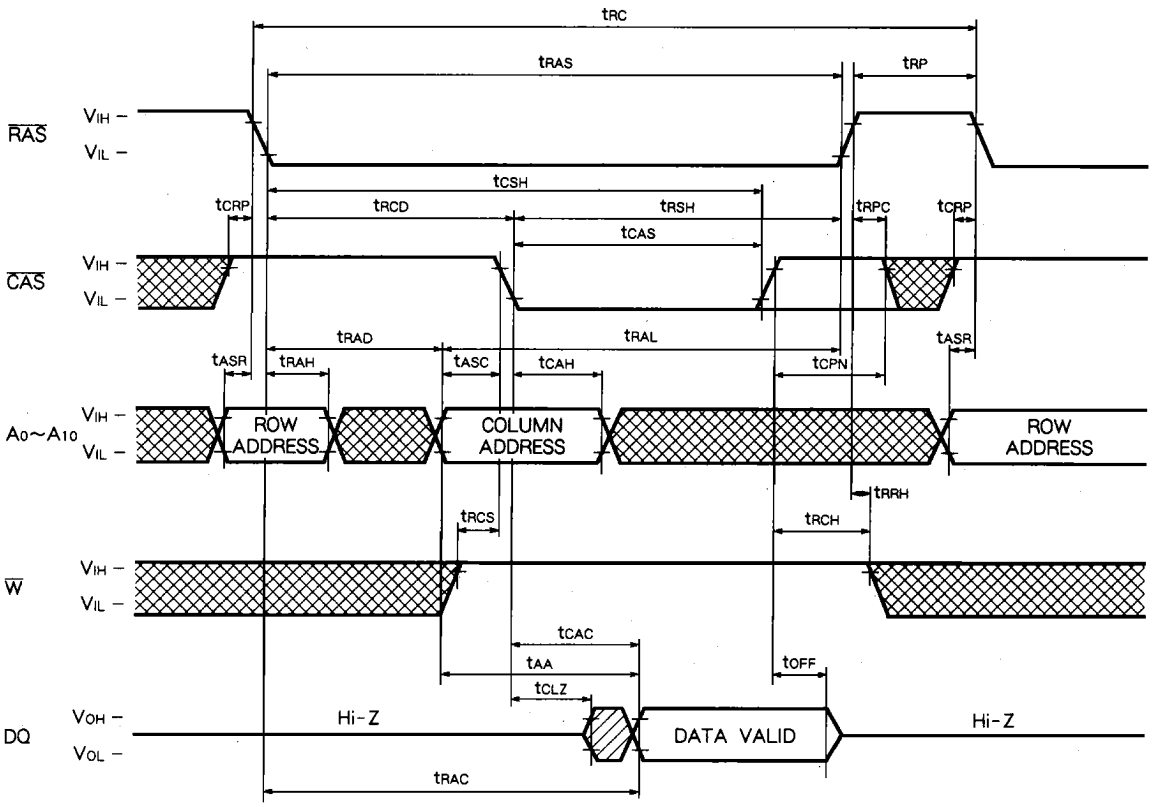
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)

Symbol	Parameter	Limits						Unit
		MH2M32EJ, SEJ-6		MH2M32EJ, SEJ-7		MH2M32EJ, SEJ-8		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		15		15		ns
tCAS	$\overline{CAS}$ low pulse width	25		30		30		ns

Note 25 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 26)

Read Cycle

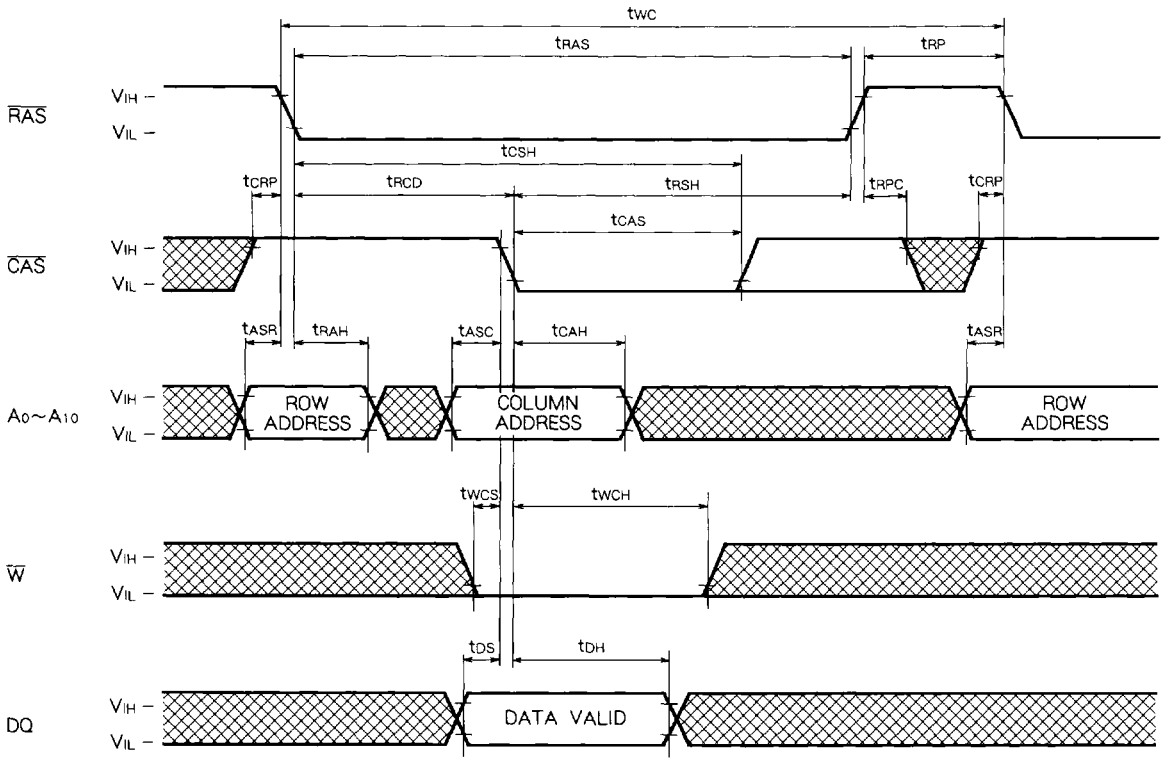


Note 26

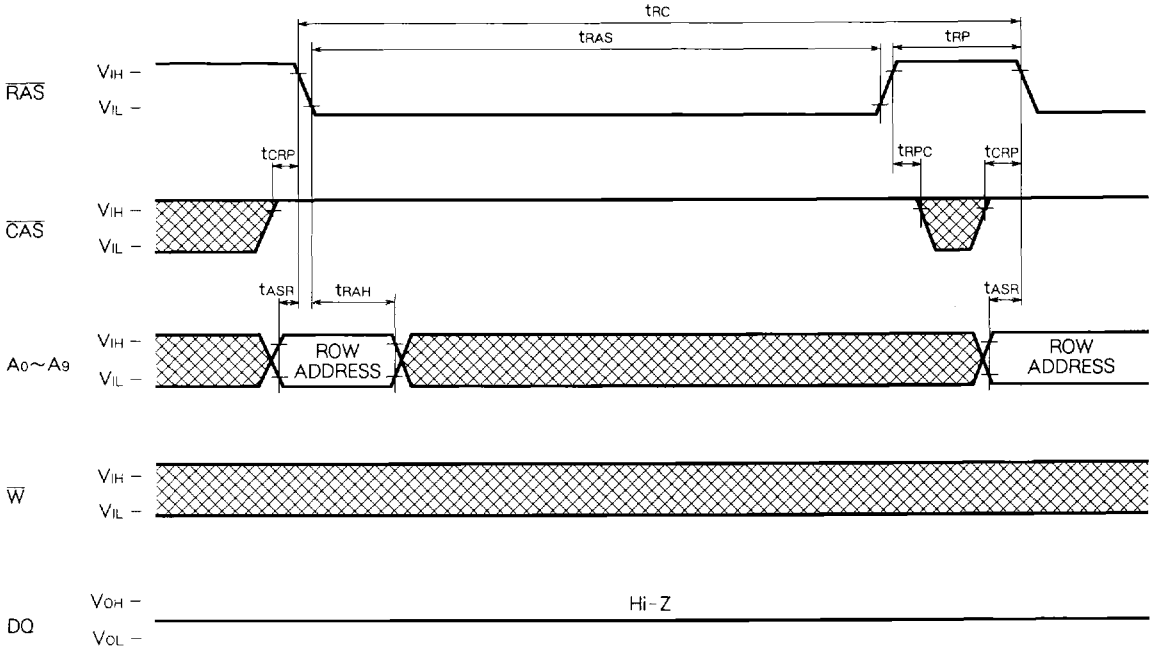
Indicates the don't care input.
VIH (min) ≦ VIN ≦ VIH (max) or VIL (min) ≦ VIN ≦ VIL (max)

Indicates the invalid output.

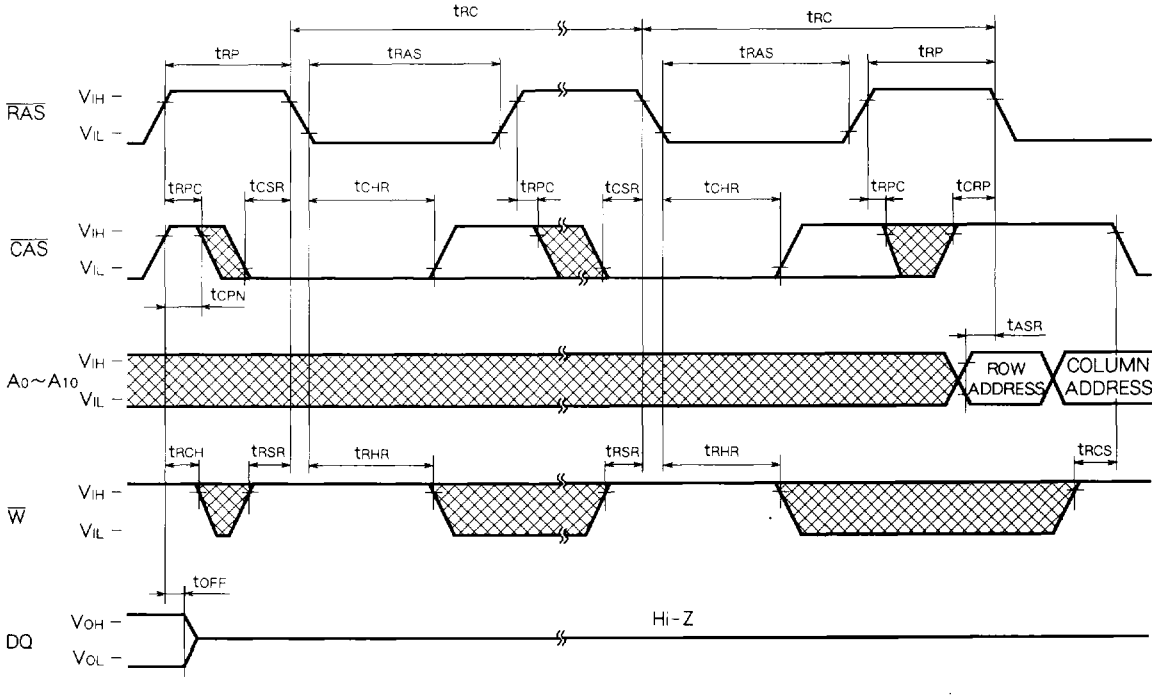
Write Cycle (Early Write)



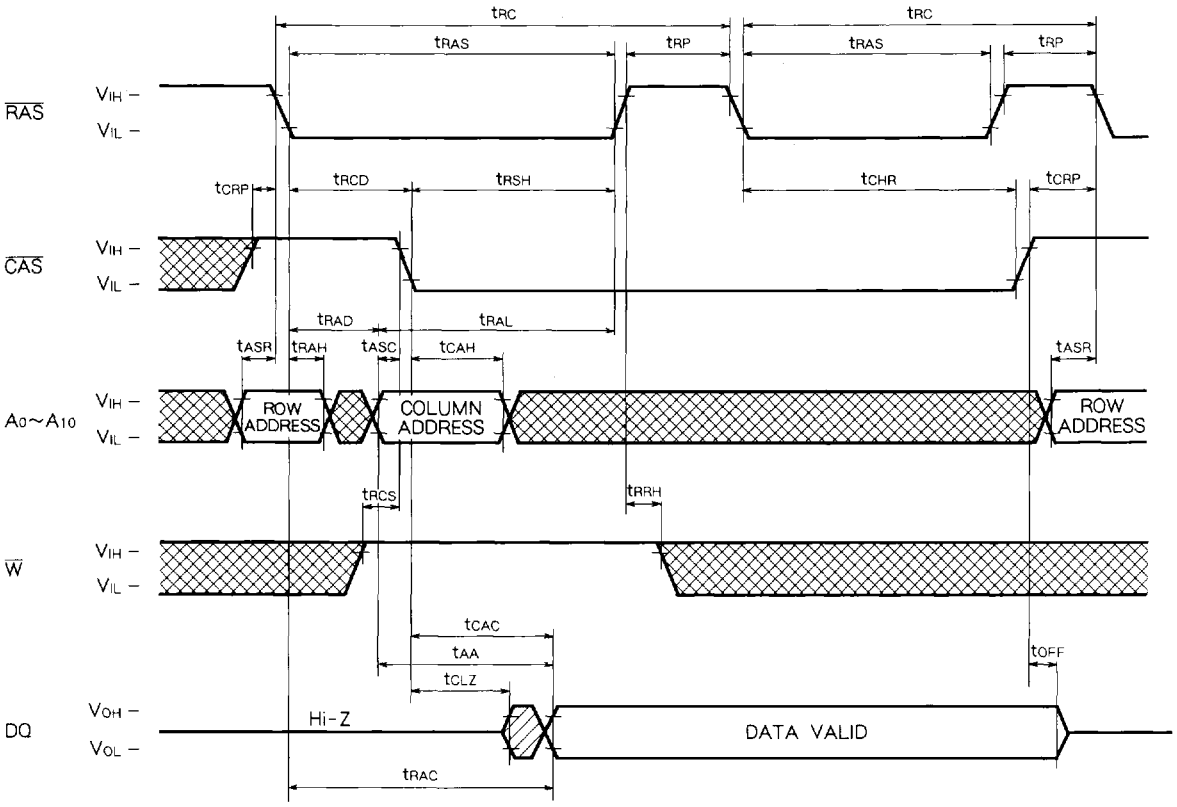
$\overline{RAS}$-only-Refresh Cycle



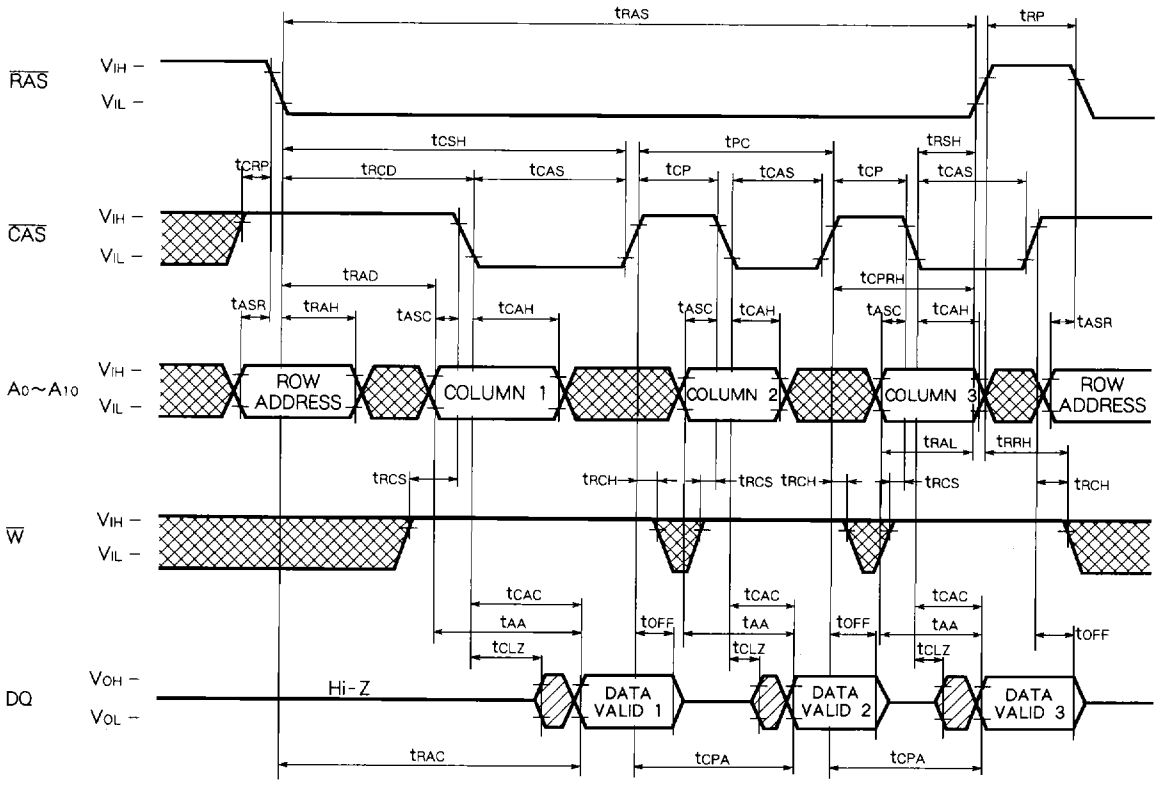
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle (Read)



Fast-Page-Mode Read Cycle



Fast-Page-Mode Write Cycle (Early Write)