IDT77222

155 Mbps ATM SAR Controller With ABR Support for PCI-based Networking Applications

Features

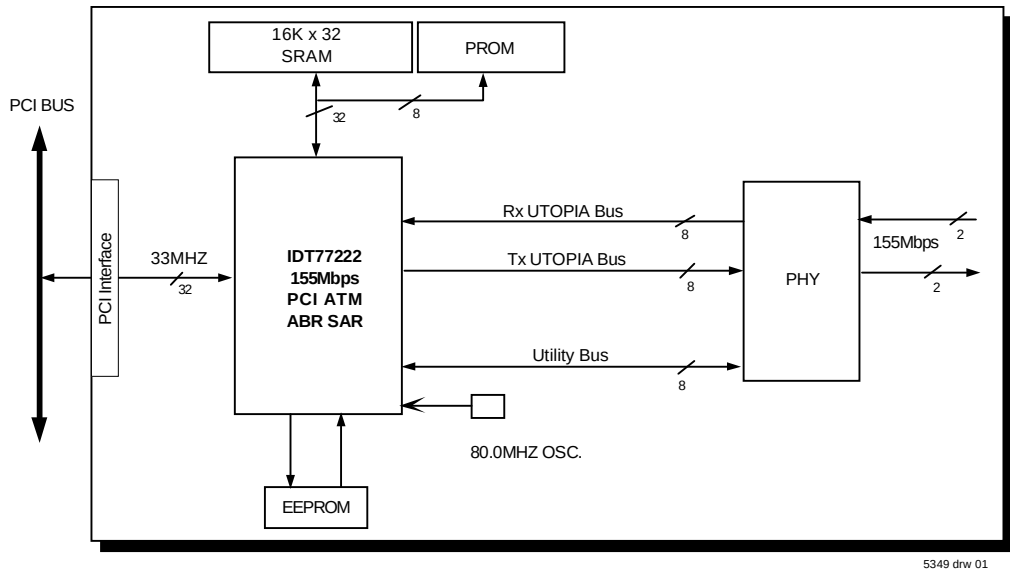
- Full-duplex Segmentation and Reassembly (SAR) at 155 Mbps "wire-speed" (310 Mbps aggregate speed)
- Operates with ATM Networks up to 155.52 Mbps
- Stand-alone Controller: Embedded Processor not required
- Performs ATM Layer Protocol Functions
- Supports AAL5, AAL3/4, AAL0 and Raw Cell Formats
- Supports Constant Bit Rate (CBR), Variable Bit Rate (VBR), and Unassigned Bit Rate (UBR), and Available Bit Rate (ABR) Service Classes
- Segments and Reassembles CS-PDUs into Host Memory
- Up to 256 Active Transmit Connections
- Up to 256 Active Receive Connections
- ABR, VBR, UBR Selectable per VC Time-out
- Automatic AAL5 Padding
- Four Buffer Pools for Independent or Chained Reassembly
- Supports Any Buffer Alignment Condition
- Free Buffer Queues Mapped Into PCI Memory Space
- Rx FIFO Size (Configurable to 1024 Kbytes)
- Configurable Transmit FIFO Depth for Reduced Latency
- Supports Big and Little Endian Data Transfers
- Null Cell Disable Option During Transmit
- NAND Test Mode
- RM Cell Handling
- UTOPIA Level 1 Interface to PHY
- Utility Bus Interface for PHY Management
- Serial EEPROM Interface
- EPROM Interface
- PCI 2.1 Compliant
- UNI 3.1, TM 4.0 Compliant
- Meets PCI Bus Power Management and Interface Specification Revision 1.1
- Pin Compatible with IDT 77211 SAR
- Commercial and Industrial Temperature Ranges
- 208-Lead PQFP Package (28 x 28mm)
- Software Drivers:
  - *SARWIN 2 Demonstration Program*
  - *NDIS Driver*
  - *Vx Works (3rd party)*
  - *Linux (3rd party)*

Description

The IDT77222 is a member of IDT's family of SAR products for Asynchronous Transfer Mode (ATM) networks. The IDT77222 performs both the ATM Adaptation Layer (AAL) Segmentation and Reassembly (SAR) function and the ATM layer protocol functions.

A Network Interface Card (NIC) or internetworking product based on the IDT77222 uses host memory, rather than local memory, to reassemble Convergence Sublayer Protocol Data Units (CS-PDUs) from ATM cell payloads received from the network. When transmitting, as CS-PDUs become ready, they are queued in host memory and segmented

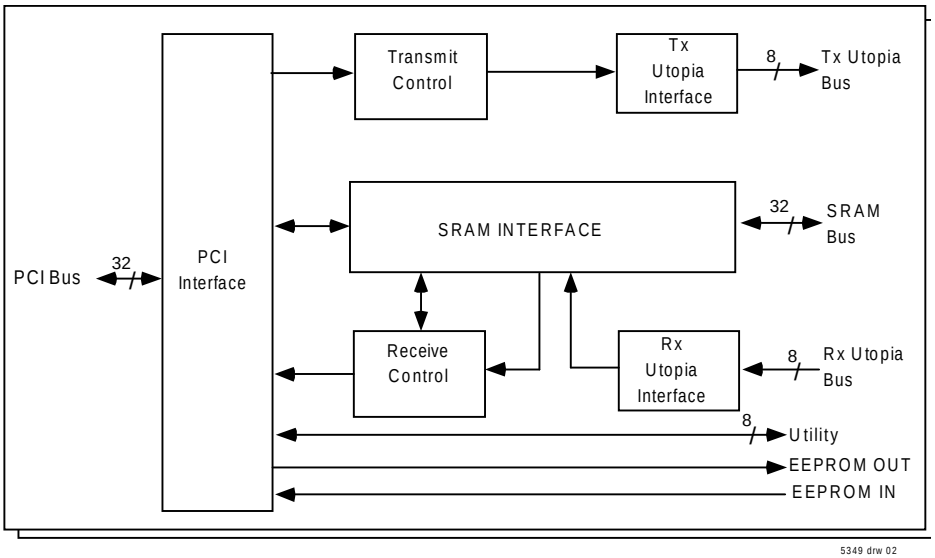
System-Level Functional Block Diagram



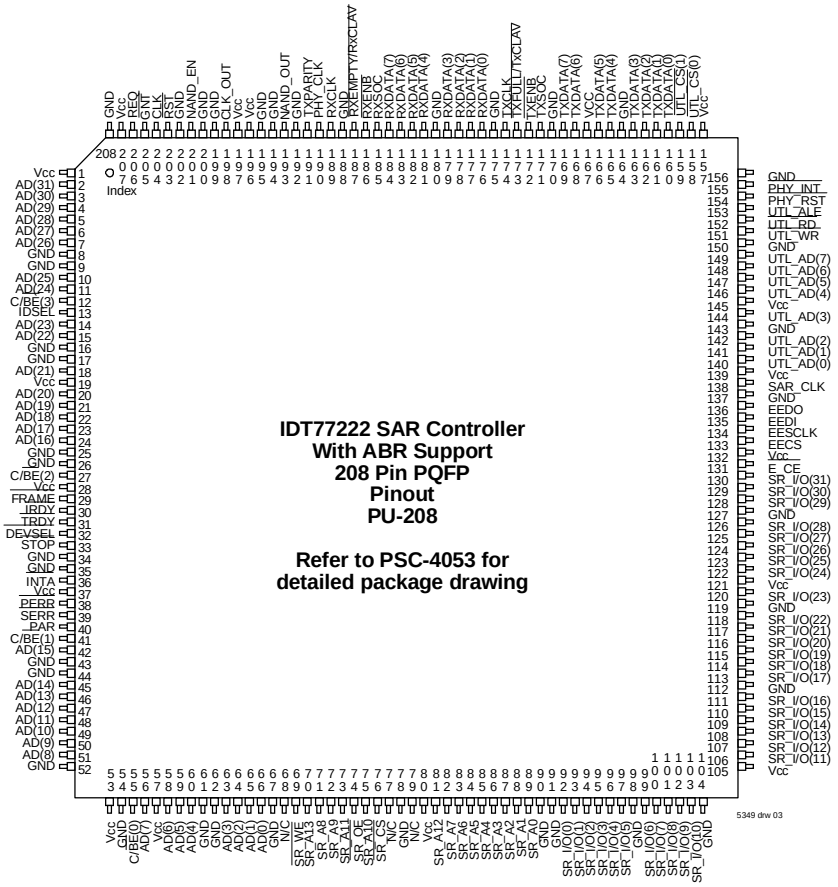
by the IDT77222 into ATM cell payloads. From this, the IDT77222 then creates complete 53-byte ATM cells which are sent through the network. The IDT77222's on-chip PCI bus master interface provides efficient, low latency DMA transfers with the host system, while its UTOPIA interface provides direct connection to PHY components used in 25.6 Mbps to 155 Mbps ATM networks.

The IDT77222 is fabricated using state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

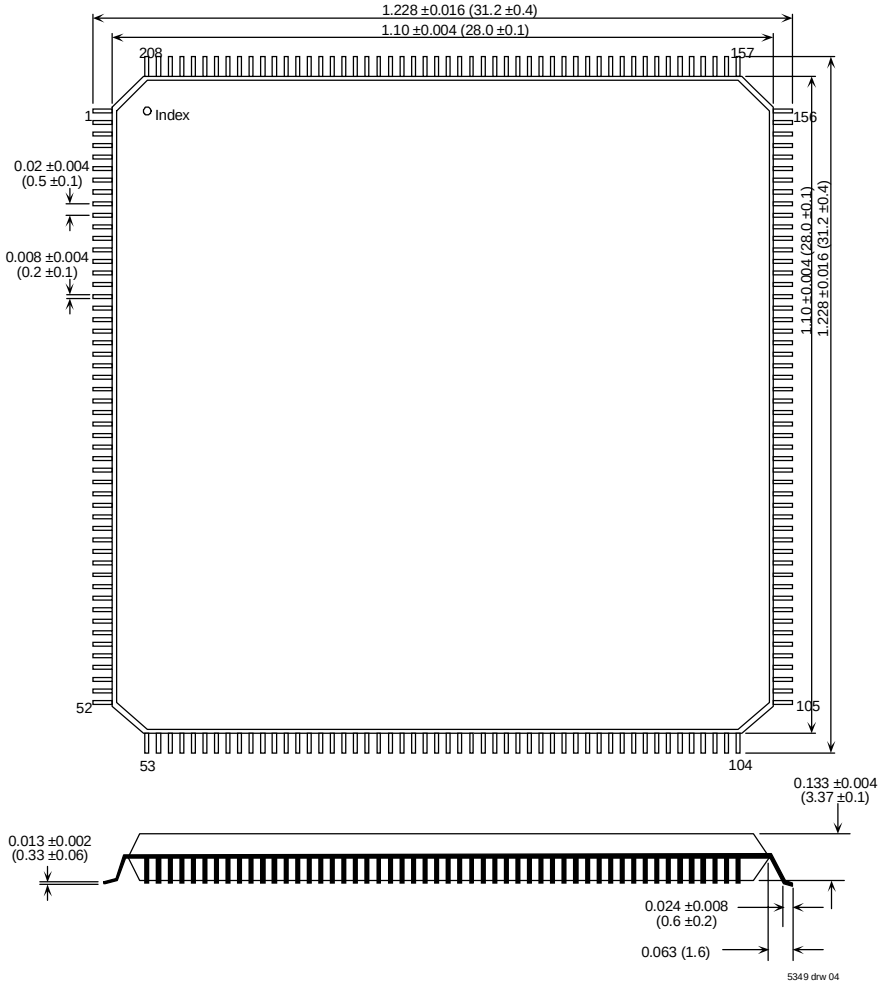
Block Diagram of the IDT77222



Package Pinout



Package Drawing



Pin Definitions

Pin #	Name	I/O	Bus Name	Description
1	Vcc	I	power	
2	AD(31)	I/O	PCI	address/data line
3	AD(30)	I/O	PCI	address/data line
4	AD(29)	I/O	PCI	address/data line
5	AD(28)	I/O	PCI	address/data line
6	AD(27)	I/O	PCI	address/data line
7	AD(26)	I/O	PCI	address/data line
8	GND	I	power	
9	GND	I	power	
10	AD(25)	I/O	PCI	address/data line
11	AD(24)	I/O	PCI	address/data line
12	$\overline{\text{C/BE(3)}}$	I/O	PCI	bus command
13	IDSEL	I	PCI	bus ID select

Pin #	Name	I/O	Bus Name	Description
14	AD(23)	I/O	PCI	address/data line
15	AD(22)	I/O	PCI	address/data line
16	GND	I	power	
17	GND	I	power	
18	AD(21)	I/O	PCI	address/data line
19	Vcc	I	power	
20	AD(20)	I/O	PCI	address/data line
21	AD(19)	I/O	PCI	address/data line
22	AD(18)	I/O	PCI	address/data line
23	AD(17)	I/O	PCI	address/data line
24	AD(16)	I/O	PCI	address/data line
25	GND	I	power	
26	GND	I	power	
27	$\overline{\text{C/BE(2)}}$	I/O	PCI	bus command
28	Vcc	I	power	
29	$\overline{\text{Frame}}$	I/O	PCI	cycle frame
30	$\overline{\text{IRDY}}$	I/O	PCI	initiator ready
31	$\overline{\text{TRDY}}$	I/O	PCI	target ready
32	$\overline{\text{DEVSEL}}$	I/O	PCI	target indicating address decode
33	$\overline{\text{STOP}}$	I/O	PCI	target requesting master to stop
34	GND	I	power	
35	GND	I	power	
36	$\overline{\text{INTA}}$	O	PCI	"interrupt" "A" "request"
37	Vcc	I	power	
38	$\overline{\text{PERR}}$	I/O	PCI	data parity error
39	$\overline{\text{SERR}}$	O	PCI	system error
40	PAR	I/O	PCI	parity (for AD[0:31] and C/BE[0:3])
41	$\overline{\text{C/BE(1)}}$	I/O	PCI	bus command
42	AD(15)	I/O	PCI	address/data line
43	GND	I	power	
44	GND	I	power	
45	AD(14)	I/O	PCI	address/data line
46	AD(13)	I/O	PCI	address/data line
47	AD(12)	I/O	PCI	address/data line
48	AD(11)	I/O	PCI	address/data line
49	AD(10)	I/O	PCI	address/data line
50	AD(9)	I/O	PCI	address/data line
51	AD(8)	I/O	PCI	address/data line
52	GND	I	power	

Pin #	Name	I/O	Bus Name	Description
53	Vcc	I	power	
54	GND	I	power	
55	C/$\overline{BE}$(0)	I/O	PCI	bus command
56	AD(7)	I/O	PCI	address/data line
57	Vcc	I	power	
58	AD(6)	I/O	PCI	address/data line
59	AD(5)	I/O	PCI	address/data line
60	AD(4)	I/O	PCI	address/data line
61	GND	I	power	
62	GND	I	power	
63	AD(3)	I/O	PCI	address/data line
64	AD(2)	I/O	PCI	address/data line
65	AD(1)	I/O	PCI	address/data line
66	AD(0)	I/O	PCI	address/data line
67	GND	I	power	
68	N/C			No connect
69	$\overline{SR\_WE}$	O	SRAM	Write enable
70	SR_A13	O	SRAM	Address line
71	SR_A8	O	SRAM	Address line
72	SR_A9	O	SRAM	Address line
73	SR_A11	O	SRAM	Address line
74	$\overline{SR\_OE}$	O	SRAM	Output Enable control
75	SR_A10	O	SRAM	Address line
76	$\overline{SR\_CS}$	O	SRAM	Chip Select
77	N/C			No connect
78	GND	I	power	
79	N/C			No connect
80	Vcc	I	power	
81	SR_A12	O	SRAM	Address line
82	SR_A7	O	SRAM	Address line
83	SR_A6	O	SRAM	Address line
84	SR_A5	O	SRAM	Address line
85	SR_A4	O	SRAM	Address line
86	SR_A3	O	SRAM	Address line
87	SR_A2	O	SRAM	Address line
88	SR_A1	O	SRAM	Address line
89	SR_A0	O	SRAM	Address line
90	GND	I	power	
91	GND	I	power	

Pin #	Name	I/O	Bus Name	Description
92	SR_I/O(0)	I/O	SRAM	Data input/output line
93	SR_I/O(1)	I/O	SRAM	Data input/output line
94	SR_I/O(2)	I/O	SRAM	Data input/output line
95	SR_I/O(3)	I/O	SRAM	Data input/output line
96	SR_I/O(4)	I/O	SRAM	Data input/output line
97	SR_I/O(5)	I/O	SRAM	Data input/output line
98	GND	I	power	
99	SR_I/O(6)	I/O	SRAM	Data input/output line
100	SR_I/O(7)	I/O	SRAM	Data input/output line
101	SR_I/O(8)	I/O	SRAM	Data input/output line
102	SR_I/O(9)	I/O	SRAM	Data input/output line
103	SR_I/O(10)	I/O	SRAM	Data input/output line
104	GND	I	power	
105	Vcc	I	power	
106	SR_I/O(11)	I/O	SRAM	Data input/output line
107	SR_I/O(12)	I/O	SRAM	Data input/output line
108	SR_I/O(13)	I/O	SRAM	Data input/output line
109	SR_I/O(14)	I/O	SRAM	Data input/output line
110	SR_I/O(15)	I/O	SRAM	Data input/output line
111	SR_I/O(16)	I/O	SRAM	Data input/output line
112	GND	I	power	
113	SR_I/O(17)	I/O	SRAM	Data input/output line
114	SR_I/O(18)	I/O	SRAM	Data input/output line
115	SR_I/O(19)	I/O	SRAM	Data input/output line
116	SR_I/O(20)	I/O	SRAM	Data input/output line
117	SR_I/O(21)	I/O	SRAM	Data input/output line
118	SR_I/O(22)	I/O	SRAM	Data input/output line
119	GND	I	power	
120	SR_I/O(23)	I/O	SRAM	Data input/output line
121	Vcc	I	power	
122	SR_I/O(24)	I/O	SRAM	Data input/output line
123	SR_I/O(25)	I/O	SRAM	Data input/output line
124	SR_I/O(26)	I/O	SRAM	Data input/output line
125	SR_I/O(27)	I/O	SRAM	Data input/output line
126	SR_I/O(28)	I/O	SRAM	Data input/output line
127	GND	I	power	
128	SR_I/O(29)	I/O	SRAM	Data input/output line
129	SR_I/O(30)	I/O	SRAM	Data input/output line
130	SR_1/O(31)	I/O	SRAM	Data input/output line

Pin #	Name	I/O	Bus Name	Description
131	$\overline{E\_CE}$	O	EPROM	EPROM chip select
132	Vcc	I	power	
133	EECS	O	EEPROM	chip select
134	EESCLK	O	EEPROM	clock
135	EEDI	I	EEPROM	Data input
136	EEDO	O	EEPROM	Data output
137	GND	I	power	
138	SAR_CLK	I		SAR clock input
139	Vcc	I	power	
140	UTL_AD(0)	I/O	Utility	address/data bus
141	UTL_AD(1)	I/O	Utility	address/data bus
142	UTL_AD(2)	I/O	Utility	address/data bus
143	GND	I	power	
144	UTL_AD(3)	I/O	Utility	address/data bus
145	Vcc	I	power	
146	UTL_AD(4)	I/O	Utility	address/data bus
147	UTL_AD(5)	I/O	Utility	address/data bus
148	UTL_AD(6)	I/O	Utility	address/data bus
149	UTL_AD(7)	I/O	Utility	address/data bus
150	GND	I	power	
151	$\overline{UTL\_WR}$	O	Utility	write control
152	$\overline{UTL\_RD}$	O	Utility	read control
153	UTL_ALE	O	Utility	address latch enable
154	$\overline{PHY\_RST}$	O	PHY	rest control
155	$\overline{PHY\_INT}$	I	PHY	interrupt input from PHY
156	GND	I	power	
157	VCC	I	power	
158	$\overline{UTL\_CS(0)}$	O	Utility	chip select (0)
159	$\overline{UTL\_CS(1)}$	O	Utility	chip select (1)
160	TxData(0)	O	UTOPIA	transmit data bit 0
161	TxData(1)	O	UTOPIA	transmit data bit 1
162	TxData(2)	O	UTOPIA	transmit data bit 2
163	TxData(3)	O	UTOPIA	transmit data bit 3
164	GND	I	power	
165	TxData(4)	O	UTOPIA	transmit data bit 4
166	TxData(5)	O	UTOPIA	transmit data bit 5
167	Vcc	I	power	
168	TxData(6)	O	UTOPIA	transmit data bit 6
169	TxData(7)	O	UTOPIA	transmit data bit 7

Pin #	Name	I/O	Bus Name	Description
170	GND	I	power	
171	TxSOC	O	UTOPIA	transmit start of cell
172	$\overline{\text{TxEnb}}$	O	UTOPIA	transmit enable control
173	$\overline{\text{TxFull}}$/TxCLAV	I	UTOPIA	transmit buffer full
174	TxCLK	O	UTOPIA	transmit data sync clock
175	GND	I	power	
176	RxData(0)	I	UTOPIA	receive data bit 0
177	RxData(1)	I	UTOPIA	receive data bit 1
178	RxData(2)	I	UTOPIA	receive data bit 2
179	RxData(3)	I	UTOPIA	receive data bit 3
180	GND	I	power	
181	RxData(4)	I	UTOPIA	receive data bit 4
182	RxData(5)	I	UTOPIA	receive data bit 5
183	RxData(6)	I	UTOPIA	receive data bit 6
184	RxData(7)	I	UTOPIA	receive data bit 7
185	RxSOC	I	UTOPIA	receive start of cell
186	$\overline{\text{RxEnb}}$	O	UTOPIA	receive enable control
187	$\overline{\text{RxEmpty}}$/RxCLAV	I	UTOPIA	receive buffer empty
188	GND	I	power	
189	RxClk	O	UTOPIA	receive data sync clock
190	PHY_Clk	I	UTOPIA	Transmit sync clock input
191	TxParity	O	UTOPIA	transmit data parity bit
192	GND	I	power	
193	NAND_OUT	O	power	NAND output chain
194	GND	I	power	
195	GND	I	power	
196	Vcc	I	power	
197	Vcc	I	power	
198	CLK_OUT	O	power	SAR_Clk divided by 3
199	GND	I	power	
200	GND	I	power	
201	NAND_EN	I	power	NAND input chain
202	GND	I	power	
203	$\overline{\text{RST}}$	I	PCI	system bus reset
204	CLK	I	PCI	bus clock
205	$\overline{\text{GNT}}$	I	PCI	bus grant signal from arbiter
206	$\overline{\text{REQ}}$	O	PCI	bus request
207	Vcc	I	power	
208	GND	I	power	

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	6.5	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{CC} + 0.3	V
V_{OUT}	Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	V
Tstg	Storage Temperature	-55	125	deg.C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_I	Input Voltage	0	V_{CC}	V
T_A	Operating temperature	0	70	deg.C
titr	Input TTL rise time	—	2	ns
titf	Input TTL fall time	—	2	ns

Clocking

Symbol	Parameter	Rate	Min	Max	Unit
SAR_CLK	SAR clock input freq.	155Mb/s	77	80	MHz
		25Mb/s	25	80	MHz
PHY_CLK	PHY clock input freq.	155Mb/s	19.44	40	MHz
		25Mb/s	3	40	MHz
PCI_CLK	PCI clock input freq.	33MHz	0	33.3	MHz

Capacitance

Symbol	Parameter	Condition	Min	Max	Typical	Unit
C_{IN}	Input Capacitance	except PCI Bus	—	—	4	pF
C_{OUT}	Output Capacitance	all outputs	—	—	6	pF
Cbid	Bi-Directional Capacitance	all bi-directional pins	—	—	10	pF
Cinpci	PCI Bus Input Capacitance	PCI Bus inputs	—	10	—	pF
Cclkpci	PCI Bus Clock Input Capacitance	—	5	12	—	pF
Cidsel	PCI Bus ID Select Input Capacitance	—	—	8	—	pF

DC Operating Conditions

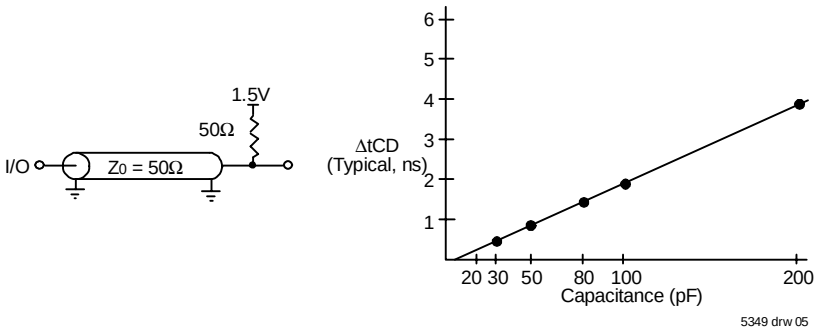
Symbol	Parameter	Condition	Min	Max	Typical	Unit
Vil	Low-level TTL input voltage	—	-0.7V	0.8	—	V
Vih	High-level TTL input voltage	—	2	V_{CC} + 0.2V	—	V
Vol	Low-level TTL output voltage	except PCI Bus	—	0.4	—	V
Vol	PCI Bus Low-level TTL output voltage	PCI Bus voltage	—	0.55	—	V
Voh	High-level TTL output voltage	—	2.4	—	—	V
Iol	Low-level TTL output current: SR_A(18-0)	VSS + 0.4V	12	—	—	mA

Symbol	Parameter	Condition	Min	Max	Typical	Unit
Ioh	High-level TTL output current: SR_A(18-0)	2.4V	-4	—	—	mA
Iol	Low-level TTL output current: RxEnb, RxClk, TxSOC, TxData (7-0), TxEnb, TxParity, TxClk, WE, OE, CS, SR_D31-0	Vss + 0.4V	6	—	—	mA
Ioh	High-level TTL output current: RxEnb, RxClk, TxSoc, TxData7-0, TxEnb, TxParity, TxClk, SR_WE, SR, OE, SR_CS, SR_I/O(31-0)	2.4V	-2	—	—	mA
Iol	Low-level TTL output current: UTL_AD(7-0), UTL_RD, UTL_WR, UTL_ALE, UTL_CS0/1, EESCLK, EECS, EEDO, PHY_RST	Vss + 0.4V	3	—	—	mA
Ioh	High-level TTL output current: UTL_AD(7-0), UTL_RD, UTL_WR, UTL_ALE, UTL_CS0/1, EESCLK, EECS, EEDO, PHY_RST	2.4V	-1	—	—	mA
Iil	Input leakage current	Vss ≤ VIN ≤ Vdd	-1	1	—	uA
Ityp	Dynamic Supply Current	—	—	300	250	mA

AC Operating Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Ref. Level	1.5V
Output Ref. Level	1.5V
AC Test Load	See Figure Below

Table 1 AC Test Conditions



NAND Tree

The NAND Chain provides a simple test to verify that all bond wires are installed correctly and that all pads are correctly soldered on a PCB.

All signal pads are linked in a NAND chain, which is enabled by asserting a high, or “1”, on NAND_EN (pin 201). Asserting a “1” on the other inputs forces NAND_OUT (pin 193) to “1”. By successively setting the inputs to “0”, starting at CLK_OUT (pin 198) and moving to TXPARITY (pin 191), NAND_OUT will toggle with each change.

1. Apply a "1" to NAND_EN.
2. Set all the I/O's in the chain to "0" and NAND_OUT should be a "1". The connection order of the pins in the chain are shown in the NAND Tree Pin Order table located on the following page.
3. Set CLK_OUT to a "0" and the NAND_OUT should be a "0".
4. Leaving pin 198 at a "1" set RST (pin 203) to "1" and NAND_OUT should be a "1".
5. Repeat for all remaining I/O's in the NAND chain.

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
CLK_OUT	198	AD[12]	47	SR_I/O[06]	99	UTL_AD[5]	147
$\overline{RST}$	203	AD[11]	48	SR_I/O[07]	100	UTL_AD[6]	148
CLK	204	AD[10]	49	SR_I/O[08]	101	UTL_AD[7]	149
$\overline{GNT}$	205	AD[9]	50	SR_I/O[09]	102	$\overline{UTL\_WR}$	151
$\overline{REQ}$	206	AD[8]	51	SR_I/O[10]	103	$\overline{UTL\_RD}$	152
AD[31]	2	C/$\overline{BE}$[0]	55	SR_I/O[11]	106	UTL_ALE	153
AD[30]	3	AD[7]	56	SR_I/O[12]	107	$\overline{PHY\_RST}$	154
AD[29]	4	AD[6]	58	SR_I/O[13]	108	$\overline{PHY\_INT}$	155
AD[28]	5	AD[5]	59	SR_I/O[14]	109	$\overline{UTL\_CS[0]}$	158
AD[27]	6	AD[4]	60	SR_I/O[15]	110	$\overline{UTL\_CS[1]}$	159
AD[26]	7	AD[3]	63	SR_I/O[16]	111	TxData[0]	160
AD[25]	10	AD[2]	64	SR_I/O[17]	113	TxData[1]	161
AD[24]	11	AD[1]	65	SR_I/O[18]	114	TxData[2]	162
C/$\overline{BE}$[3]	12	AD[0]	66	SR_I/O[19]	115	TxData[3]	163
$\overline{IDSEL}$	13	$\overline{SR\_WE}$	69	SR_I/O[20]	116	TxData[4]	165
AD[23]	14	SR_A[13]	70	SR_I/O[21]	117	TxData[5]	166
AD[22]	15	SR_A[8]	71	SR_I/O[22]	118	TxData[6]	168
AD[21]	18	SR_A[9]	72	SR_I/O[23]	120	TxData[7]	169
AD[20]	20	SR_A[11]	73	SR_I/O[24]	122	TxSOC	171
AD[19]	21	SR_OE	74	SR_I/O[25]	123	$\overline{TxEnb}$	172
AD[18]	22	SR_A[10]	75	SR_I/O[26]	124	TxCLAV	173
AD[17]	23	$\overline{SR\_CS}$	76	SR_I/O[27]	125	TxCLK	174
AD[16]	24	SR_A[12]	81	SR_I/O[28]	126	RxData[0]	176
C/$\overline{BE}$[2]	27	SR_A[7]	82	SR_I/O[29]	128	RxData[1]	177
$\overline{Frame}$	29	SR_A[6]	83	SR_I/O[30]	129	RxData[2]	178
$\overline{IRDY}$	30	SR_A[5]	84	SR_I/O[31]	130	RxData[3]	179
$\overline{TRDY}$	31	SR_A[4]	85	$\overline{E\_CE}$	131	RxData[4]	181
$\overline{DEVSEL}$	32	SR_A[3]	86	EECS	133	RxData[5]	182
$\overline{STOP}$	33	SR_A[2]	87	EESCLK	134	RxData[6]	183
$\overline{INITA}$	36	SR_A[1]	88	EEDI	135	RxData[7]	184
$\overline{PERR}$	38	SR_A[0]	89	EEDO	136	RxSOC	185
$\overline{SERR}$	39	SR_I/O[00]	92	SAR_CLK	138	$\overline{RxEnb}$	186
PAR	40	SR_I/O[01]	93	UTL_AD[0]	140	RxCLAV	187
C/$\overline{BE}$[1]	41	SR_I/O[02]	94	UTL_AD[1]	141	RxCLK	189
AD[15]	42	SR_I/O[03]	95	UTL_AD[2]	142	PHY_CLK	190
AD[14]	45	SR_I/O[04]	96	UTL_AD[3]	144	TxParity	191
AD[13]	46	SR_I/O[05]	97	UTL_AD[4]	146		

Table 2 NAND Tree Pin Order

PCI Bus (See Figure 1 and 2)

Symbol	Parameter	Min	Max	Unit
tval	CLK to Output Signal Valid Delay: AD31-0, C/BE3-0, PAR, FRAME, IRDY, DEVSEL, TRDY, STOP, PERR, SERR	2	11	ns
tval(ptp)	CLK to Output Signal Valid Delay: REQ	2	12	ns
ton	Float to Signal Active Delay: AD31-0, C/BE3-0, PAR, FRAME, IRDY, DEVSEL, TRDY, STOP, PERR, SERR	2	—	ns
toff	Signal Active to Float Delay: AD31-0, C/BE3-0, PAR, FRAME, IRDY, DEVSEL, TRDY, STOP, PERR, SERR	—	28	ns
tsu	Input Setup Time to CLK: AD31-0, C/BE3-0, PAR, FRAME, IRDY, DEVSEL, TRDY, STOP, PERR	7	—	ns
tsu(ptp)	Input Setup Time to CLK: GNT, (REQ)	10(12)	—	ns
th	Input Hold Time from CLK: AD31-0, C/BE3-0, PAR, FRAME, IRDY, DEVSEL, TRDY, STOP, PERR, GNT	2[1]	—	ns
trst-pwr	Reset Active Time After Power Stable	1	—	ns
trst-clk	Reset Active Time After CLK Stable	100	—	ns
trst-off	Reset Active to Output Float Delay: AD31-0, C/BE3-0, PAR, FRAME, IRDY, DEVSEL, TRDY, STOP, PERR, SERR	—	40	ns
thigh	Clock high time	11n	—	ns
tlow	Clock low time	11n	—	ns

1. Does not meet PCI Local Bus revision 2.1 timing specification

UTOPIA Bus (See Figure 3)

Symbol	Parameter	Min	Max	Unit
t1	TxClk, RxClk Delay from PHY_CLK	—	5	ns
t2	TxData(7-0), TxSOC, TxEnb, TxParity Output Valid from TxClk	1	15	ns
t3	TxFull/TxCLAV Setup Time to TxClk	10	—	ns
t4	TxFull/TxCLAV Hold Time from TxClk	3[1]	—	ns
t5	RxEnb Output Valid from RxClk	1	15	ns
t6	RxData(7-0), RxSOC Setup Time to RxClk	10	—	ns
t7	RxData(7-0), RxSOC Hold Time from RxClk	2[1]	—	ns
t8	RxEmpty/RxCLAV Setup Time to RxClk	10	—	ns
t9	RxEmpty/RxCLAV Hold Time from TxClk	2[1]	—	ns

1. Does not meet UTOPIA 1 timing specification (Af-phy-0017.00)

Utility Bus Write Cycle (See Figure 4)

Symbol	Parameter	Min	Max	Unit
tw1	UTL_ALE Pulse Width	25	—	ns
tw2	UTL_CS0/1 Output Valid to UTL_ALE falling edge	25	—	ns
tw3	UTL_WR Output Valid from UTL_ALE falling edge	—	80	ns
tw4	UTL_CS0/1 Pulse Width	275	—	ns
tw5	UTL_WR Pulse Width	175	—	ns
tw6	UTL_ALE falling edge to UTL_WR rising edge	225	—	ns
tw7	UTL_AD(7-0) Address Setup Time to UTL_ALE falling edge	30	—	ns
tw8	UTL_AD(7-0) Address Hold Time from UTL_ALE falling edge	10	—	ns
tw9	UTL_AD(7-0) Data Setup Time to UTL_WR rising edge	185	—	ns
tw10	UTL_AD(7-0) Data Hold Time from UTL_WR rising edge	10	—	ns
tw11	UTL_ALE falling edge to UTL_CS0/1 rising edge	250	—	ns

Utility Bus Read Cycle (See Figure 5)

Symbol	Parameter	Min	Max	Unit
tr1	UTL_ALE Pulse Width	25	—	ns
tr2	$\overline{\text{UTL\_CS0/1}}$ Output Valid to UTL_ALE falling edge	25	—	ns
tr3	$\overline{\text{UTL\_RD}}$ Output Valid from UTL_ALE falling edge	—	80	ns
tr4	$\overline{\text{UTL\_CS0/1}}$ Pulse Width	250	—	ns
tr5	$\overline{\text{UTL\_RD}}$ Pulse Width	185	—	ns
tr6	UTL_ALE falling edge to $\overline{\text{UTL\_RD}}$ rising edge	250	—	ns
tr7	UTL_AD(7-0) Address Setup Time to UTL_ALE falling edge	30	—	ns
tr8	UTL_AD(7-0) Address Hold Time from UTL_ALE falling edge	10	—	ns
tr9	UTL_AD(7-0) Data Setup Time to $\overline{\text{UTL\_CS0/1}}$ rising edge	80	—	ns
tr10	UTL_AD(7-0) Data Hold Time from $\overline{\text{UTL\_CS0/1}}$ rising edge	10	—	ns
tr11	UTL_ALE falling edge to $\overline{\text{UTL\_CS0/1}}$ rising edge	225	—	ns

SRAM Bus Write Cycle (See Figure 6)

Symbol	Parameter	Min	Max	Unit
t1	SR_A(18-0) Setup Time to $\overline{\text{SR\_WE}}$ falling edge	2	—	ns
t2	$\overline{\text{SR\_CS}}$ falling edge to $\overline{\text{SR\_WE}}$ falling edge	0	—	ns
t3	$\overline{\text{SR\_CS}}$ pulse width	25	—	ns
t4	SR_I/O(31-0) Setup Time to $\overline{\text{SR\_WE}}$ rising edge	6	—	ns
t5	SR_I/O(31-0) Hold Time from $\overline{\text{SR\_WE}}$ rising edge	0	—	ns
t6	$\overline{\text{SR\_WE}}$ Pulse Width	10	—	ns

SRAM Bus Read Cycle (See Figure 7)

Symbol	Parameter	Min	Max	Unit
t1	SR_A(18-0) to SR_I/O(31-0) Valid[1]	—	15	ns
t2	$\overline{\text{SR\_OE}}$ pulse width	25	—	ns

1. SR_I/O (31-0) Setup and Hold times are guaranteed by design when t1 access time is met.

EPROM (See Figure 8)

Symbol	Parameter	Min	Max	Unit
t1	SR_I/O(7-0) Hold Time from $\overline{\text{E\_CE}}$ rising edge	0	—	ns
t2	$\overline{\text{E\_CE}}$ Pulse Width	75	—	ns
t3	SR_A(18-0) Change to SR_I/O(7-0) Valid	—	70	ns
t4	SR_A(18-0) Pulse Width	75	—	ns

EPROM (See Figure 9)

Symbol	Parameter	Min	Max	Unit	Comments
t1	SAR_CLK to Output Signal Valid Delay: EECS, EEDO, EECLK	100	—	ns	software controlled
t2	EEDI Input Setup Time to SAR_CLK	10	—	ns	software controlled
t3	EEDI Input Hold Time from SAR_CLK	0	—	ns	software controlled

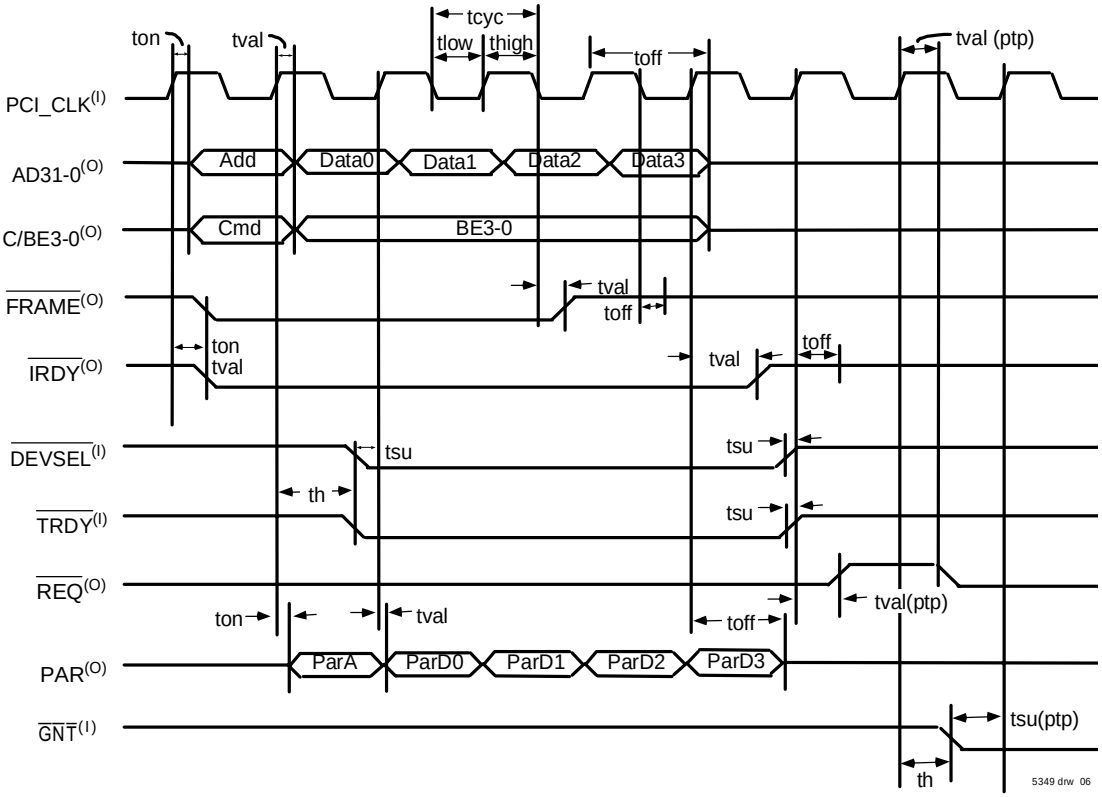


Figure 1 The IDT77222 as a PCI Master (illustrates a 4-word write operation by the IIDT77222 to host memory)

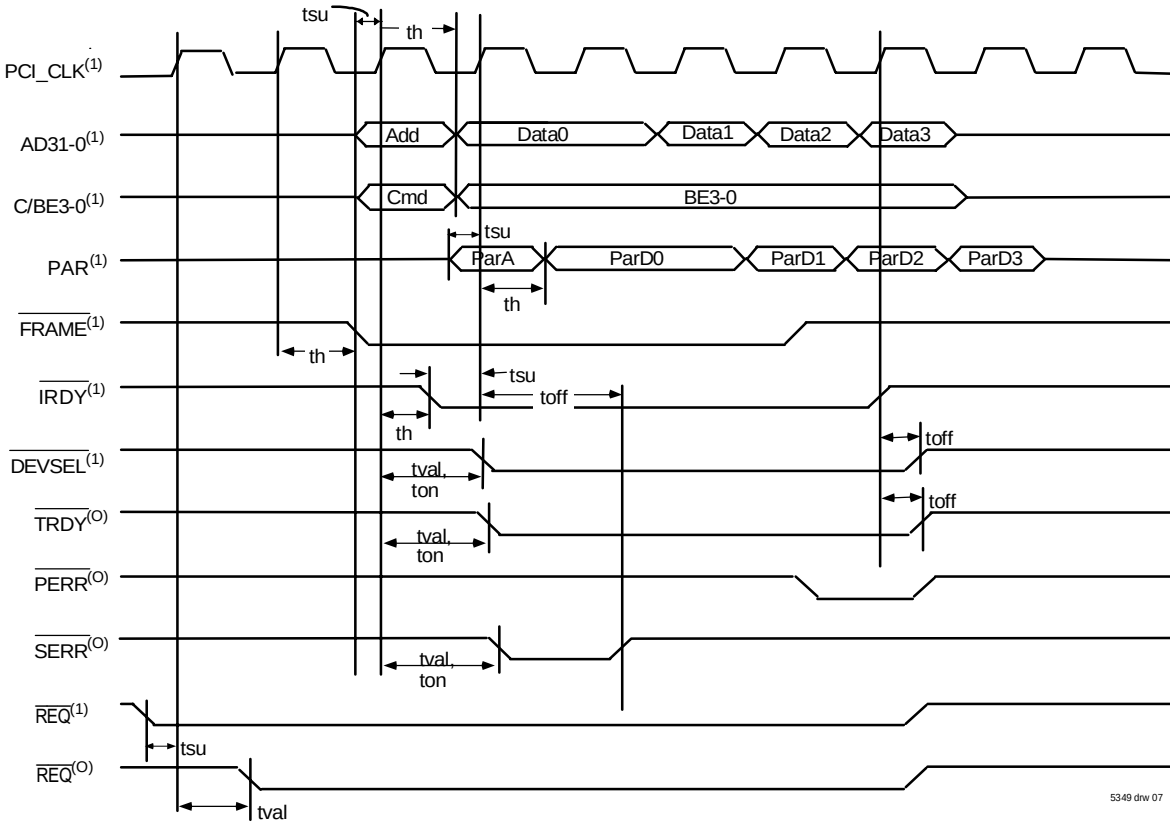


Figure 2 The IDT77222 as a PCI Target (illustrates a 4-word write operation by the host device driver to the IDT77222)

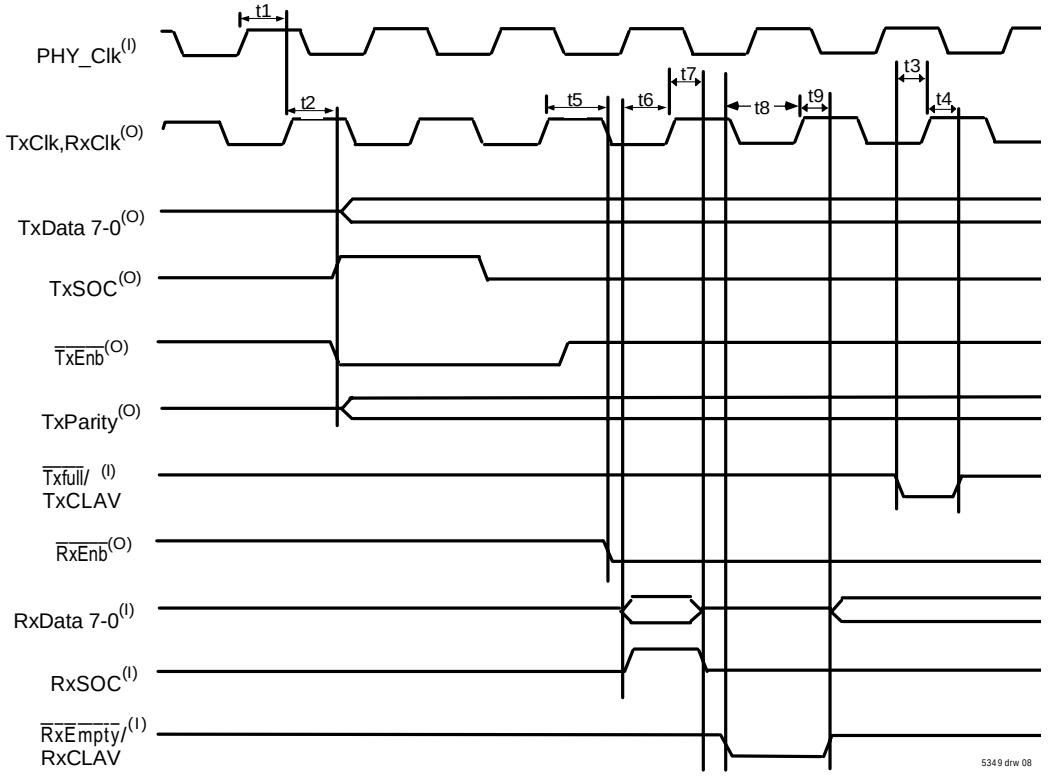


Figure 3 UTOPIA Bus Timing

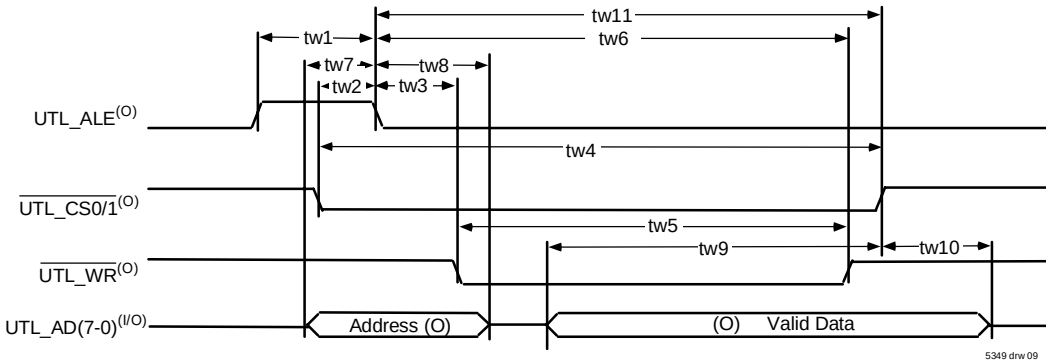


Figure 4 Utility Bus Write Cycle

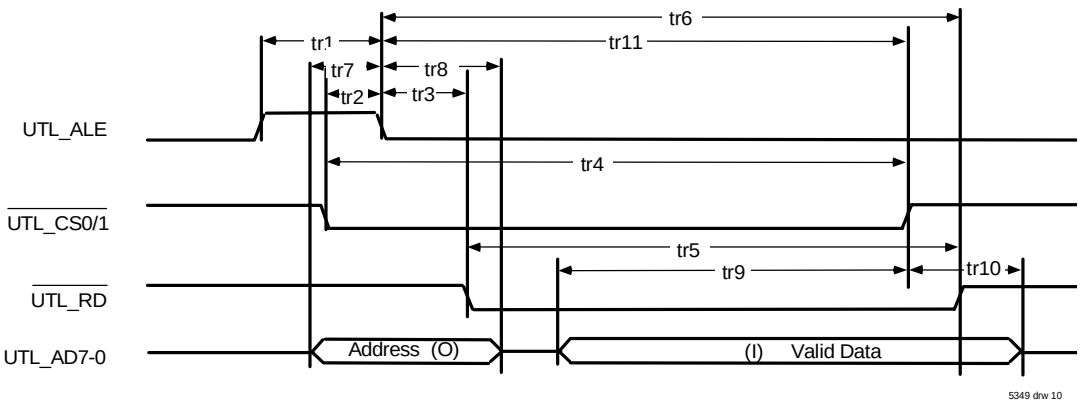


Figure 5 Utility Bus Read Cycle

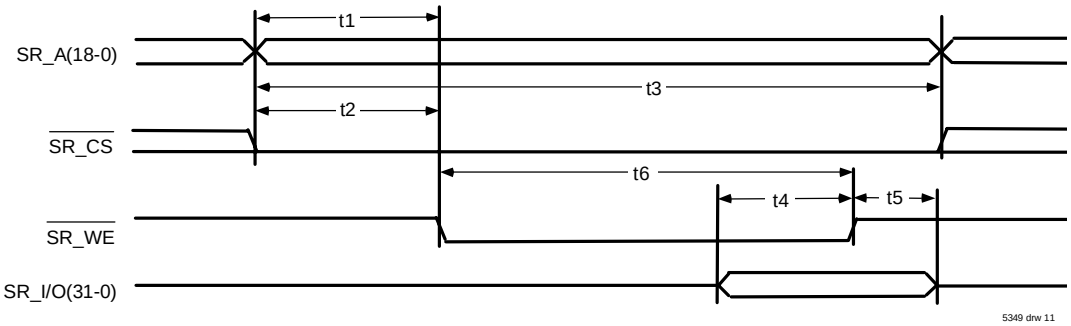


Figure 6 SRAM Bus Write Cycle Timing

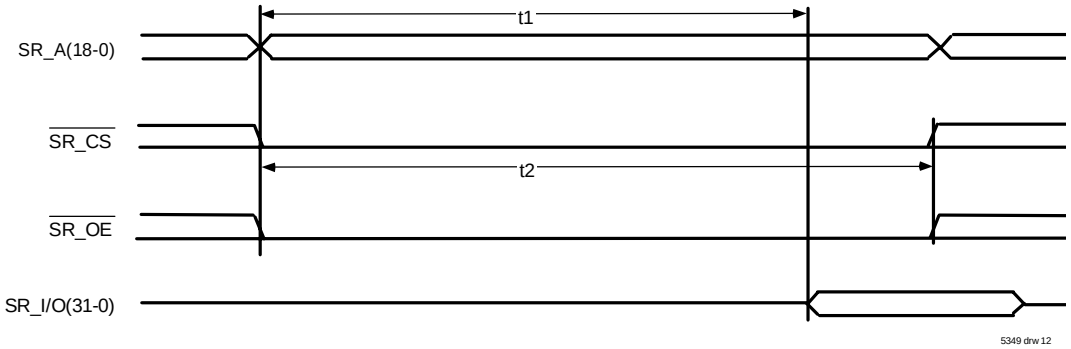


Figure 7 SRAM Bus Read Cycle Timing

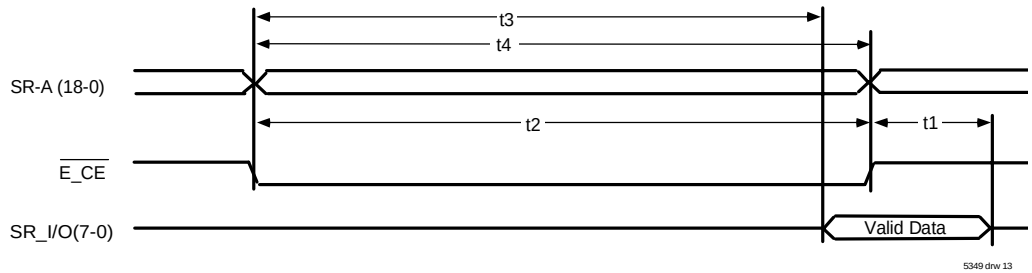


Figure 8 EPROM Timing

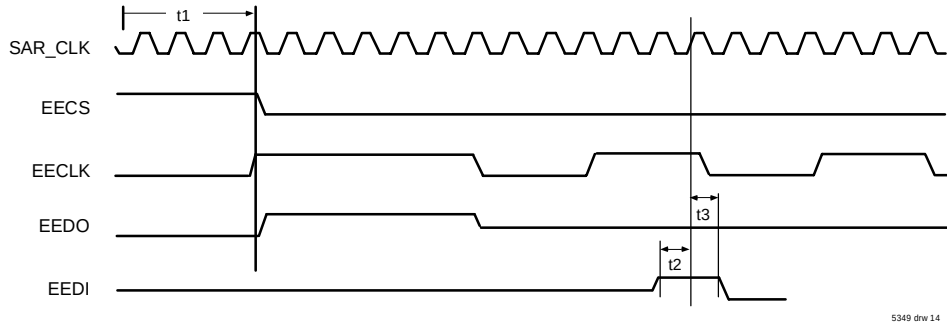


Figure 9 EEPROM Timing

Software and Software Drivers

Several software vendors have written IDT77222 software drivers for various operating systems. Please contact your local IDT sales representative for a vendor list, or send an e-mail to sarhelp@idt.com.

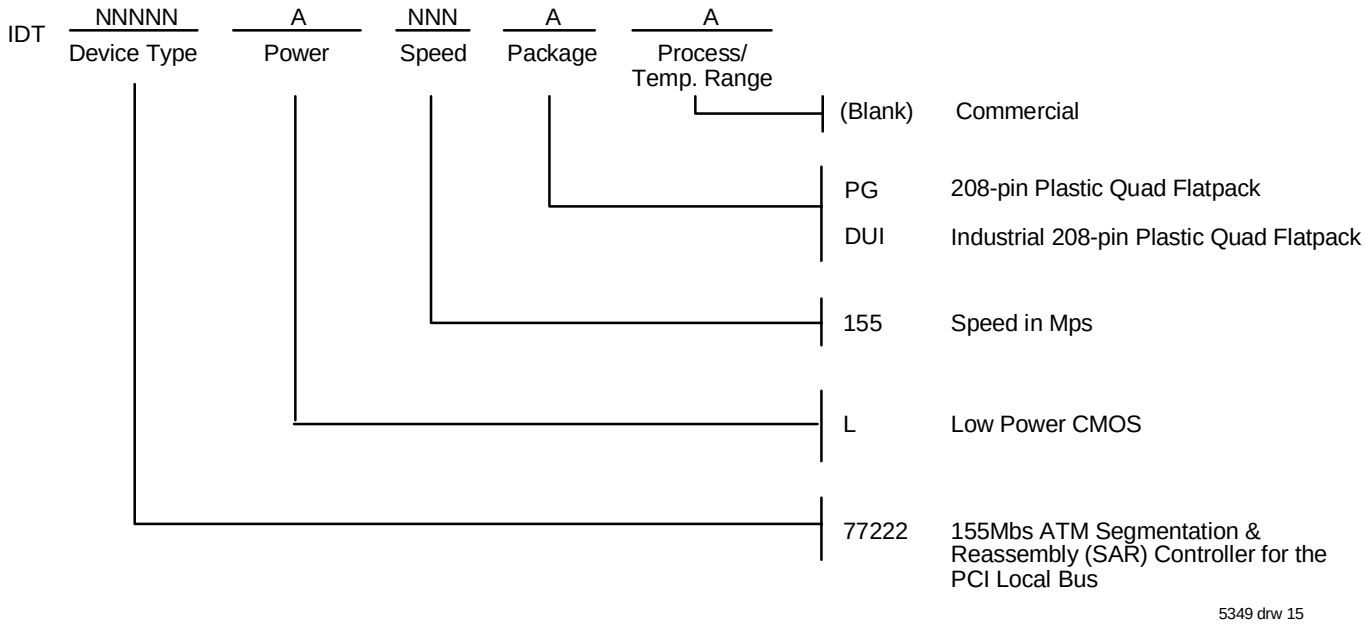
IDT offers the Sarwin2 demo driver and application suite, which can be used to evaluate the IDT77222 when used with a IDT NIC reference or evaluation adapter. It may also be used as a reference for sample source code when developing a proprietary device driver. Pleas e contact your IDT sales representative or send an e-mail to sarhelp@idt.com to obtain a free CD-ROM.

NIC Reference and Evaluation Adapters

NIC Reference and Evaluation adapters are available in several form factors. Bill of Materials (BOM) and schematics are availabl e upon request for each of the NIC adapters. A list of current NIC adapter offerings can be found at www.idt.com.

Note: The Micro ABR SAR User Manual provides a detailed description of the 77222 operation and registers.

Ordering Information



Note: Refer to PSC-4053 for detailed package drawing.
Refer to errata list for revision history and how to identify revision.

Replacing the 77211 with the 77222

The 77222 PG package is the same package as the 77211 PQF . The 77222 is a direct replacement to the 77211 SAR. To use the 77222 in a 155 Mbps application, a 80 MHz oscillator is required (replace the 50 MHz oscillator used with the 77211).

Data Sheet Document History

6/24/98: Created new document.

9/15/99: Updated software section.

6/22/00: Added PG-208 to package pinout and added PSC-4053 reference. Removed Industrial temp rating. Changed pin name for pin 198. Updated SRAM, Utility Bus, UTOPIA Bus, EEPROM and PCI timing parameters and diagrams. Updated AC test Conditions section. Added information for NAND Tree. Changed from Advanced to Preliminary data sheet.

03/26/01: Changed from Preliminary to Final data sheet. Added to and rearranged the Features list.

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