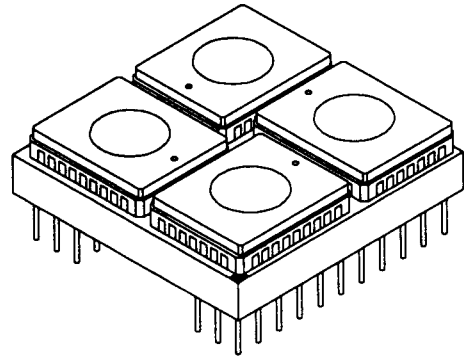


### DESCRIPTION:

The DPV3232V is a 66-pin Pin Grid Array (PGA) consisting of four 32K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

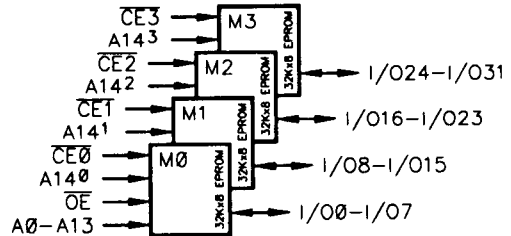


### FEATURES:

- Organizations Available:  
128K X 8, 64K X 16 or 32K X 32
- Access Times:  
55\*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

\* Commercial only.

### FUNCTIONAL BLOCK DIAGRAM



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### PIN NAMES

A0-A13, A14 <sup>0</sup> -A14 <sup>3</sup>	Address Inputs
I/O0 - I/O31	Data In/Out
CE0 - CE3	Chip Enables
OE	Output Enable
VDD	Power (+5V)
VSS	Ground
VPP	Programming Voltage
N.C.	No Connect

### PIN-OUT DIAGRAM

1	I/O8	12	A14 <sup>1</sup>	23	I/O14	34	I/O24	45	VDD	56	I/O30
2	I/O9	13	CE1	24	I/O13	35	I/O25	46	CE3	57	I/O29
3	I/O10	14	VSS	25	I/O12	36	I/O26	47	A14 <sup>3</sup>	58	I/O28
4	A13	15	I/O15	26	I/O11	37	A6	48	I/O31	59	I/O27
5	VPP	16	A10	27	OE	38	A7	49	A3	60	A0
6	N.C.	17	A11	28	N.C.	39	N.C.	50	A4	61	A1
7	N.C.	18	A12	29	A14 <sup>0</sup>	40	A8	51	A5	62	A2
8	N.C.	19	VDD	30	I/O6	41	A9	52	A14 <sup>2</sup>	63	I/O22
9	I/O0	20	CE0	31	I/O5	42	I/O16	53	CE2	64	I/O21
10	I/O1	21	N.C.	32	I/O4	43	I/O17	54	VSS	65	I/O20
11	I/O2	22	I/O7	33	I/O3	44	I/O18	55	I/O23	66	I/O19

FOR FURTHER INFORMATION  
SEE CHAPTER 10  
FOR COMPLETE DATA SHEET