

HD64540

LAPB Controller

Description

The HD64540 one-chip CMOS communications device supports the LAPB protocols described by CCITT recommendation X.25. Because of its asynchronous bus interface, the HD64540 can be used with 16-bit external microprocessors.

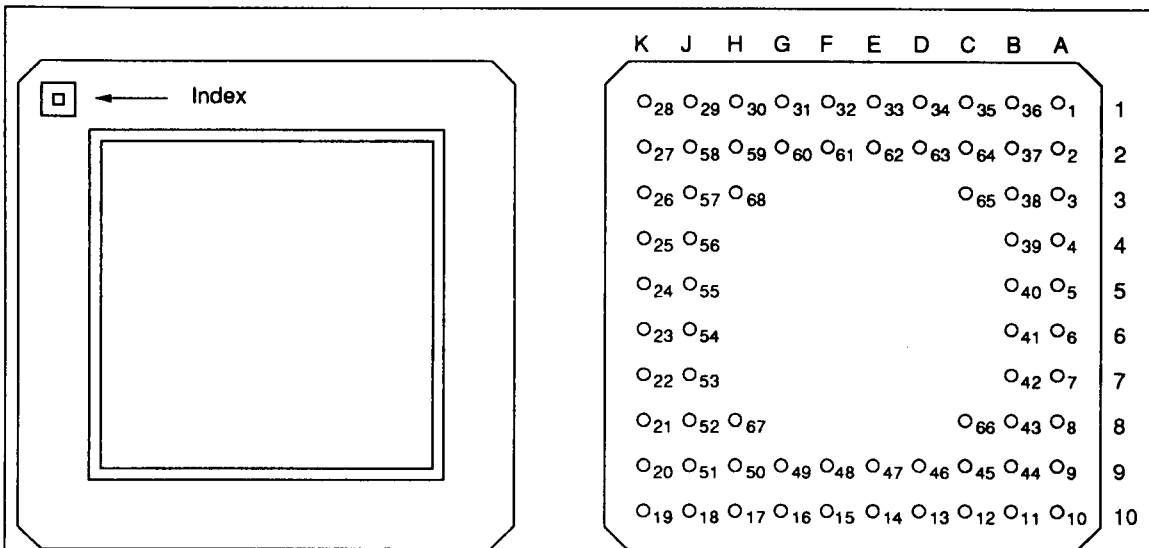
Features

- CCITT recommendation X.25 procedure support
 - Processes X.25 layer 2 protocols (LAPB single link)
 - Reduces main processor load, improving system throughput
- Protocol processing operations
 - HDLC framing, zero insertion/deletion, flag control, retransmission control, and state transition control
- Statistical counters
 - Includes seventeen counters for statistical information: counters for specific frame types transmitted or received, transmission errors, etc.
 - Reports counter status to host processor
- Selectable mode and parameters
 - Terminal (DTE)/network (DCE) mode/transparent mode
 - System parameters programmable
- Chained transmit/receive function
 - Long frames may be stored in multiple data buffers that are chained together and, except for UI, TEST, and XID frames, may be transmitted or received.
 - Transmitted UI, TEST, and XID frame lengths are limited to a single buffer
- High throughput through unique architecture
 - High performance protocol processing and data transmission

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Pin Arrangement (ceramic pin grid array)

PGA-68 pin



(Top view)

(Bottom view)

Pin Code	Pin No.	Name
A1	1	IRQ
A2	2	S/U
A3	3	NUM
A4	4	A ₁
A5	5	V _{SS}
A6	6	φ
A7	7	A ₄
A8	8	A ₅
A9	9	A ₇
A10	10	A ₉ /D ₁
B1	36	READY
B2	37	IACK
B3	38	PF
B4	39	A ₂
B5	40	V _{CC}
B6	41	A ₃
B7	42	A ₆
B8	43	A ₈ /D ₀
B9	44	A ₁₁ /D ₃
B10	11	A ₁₂ /D ₄
C1	35	HDS
C2	64	AIN
C3	65	NC

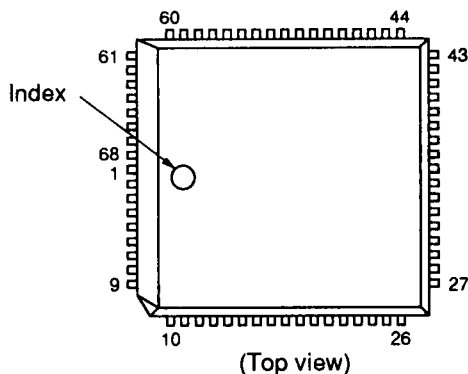
Pin Code	Pin No.	Name
C8	66	A ₁₀ /D ₂
C9	45	A ₁₃ /D ₅
C10	12	A ₁₄ /D ₆
D1	34	R/W
D2	63	LDS
D9	46	A ₁₅ /D ₇
D10	13	A ₁₆ /D ₈
E1	33	V _{SS}
E2	62	V _{CC}
E9	47	V _{SS}
E10	14	A ₁₇ /D ₉
F1	32	DBEN
F2	61	DIN
F9	48	A ₁₉ /D ₁₁
F10	15	A ₁₈ /D ₁₀
G1	31	NC
G2	60	AS
G9	49	A ₂₂ /D ₁₄
G10	16	A ₂₀ /D ₁₂
H1	30	ABEN
H2	59	BACK
H3	68	NUM
H8	67	BRTRY

Pin Code	Pin No.	Name
H9	50	V _{SS}
H10	17	A ₂₁ /D ₁₃
J1	29	CS
J2	58	TXC
J3	57	V _{SS}
J4	56	V _{CC}
J5	55	PI2
J6	54	PO1
J7	53	NUM
J8	52	V _{CC}
J9	51	V _{CC}
J10	18	A ₂₃ /D ₁₅
K1	28	BREQ
K2	27	TXD
K3	26	RXD
K4	25	RXC
K5	24	PI1
K6	23	PI0
K7	22	PO0
K8	21	NUM
K9	20	RES
K10	19	BERR

NUM: Not Users Mode

NC: No Connection

Pin Arrangement (plastic PLCC)



Pin No.	Names	Pin No.	Names	Pin No.	Names
1	V _{SS}	24	A8/D0	47	NUM
2	V _{CC}	25	A9/D1	48	NUM
3	R \bar{W}	26	A10/D2	49	PO0
4	HDS	27	A11/D3	50	PO1
5	LDS	28	A12/D4	51	PI0
6	READY	29	A13/D5	52	PI1
7	A \bar{IN}	30	A14/D6	53	PI2
8	I \bar{RQ}	31	A15/D7	54	RXC
9	I \bar{ACK}	32	A16/D8	55	RXD
10	NC	33	V _{SS}	56	V _{SS}
11	S \bar{U}	34	A17/D9	57	V _{CC}
12	PF	35	A18/D10	58	TXD
13	NUM	36	A19/D11	59	TXC
14	A1	37	A20/D12	60	NUM
15	A2	38	A21/D13	61	BREQ
16	V _{SS}	39	A22/D14	62	BACK
17	V _{CC}	40	A23/D15	63	C \bar{S}
18	ϕ	41	V _{SS}	64	A \bar{S}
19	A3	42	V _{CC}	65	ABEN
20	A4	43	V _{CC}	66	NC
21	A5	44	BTRY	67	DIN
22	A6	45	BERR	68	DBEN
23	A7	46	RES		

NUM: Not Users Mode
 NC: No Connection

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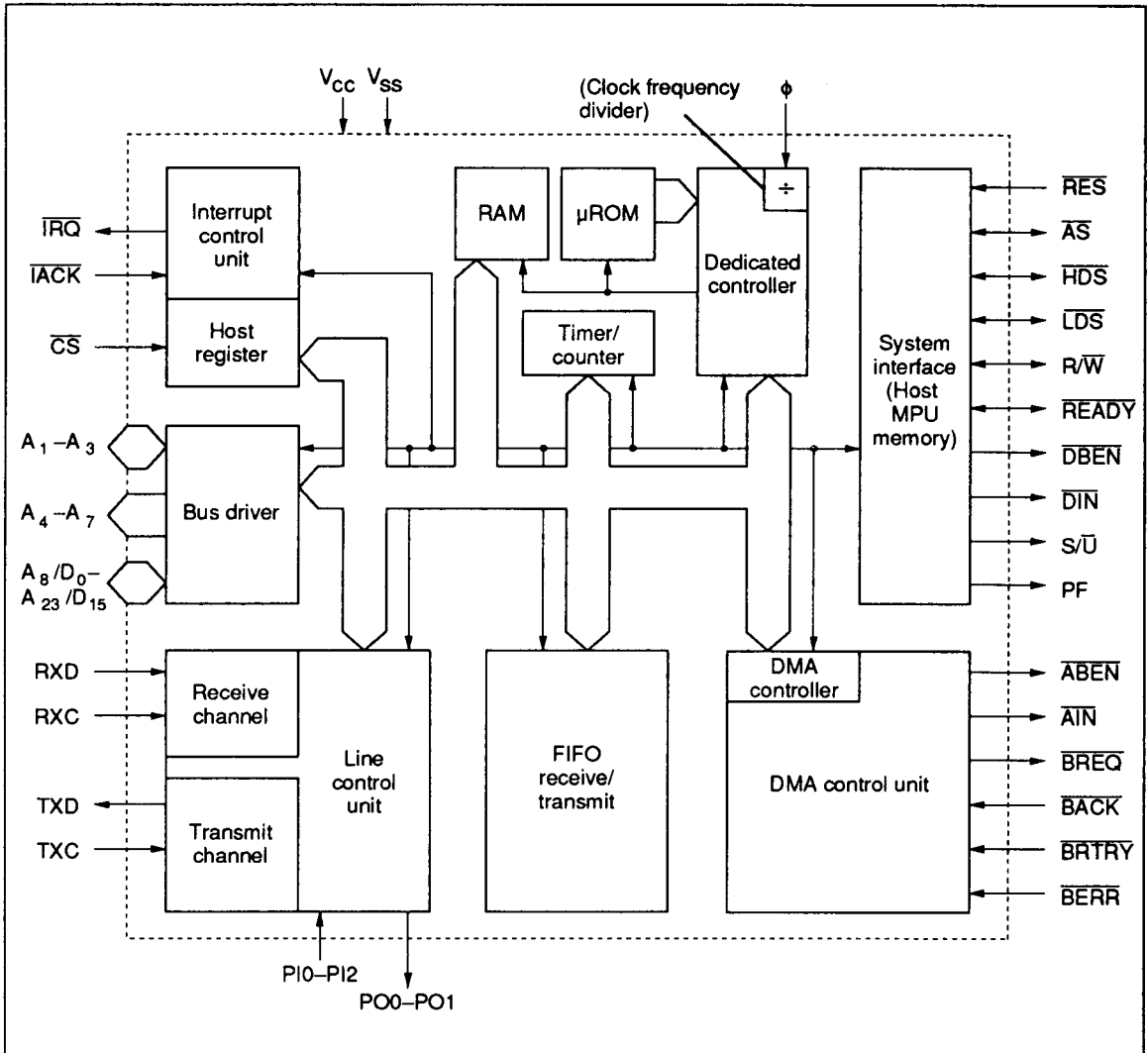
Function Summary

Table 2 summarizes HD64540 functions.

Table 2 HD64540 Function Summary

Feature	Function
Communication protocol	CCITT X.25 layer 2 (LAPB)
Line rate (data rate)	Max 5 Mbps (HD64540R) Max 64 kbps (HD64540)
Number of lines	One full duplex line
Operation mode	Terminal (DTE) mode/network (DCE) mode/transparent mode
Selectable parameters	Maximum number of retransmissions: N2 Maximum number of octets in an information field: N1 Maximum time allowed without receiving acknowledgement to transmitted frames (0.1 to 25.5 seconds, 0.1 second steps): T1 Maximum time allowed for idle state (0.1 to 25.5 seconds, 0.1 second steps or 1 to 255 seconds, 1 second steps): T3 Maximum number of outstanding I frames (1 to 127): K Time for delayed acknowledgement: T2
Diagnostics	Auto-echo Local loopback Auto-echo and local loopback
Peripheral I/O ports	3 inputs, 2 outputs (general-purpose I/O, level detection)
Data encoding	NRZ serial data
Data transfer with memory	DMA
Address space	16 Mbyte
Data bus width	16 bits (multiplexed with address bus)
Power supply	Single +5 V
Power consumption	130 mW (typ)
Process	CMOS 1.3- μ m
Package	68-pin ceramic PGA (pin grid array), 68-pin plastic PLCC
Ordering code	HD64540B03CP, HD64540B03Y, HD64540RB04Y

Block Diagram



System Configuration

Figure 19 is an example of a system configuration using the HD64540. The HD64540 processes the signal received from the line according to protocol

procedure. The processed result is sent to the host MPU. Transmit data is transferred to the line according to commands from the host MPU.

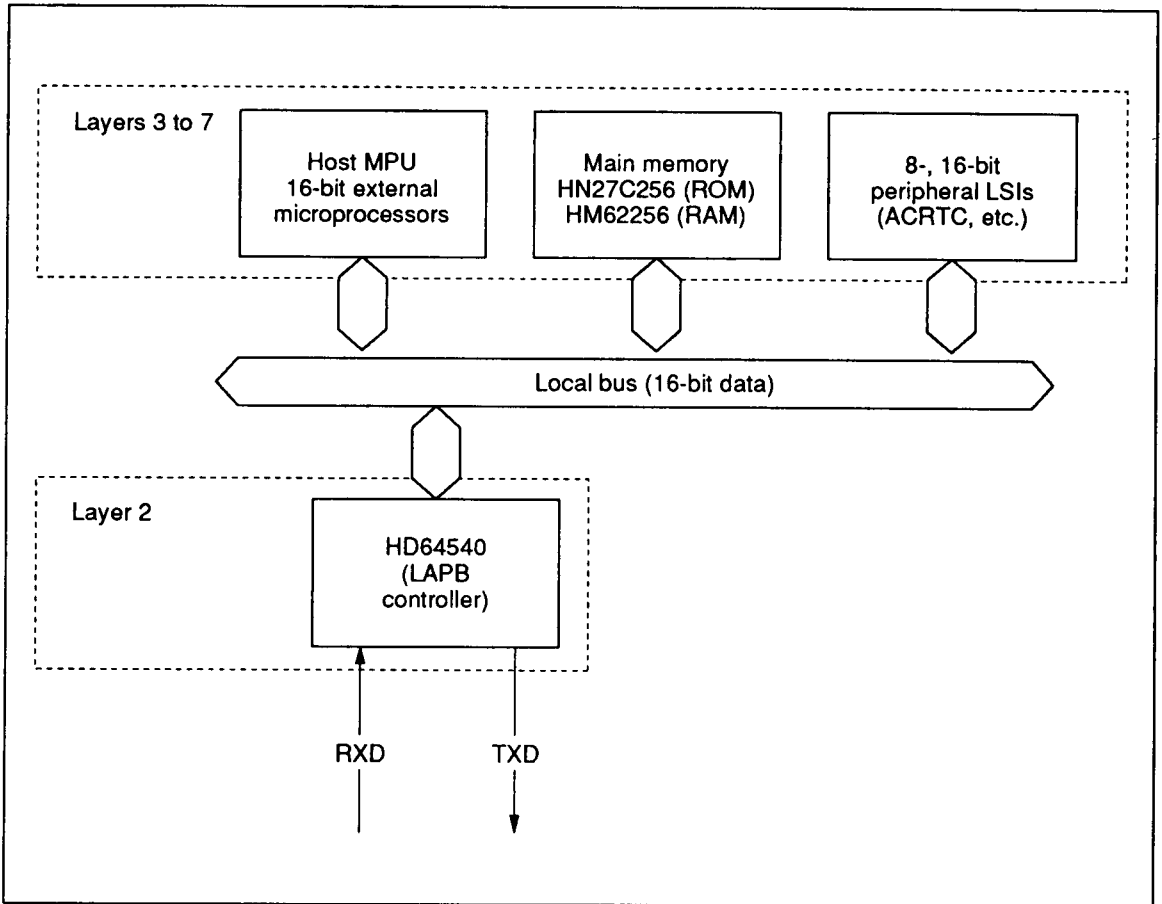


Figure 19 System Configuration Block Diagram

Absolute Maximum Ratings

Table 14 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}^{*2}	7.0	V
Input voltage	V_{in}^{*2}	$V_{SS} - 0.3$ to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.

2. With respect to V_{SS} (system ground).

Recommended Operating Conditions

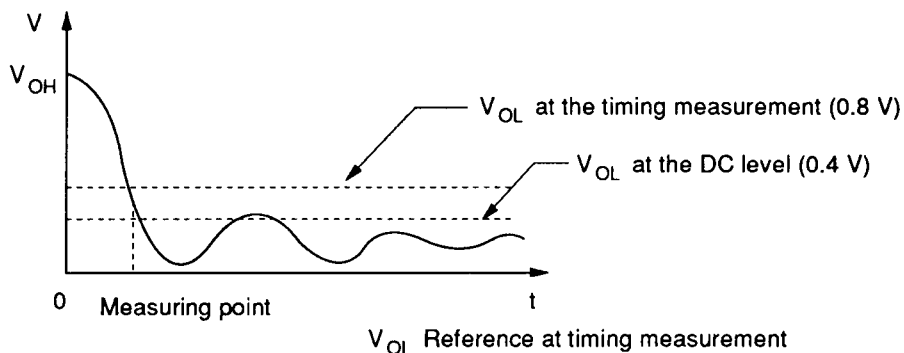
Table 15 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}^{Note}	4.75	5.0	5.25	V
Input low level voltage	V_{IL}^{Note}	-0.3		0.8	V
Input high level voltage	V_{IH}^{Note}	2.0		V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Note: With respect to V_{SS} (system ground).

Timing measurement: The timing measurement point for the output low level is defined at 0.8 V throughout this specification.

The output low level at stable condition (DC characteristics) is defined at 0.4 V.



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Electrical Characteristics

DC Electrical Characteristics

Table 16 DC Electrical Characteristics ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Min	Typ ^{Note}	Max	Unit	Condition
Input high level voltage	V_{IH}	ϕ (clock)	2.4	—	V_{CC}	V
		Others	2.0	—	V_{CC}	V
Input low level voltage	V_{IL}	-0.3	—	0.8	V	
Input leakage current	I_{IN}	—	—	2.5	μA	
Output high level voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -200\ \mu\text{A}$
Output low level voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\ \text{mA}$
Output leakage current	I_{LOH}	—	—	10	μA	
Pin capacitance	C_P	—	—	15	pF	$V_{in} = 0\ \text{V}$ $F = 1\ \text{MHz}$ $T_a = 25^\circ\text{C}$
Current consumption	I_{CC}	—	26	50	mA	

Note: $T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\ \text{V}$.