



## 54F/74F384

# 8-Bit Serial/Parallel Twos Complement Multiplier

### General Description

The 'F384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ( $X_0-X_7$ ). The multiplier word is then applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

The K input is used for expansion to longer X words, using two or more 'F384 devices by connecting the output (SP) of one device to the K input of the other device. The Mode Control (M) input is used to establish the most significant

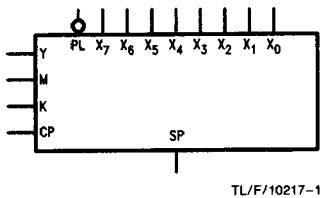
device. An asynchronous Parallel Load ( $\overline{PL}$ ) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data. The Parallel Load ( $\overline{PL}$ ) also clears the output (SP).

### Features

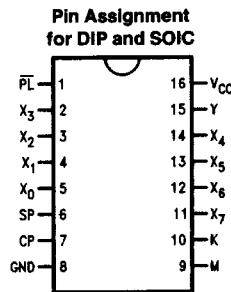
- Twos complement multiplication
- 8-bit by 1-bit sequential logic element
- Parallel inputs accept and store an 8-bit multiplicand ( $X_0-X_7$ )
- K input is used for expansion to longer X words
- Functionally and pin compatible to the Am25LS14A

**Ordering Code:** See Section 5

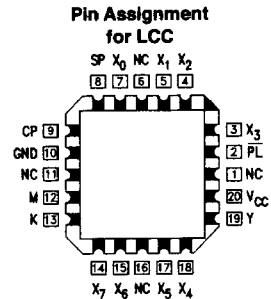
### Logic Symbol



### Connection Diagrams



TL/F/10217-2



TL/F/10217-3

**Input Loading/Fan-Out:** See Section 2 For U.L. Definitions

Pin Names	Description	54F/74F (U.L.) High/Low	$I_{IH}/I_{IL}$ $I_{OH}/I_{OL}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
K	Serial Expansion Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/2.0	20 $\mu$ A/ -1.2 mA
$X_0-X_7$	Multiplicand Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
Y	Serial Multiplier Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
SP	Serial X*Y Product Output	50/33.3	-1 mA/20 mA

## Functional Description

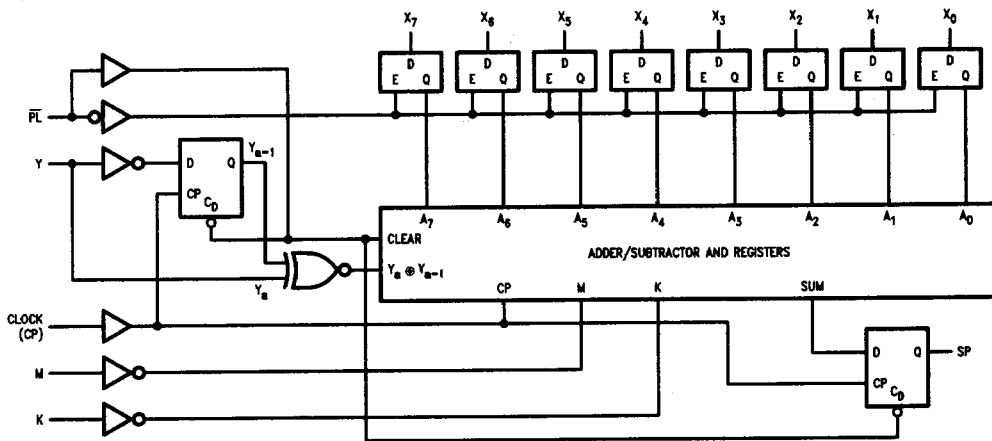
Referring to the Logic Diagram and *Figure A*, the multiplier ( $X_0$ - $X_7$ ) latches are enabled to receive new data when  $\overline{PL}$  is LOW. Data that meet the setup/hold time requirements are stored when  $\overline{PL}$  goes HIGH. The LOW signal on  $\overline{PL}$  clears the output (SP) as well as the internal flip-flops.

New multiplicand data enter the X latches during bit time  $T_0$ . It is assumed that  $\overline{PL}$  goes LOW shortly after the CP rising edge that marks the beginning of  $T_0$  and goes HIGH again one recovery time before the beginning of  $T_1$ . The LSB ( $Y_0$ ) of the multiplier is applied to the Y input during  $T_0$  and must be held one hold time after the beginning of  $T_1$ . One propagation delay after the beginning of  $T_1$ , the LSB ( $S_0$ ) of the product appears at the output (SP). This multiplication process is continued by applying  $Y_1$ - $Y_6$  to the Y input causing  $S_1$ - $S_6$  of the product to appear at the output (SP).

The MSB  $Y_7$  (the sign bit) of the multiplier is first applied to the Y input during  $T_7$  and must be held through  $T_{16}$  causing  $S_7$ - $S_{15}$  of the product to appear at the output (SP). This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm. This is a built-in feature of the 'F322 Shift Register (See *Figure B*).

*Figure C* shows the method of using two F384's to perform a  $12 \times n$  bit multiplication. Notice that the sign of X is effectively extended by connecting  $X_{11}$  to  $X_4$ - $X_7$  of the most significant package. Whereas the  $8 \times 8$  multiplication required 17 clock periods ( $m + n$  to form the product terms plus  $T_0$  to clear the multiplier), the arrangement of *Figure C* requires  $12 + n + 1$  bits to form the product terms.

## Logic Diagram



TL/F/10217-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Internal	Output	Function	
$\overline{PL}$	CP	K	$Y_{n-1}$	SP		
X	X	L	L	X	Most Significant Multiplier Device	
X	X	CS	H	X	Devices Cascaded in Multiplier String	
L	X	X	X	OP	Load New Multiplicand and Clear Internal Sum and Carry Registers	
H	X	X	X	X	Device Enabled	
H	↑	X	X	X	L	Shift Sum Register
H	↑	X	X	X	L	Add Multiplicand to Sum Register and Shift
H	↑	X	X	X	H	Subtract Multiplicand from Sum Register and Shift
H	↑	X	X	X	H	Shift Sum Register

H = HIGH Voltage Level

L = LOW Voltage Level

↑ = LOW-to-HIGH Transition

CS = Connected to SP output of high order device

OP =  $X_i$  latches open for new data ( $i = 0-7$ )

AR = Output as required per Booth's algorithm

X = Immaterial

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Output HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7 V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0 V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (Except PL) V <sub>IN</sub> = 0.5V (PL)
				-1.2	mA	Max	
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		60	90	mA	Max	V <sub>O</sub> = HIGH

**AC Electrical Characteristics** : See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} =$ MII $C_L = 50\text{ pF}$		$T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	50					50		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to SP	3.5	6.5	9.0			3.5	10.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{PL}}$ to SP	6.0	10.0	13.0			6.0	14.0	ns	2-3

**AC Operating Requirements** : See Section 2 for Waveforms

Symbol	Parameter	54F/74F		54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} =$ MII		$T_A, V_{CC} =$ Com			
		Min	Max	Min	Max	Min	Max		
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup Time, HIGH or LOW K to CP	9.0				10.0		ns	2-6
		9.0				10.0			
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold Time, HIGH or LOW K to CP	2.0				2.0		ns	2-6
		2.0				2.0			
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup Time, HIGH or LOW Y to CP	15.0				15.0		ns	2-6
		15.0				15.0			
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold Time, HIGH or LOW Y to CP	2.0				2.0		ns	2-6
		2.0				2.0			
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup Time, HIGH or LOW $X_n$ to $\overline{\text{PL}}$	3.0				4.0		ns	2-6
		6.0				7.0			
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold Time, HIGH or LOW $X_n$ to $\overline{\text{PL}}$	2.0				2.0		ns	2-4
		4.0				4.0			
$t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$	CP Pulse Width HIGH or LOW	7.0				7.0		ns	2-4
		7.0				7.0			
$t_{\text{w}}(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	6.5				7.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{PL}}$ to CP	6.0				10.0		ns	2-6



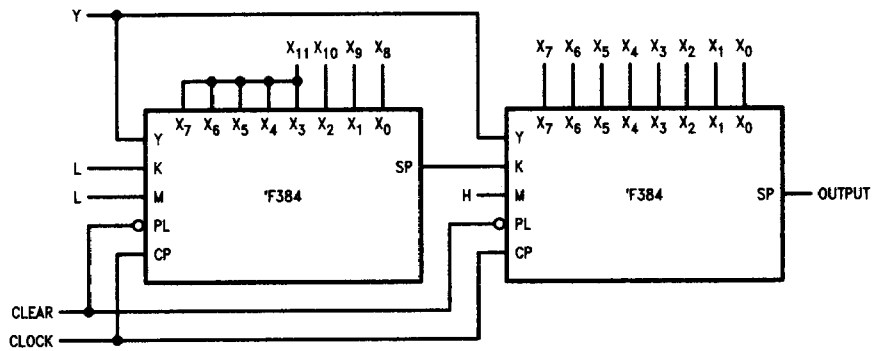


FIGURE C. 12-Bit by n-Bit Two's Complement Multiplier

TL/F/10217-8