FAIRCHILD
A Schlumberger Company

F1600A/F1601A
65,536 x 1-Bit Static RAM

January 1987 PRELIMINARY INFORMATION

Memory & High Speed Logic

Description

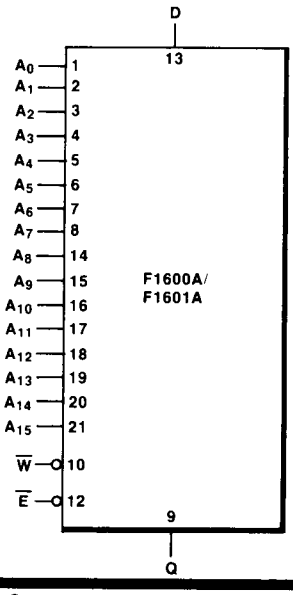
The F1600A/F1601A is a 65,536-bit fully-static, asynchronous, random access memory organized as 65,536 words by 1-bit per word. The F1600A/F1601A is based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device.

- **Fast Address Access Times: 25 ns/35 ns/45 ns (Maximum)**
- **Enable Read Access Faster Than Address Access**
- **Minimum Write Cycle Time, Including Moderate System Timing Skews, Equal to Minimum Read Cycle Time**
- **No Internal Clocks — High Speed Achieved Without Address Transition Detection Circuitry**
- **All Inputs and Outputs Directly TTL Compatible**
- **Separate Data Input and Three-State Output**
- **Available in 22-Pin DIP or LCC**
- **Single +5V Operation (±10%)**
- **Low Power Dissipation (Data Retention F1601A). I_{CCDR} = 50 μA Max. (2.0V ≤ V_{DR} ≤ 3.0V)**
- **Data Retention Supply Voltage F1601A (2.0V to 5.5V)**

Pin Names

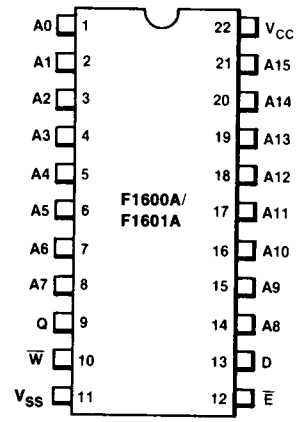
A_0-A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0V)
V_{SS}	Ground (0V)

Logic Symbol

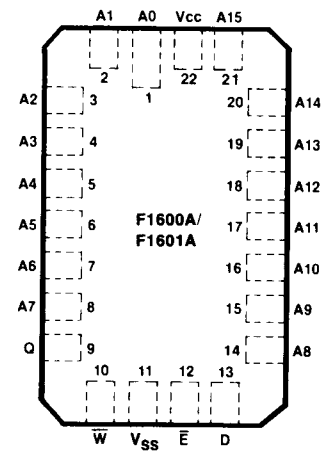


Connection Diagrams

22-Pin DIP (Top View)



22-Pin LCC (Top View)



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003971
3971 FSC

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Absolute Maximum Ratings

Voltage on Any Input or Output Pin With Respect to V_{SS}	-2.0V to V_{CC} + 2V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation	1.0W
Continuous Output Current	25 mA
Average Input or Output Current (Averaged over any 1 μs time interval).	25 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions: T_A = 0°C to +70°C

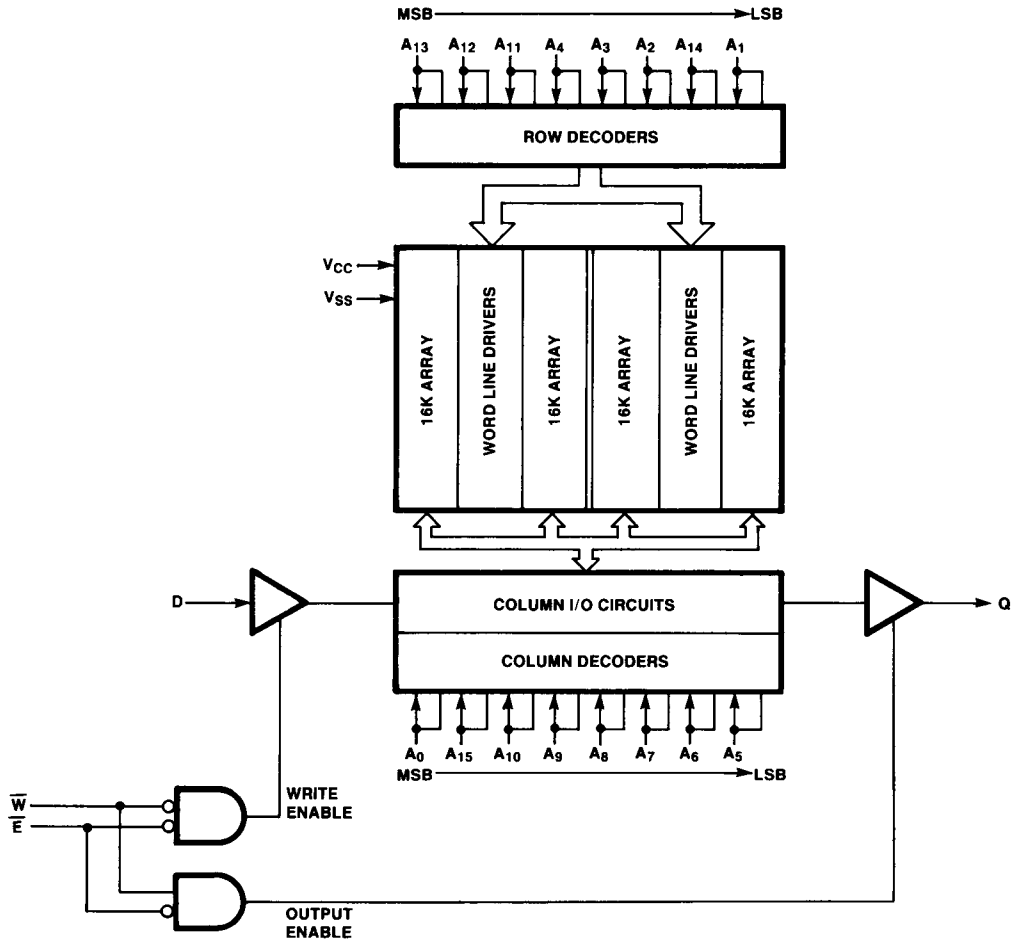
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{CC} +0.5	V
V_{IL}	Input LOW Voltage	-1*		0.8	V

All Voltages are referenced to V_{SS} pin = 0V.

*The device will withstand undershoots to -3V of 20 ns duration.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



DC Operating Characteristics: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, V_{SS} = 0V

Symbol	Characteristic		F1600A-25 F1601A-25 Min	F1600A-25 F1601A-25 Max	F1600A-35 F1601A-35 Min	F1600A-35 F1601A-35 Max	F1600A-45 F1601A-45 Min	F1600A-45 F1601A-45 Max	Unit	Notes on page 7 Condition
I_{LI}	Input Leakage Current			±2		±2		±2	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current			±10		±10		±10	µA	$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$
I_{CC}	Dynamic Operating Supply Current			90		80		70	mA	Min. Read Cycle Time Duty Cycle = 100% Output Open
I_{SB1}	Standby Supply Current			20		20		20	mA	$\overline{E} = V_{IH}$, *see note 1*
I_{SB2}	Full Standby Supply Current	F1600A		15		15		15	mA	*see note 2*
		F1601A		5		5		5		
I_{SB3}	Standby Supply Current (Inputs Active)			45		40		35	mA	$\overline{E} = V_{IH}$, All Other Inputs f_0 = 1/t Cycle
V_{OL}	Output LOW Voltage			0.4		0.4		0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output HIGH Voltage		2.4		2.4		2.4		V	I_{OH} = -4.0 mA
V_{OH}	Output HIGH Voltage		V_{CC}-0.4		V_{CC}-0.4		V_{CC}-0.4		V	I_{OH} = -0.05 mA

AC Test Conditions *(See Notes 3, 11 on page 7)*
Input Pulse Levels.....0V to 3.0V
Input Rise and Fall Times.....3 ns
Input and Output Timing Reference Levels.....1.5V
Output Load.....*See Figures 1 and 2*

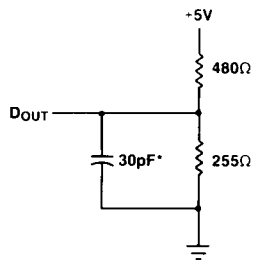
Capacitance *(See note 4)*

Symbol	Parameter	Max.	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$

Figure 1 Output Load

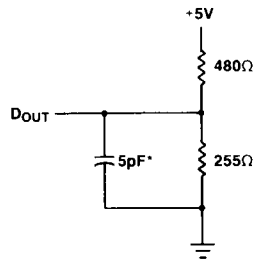


Truth Table

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

Figure 2 Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX)



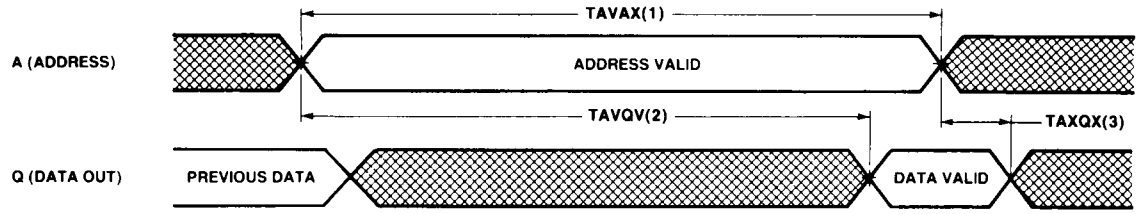
*including scope and jig.

AC Operating Conditions and Characteristics: Read Cycles. T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%

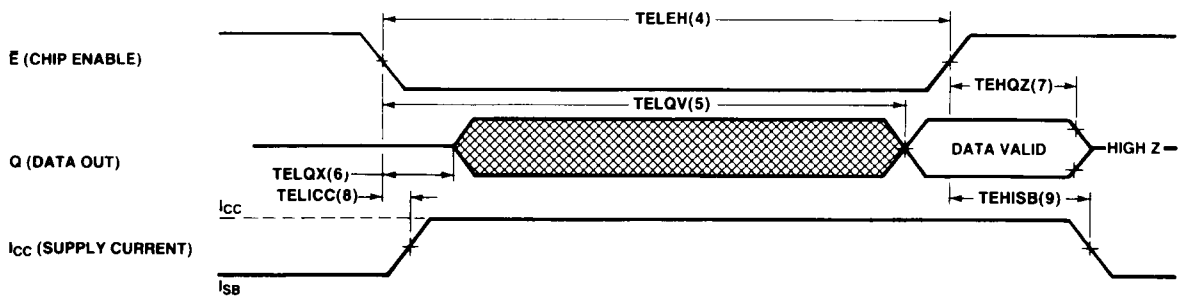
No.	Symbol		Parameter	F1600A-25 F1601A-25		F1600A-35 F1601A-35		F1600A-45 F1601A-45		Unit	Notes on page 7 Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	25		35		45		ns	
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time)		25		35		45	ns	5
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns	
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH	20		30		40		ns	6
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time)		20		30		40	ns	6
6	TELQX	TLZ	Chip Enable LOW to Output Low Z (Chip Enable to Output Active)	5		5		5		ns	
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable)	0	10	0	15	0	15	ns	9
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current	0		0		0		ns	4
9	TEHISB	TPD	Chip Enable HIGH to Standby Current		25		30		40	ns	4

Timing Waveforms

Read Cycle 1 (Where $\overline{E}$ is active prior to or within 5 ns of address change. $\overline{W}$ = V_{IH})



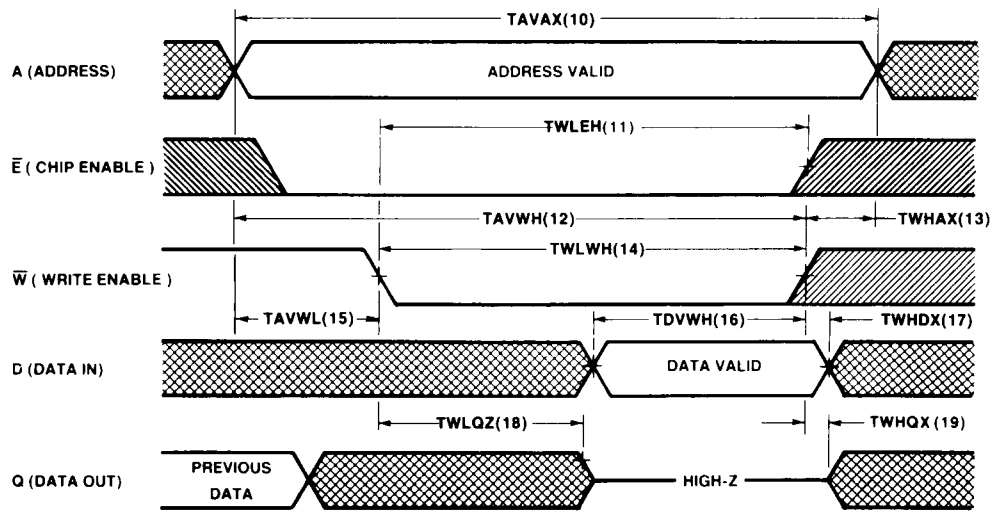
Read Cycle 2 (Where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active. $\overline{W}$ = V_{IH})



AC Operating Conditions and Characteristics: Write Cycle 1. T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%

No.	Symbol		Parameter	F1600A-25 F1601A-25		F1600A-35 F1601A-35		F1600A-45 F1601A-45		Unit	Notes on page 7 Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
10	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	25		35		45		ns	
11	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width)	15		20		25		ns	7,10
12	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write)	15		20		25		ns	7
13	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	7,12
14	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width)	15		20		25		ns	7,10
15	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write)	0		0		0		ns	7,8
16	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write)	6		8		10		ns	7,12
17	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold After End of Write)	0		0		0		ns	7,12
18	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable)	0	9	0	12	0	15	ns	9
19	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active After End of Write)	5		5		5		ns	4

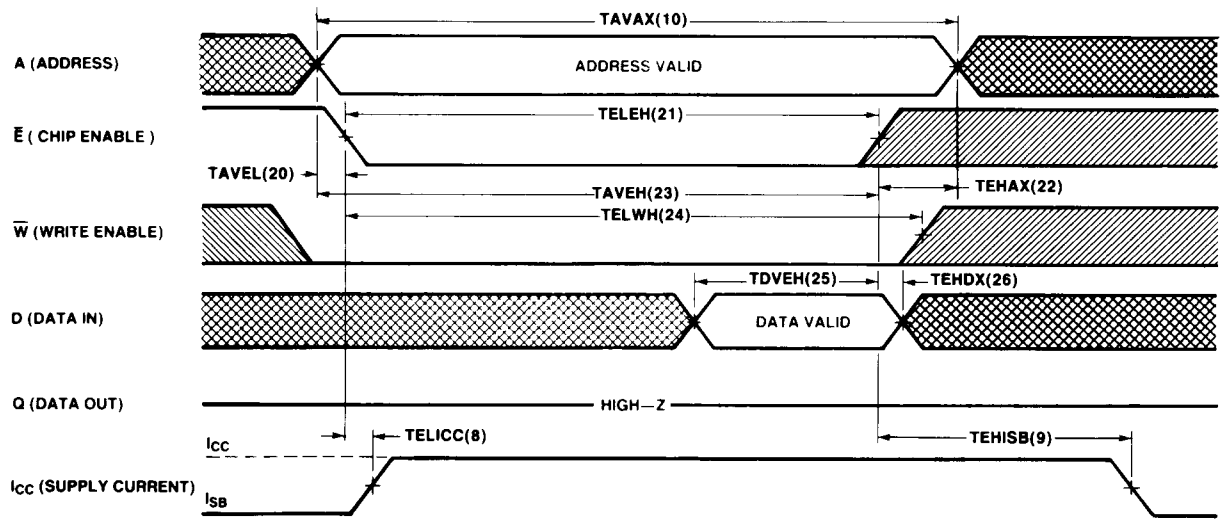
Write Cycle 1 This write cycle is $\overline{W}$ controlled, where $\overline{E}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out may become active, requiring observance of TWLQZ to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{E}$ becoming inactive (HIGH).



AC Operating Conditions and Characteristics: Write Cycle 2. T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%

No.	Symbol		Parameter	F1600A-25 F1601A-25		F1600A-35 F1601A-35		F1600A-45 F1601A-45		Unit	Notes on page 7 Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
20	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Set Up)	0		0		0		ns	7,8
21	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width)	15		20		25		ns	7,10
22	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	7,12
23	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write)	15		20		25		ns	7
24	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width)	15		20		25		ns	7,10
25	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write)	6		8		10		ns	7,12
26	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold)	0		0		0		ns	7,12

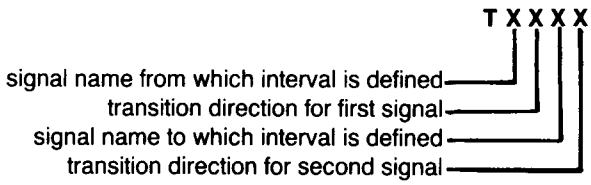
Write Cycle 2 This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (3 state) at the beginning of the write cycle, precluding potential data contention in common I/O applications.



Notes

1. Standby supply current (TTL) is measured with $\bar{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.
2. Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: V_{CC} -0.2V $\leq \bar{E} \leq V_{CC}$ + 0.5V, and all other inputs, (including the data inputs at steady state and satisfying one of two conditions: Either, V_{CC} -0.2V $\leq V_{IN} \leq V_{CC}$ + 0.5V or V_{SS} -0.5V $\leq V_{IN} \leq V_{SS}$ + 0.2V. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.
3. Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operating voltage.
4. This parameter is sampled, not 100% tested.
5. Address Access Time (Read Cycle 1) assumes that $\bar{E}$ occurs before, or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.
6. Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\bar{E}$ transitioning LOW (active). Timing considerations are then referenced to the LOW (active) transitioning edge of $\bar{E}$.
7. A write condition exists only during intervals where both $\overline{W}$ and $\bar{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).
8. Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\bar{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\bar{E}$) to transition LOW (active) is a Don't Care.
9. Transition to the high-impedance state is measured at a ± 500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in Figure 2. This parameter is sampled, not 100% tested.
10. Write pulse width is measured from the time when the last of the two signals $\bar{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\bar{E}$ or $\overline{W}$ to transition HIGH (inactive).
11. For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outside specified switching levels or transition times.
12. Timing specifications of Data Setup to End of Write, Data Hold After End of Write, and Address Hold After End of Write are all referenced to the time when the first of $\bar{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\bar{E}$) to transition HIGH (inactive) is a Don't Care.
13. TAVAV = Read Cycle Timing.
14. V_{CC} -0.2V $\leq \bar{E} \leq$ +5.5V . V_{CC} -0.2V $\leq V_{IN} \leq$ +5.5V or V_{SS} -0.5V $\leq V_{IN} \leq V_{SS}$ +0.2V.

STANDARD TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
H = transition to high state.
L = transition to low state.
V = transition to valid state.
X = transition to invalid or don't care condition.
Z = transition to off (high impedance) condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.


INVALID or Don't Care

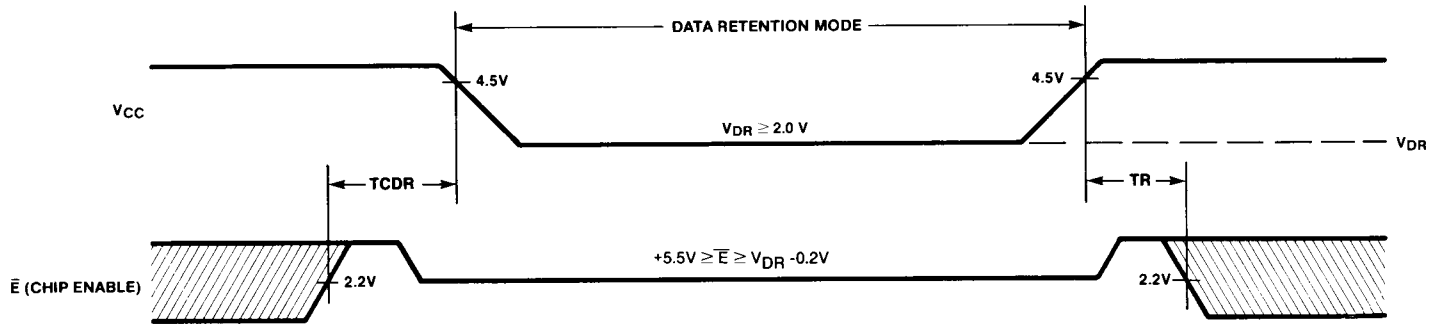

Transition from HIGH to LOW level, may occur any time during this period


Transition from LOW to HIGH level, may occur any time during this period

F1601A Data Retention Characteristics: T_A = 0°C to +70°C, V_{CC} = 2.0V to 5.5V

Symbol	Parameter	Conditions	Min.	Max.	Unit	Notes
V_{DR}	V_{CC} Voltage for Data Retention	V_{CC} -0.2V ≤ $\overline{E}$ ≤ +5.5V V_{CC} -0.2V ≤ V_{IN} ≤ +5.5V or V_{SS} -0.5V ≤ V_{IN} ≤ V_{SS} +0.5V	2.0	5.5	V	
I_{CCDR}	Data Retention Current	V_{DR} = 3.0V, T_A = 0°C to + 70°C		50	µA	14
		V_{DR} = 2.0V, T_A = 0°C to + 70°C		35	µA	14
TCDR	Chip Disable to Data Retention Time		0		ns	
TR	Recovery Time		t_{AVAV}		ns	4, 13

Data Retention Waveform



Applications Information

Using high speed static RAM's at specified full speed can be a challenge, especially write cycle timing. The F1600A/F1601A is designed, specified and tested to simplify this challenge.

Typically SRAM Read and Write Cycle times are specified equal. However, timing requirements (eq. Write Pulse Width, Address Setup and Hold Times) often combine to consume the total Write Cycle Time. This slows down the realizable system speed due to system timing skews between addresses, enables and write pulses.

The F1600A/F1601A simplifies this problem. In both Write Cycle 1 and 2 the speed limiting parameters sum to less than a cycle time:

Write Cycle 1

TAVWL	+	TWLWH	+	TWHAX	<	TAVAX				
0	+	15	+	0	<	25 ns				

And:

TAVWL	+	TWLQZ	+	TDVWH	+	TWHAX	<	TAVAX		
0	+	9	+	6	+	0	<	25 ns		

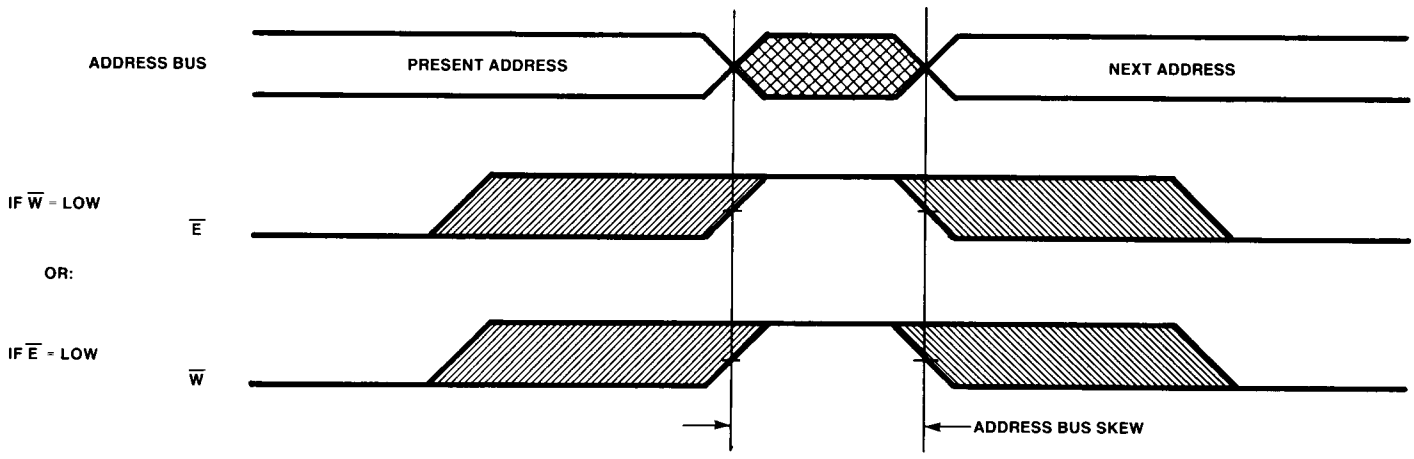
Write Cycle 2

TAVEL	+	TELEH	+	TEHAX	<	TAVAX
0	+	15	+	0	<	25 ns

For all F1600A/F1601A speed grades at least 40% of the write cycle time is available for accomodating realistic system timing skews.

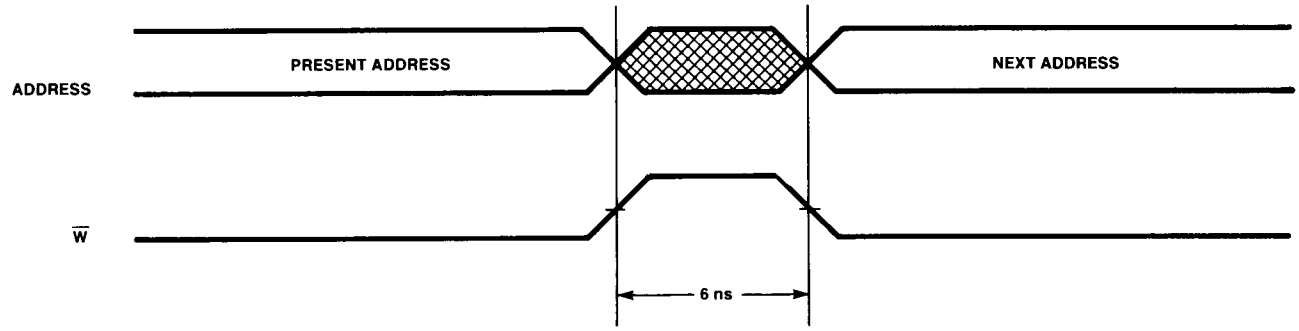
Typical SRAM specifications give no information regarding timing constraints for high speed consecutive write cycles. Timings within a cycle are given, but nothing indicates the timing requirements between cycles. For consecutive read cycles a static (asynchronous) RAM imposes no delay requirement (ie. as soon as data is valid the address may be changed to the next desired address).But timing requirements for write cycles are more complicated. Normally, the write mode is defined by the coincidence of $\overline{W}$ = low and $\overline{E}$ = low. During this time the addresses must be held valid. A changing address could cause data to change at unintended address locations. Most data sheets define two write cycles; one where $\overline{W}$ goes high at the end of the cycle and one where $\overline{E}$ goes high at the end of the cycle. Most data sheets do not define how long either $\overline{E}$ or $\overline{W}$ must remain high before going low again beginning the next write cycle.

The F1600A/F1601A is designed, characterized and tested to alleviate this problem. Characterization data shows that if the write cycle is terminated (by $\overline{E}$ or $\overline{W}$ going high) at the same time as the address change begins (TEHAX or TWHAX = 0 ns), and if the subsequent write cycle begins (by $\overline{E}$ or $\overline{W}$ going low again) at the same time as the address change ends (TAVEL or TAVWL = 0 ns) then the F1600A/F1601A will not disturb data at any address location.

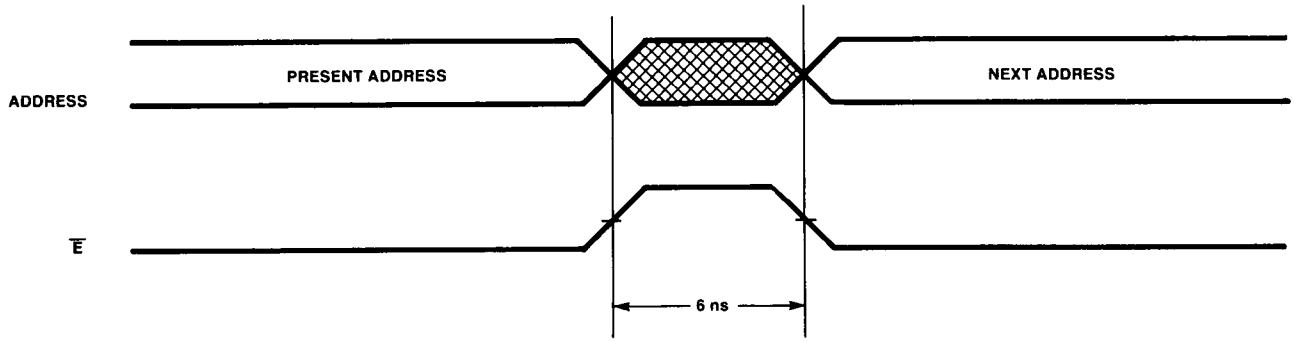


The F1600A/F1601A is guaranteed for the timing condition shown below.

Minimum Write Pulse Disable



Minimum Enable (Write) Disable



Ordering Information (F1600A)

Part Number	Access Time	Temperature Range	Package	Order Code
F1600A-25	25 ns	0° to +70°C	Side-Brazed	1600A DC 25
F1600A-35	35 ns	0° to +70°C	Side-Brazed	1600A DC 35
F1600A-45	45 ns	0° to +70°C	Side-Brazed	1600A DC 45
F1600A-25	25 ns	0° to +70°C	Leadless Chip Carrier	1600A LC 25
F1600A-35	35 ns	0° to +70°C	Leadless Chip Carrier	1600A LC 35
F1600A-45	45 ns	0° to +70°C	Leadless Chip Carrier	1600A LC 45

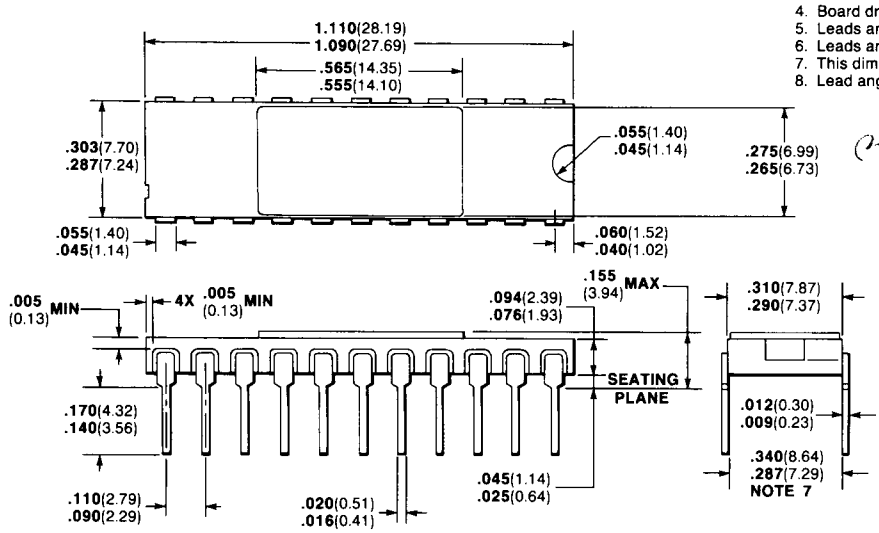
Ordering Information (F1601A)

Part Number	Access Time	Temperature Range	Package	Order Code
F1601A-25	25 ns	0° to +70°C	Side-Brazed	1601A DC 25
F1601A-35	35 ns	0° to +70°C	Side-Brazed	1601A DC 35
F1601A-45	45 ns	0° to +70°C	Side-Brazed	1601A DC 45
F1601A-25	25 ns	0° to +70°C	Leadless Chip Carrier	1601A LC 25
F1601A-35	35 ns	0° to +70°C	Leadless Chip Carrier	1601A LC 35
F1601A-45	45 ns	0° to +70°C	Leadless Chip Carrier	1601A LC 45

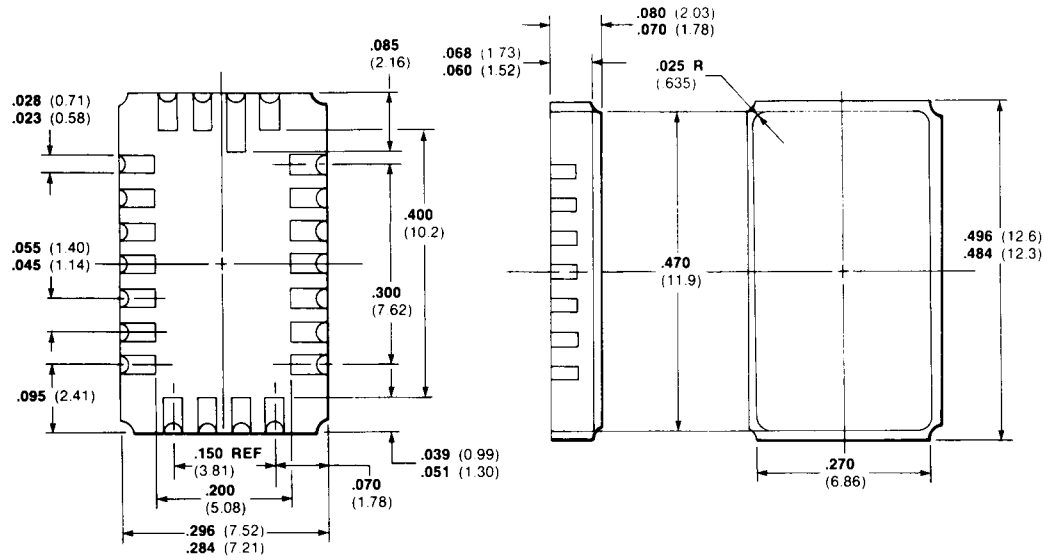
Package Outlines

22-Pin Side-Brazed Package

Notes:
1. Leads are Ni/Au plated alloy 42 or equivalent.
2. Package Material is alumina, 90% min.
3. Lid is Ni/Au plated kovar or equivalant.
4. Board drilling dimensions should equal your practice for .030(0.76) diameter holes.
5. Leads are intended for insertion in hole rows on .300(7.62) centers.
6. Leads are purposely shipped with "positive" misalignment to facilitate insertion.
7. This dimension includes allowable leadspread, inside leads.
8. Lead angle: ∝ 0°-14°.



22-Pin Leadless Chip Carrier



Notes
Chip carrier is 90% min. black alumina
Cap is Ni/Au plated kovar or equivalent
Cavity size is **.214 x .325** (5.44 x 8.26)
Package weight is 0.60 gram