TI486DX2-G66, TI486DX2-G80 MICROPROCESSORS

SRZS006A — MAY 1995 — REVISED JANUARY 1996

- **486DX Architecture and Performance**
  - **—486-Compatible Instruction Set and Register Set**
  - **—Integrated Floating-Point Unit (FPU)**
  - **—Integrated 16-Bit Hardware Multiplier**
  - **—On-Chip 8K-Byte, 32-Bit Instruction/Data Cache Can be Configured to Operate in Write-Through or Write-Back Mode**
  - **—Clock-Doubled Operation at 3.45-V With 5-V-Tolerant I/Os**
  - **—Highly Optimized, Variable-Length Pipeline**
- **High-Performance, Footprint-Compatible Upgrade for 486-Class Platforms**
  - **—Internal CPU Clock Speeds of 66/80 MHz**
  - **—Industry-Standard Footprints Using 168-Pin Ceramic PGA and 208-Pin Ceramic QFP**
- **Advanced Power-Management Features for Battery-Powered Notebook and Energy-Efficient Desktop PC Systems**
  - **—System-Management Mode (SMM)**
  - **—High-Priority System-Management Interrupt (SMI) With Separate Memory-Address Space**
  - **—Suspend Mode (Initiated by Hardware or Software)**
  - **—Fully Static Device Permits Clock-Stop State**
  - **—3.45-V Device With 5-V-Tolerant I/Os Can Be Used in 3.45-V-Only or Mixed 3.45-V/5-V Systems**
- **Architecture Features 32-Bit Internal and 32-Bit External Buses.**
- **Texas Instruments (TI™) EPIC™ Submicron CMOS Technology**

description

The TI486DX2 microprocessors are attractive for new 486-compatible system designs because they are instruction-set and footprint compatible with 486-class platforms. Additionally, they feature an on-chip floating point unit that simplifies implementation of high-performance levels with clock-doubled CPU, on-chip 8K-byte cache, and advanced power-management techniques. Industry-standard footprint facilitates implementation of energy-efficient desktop and/or battery-powered notebook systems.

The TI486DX2 microprocessors support 8-, 16-, and 32-bit data types and operate in real, virtual-8086, and protected modes. The microprocessors achieve high performance through use of a highly optimized, variable-length pipeline combined with a RISC-like, single-cycle execution unit, an integrated floating point unit, a hardware multiplier, and an 8K-byte integrated instruction and data cache. The microprocessor can access up to 4G bytes of physical memory using a 32-bit bus and can perform burst bus cycles to improve the efficiency of multiple word transfers.

The TI486DX2 microprocessors are ideal for battery-powered applications because they typically draw 200 μA when the input clock is stopped in the suspend mode. The devices operate from a 3.45-V power supply in 3.45-V-only systems or mixed 3.45-V/5-V systems.

description (continued)

The TI486DX2 microprocessors contain an on-chip 8K-byte cache memory that can be configured to operate in write-through or write-back mode. Conventional write-through mode updates external memory for each cache transaction. The write-back mode permits cache transactions to occur without updating external memory until a cache miss occurs, a modified line is replaced in the cache, or when an external bus master requires access to data. Configuring the cache to operate in write-back mode can improve overall performance by up to 15% when compared to write-through mode.

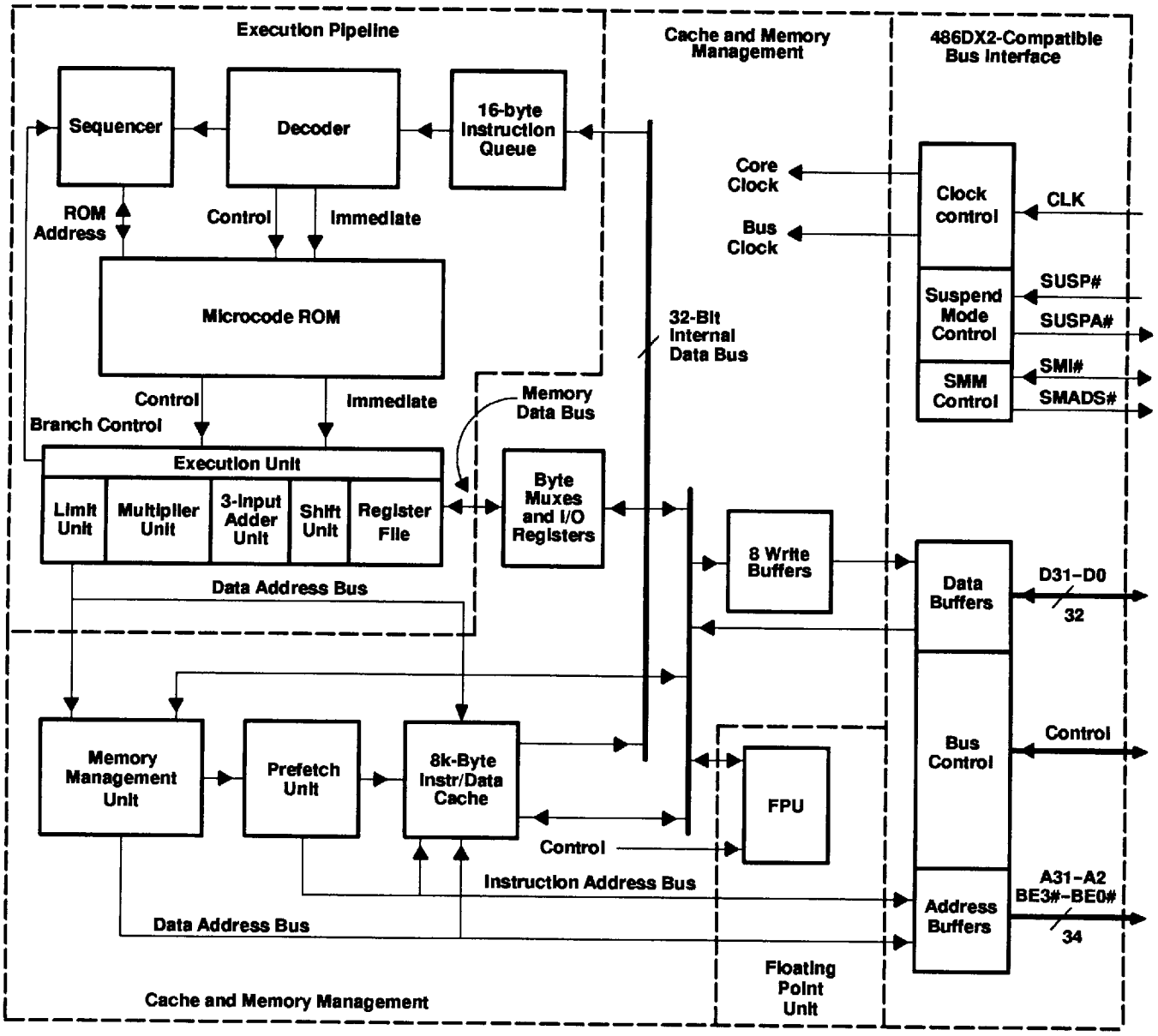
The TI486DX2 microprocessors are fabricated using Texas Instruments EPIC submicron CMOS technology. The combination of high-performance 486 operation, on-chip floating point unit, internal 8K-byte cache, 32-bit external data path, and advanced power-management features makes the TI486DX2 well suited for energy-efficient desktop and notebook applications.

TI486DX2 PRODUCT OPTIONS

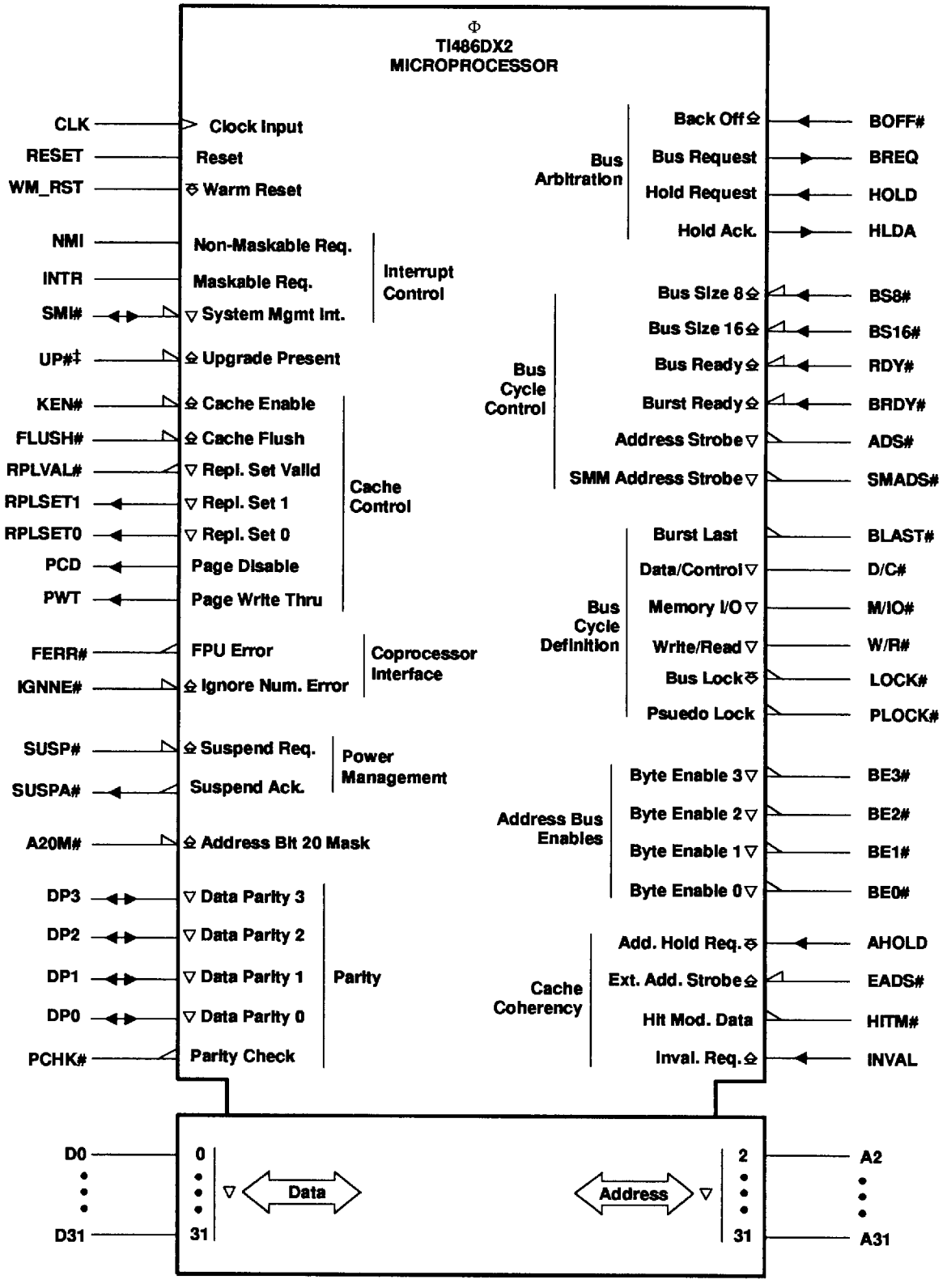
DEVICE PART NO.	SUPPLY VOLTAGE†	SPEED (MHz)		PACKAGE
		CORE	BUS	
TX486DX2-G80-GA	3.45 V	80	40	168-pin PGA
TX486DX2-G66-GA	3.45 V	66	33	
TX486DX2-G80-WR	3.45 V	80	40	208-pin Ceramic QFP
TX486DX2-G66-WR	3.45 V	66	33	

† All devices have 5-V-tolerant I/Os.

functional block diagram



logic symbol†

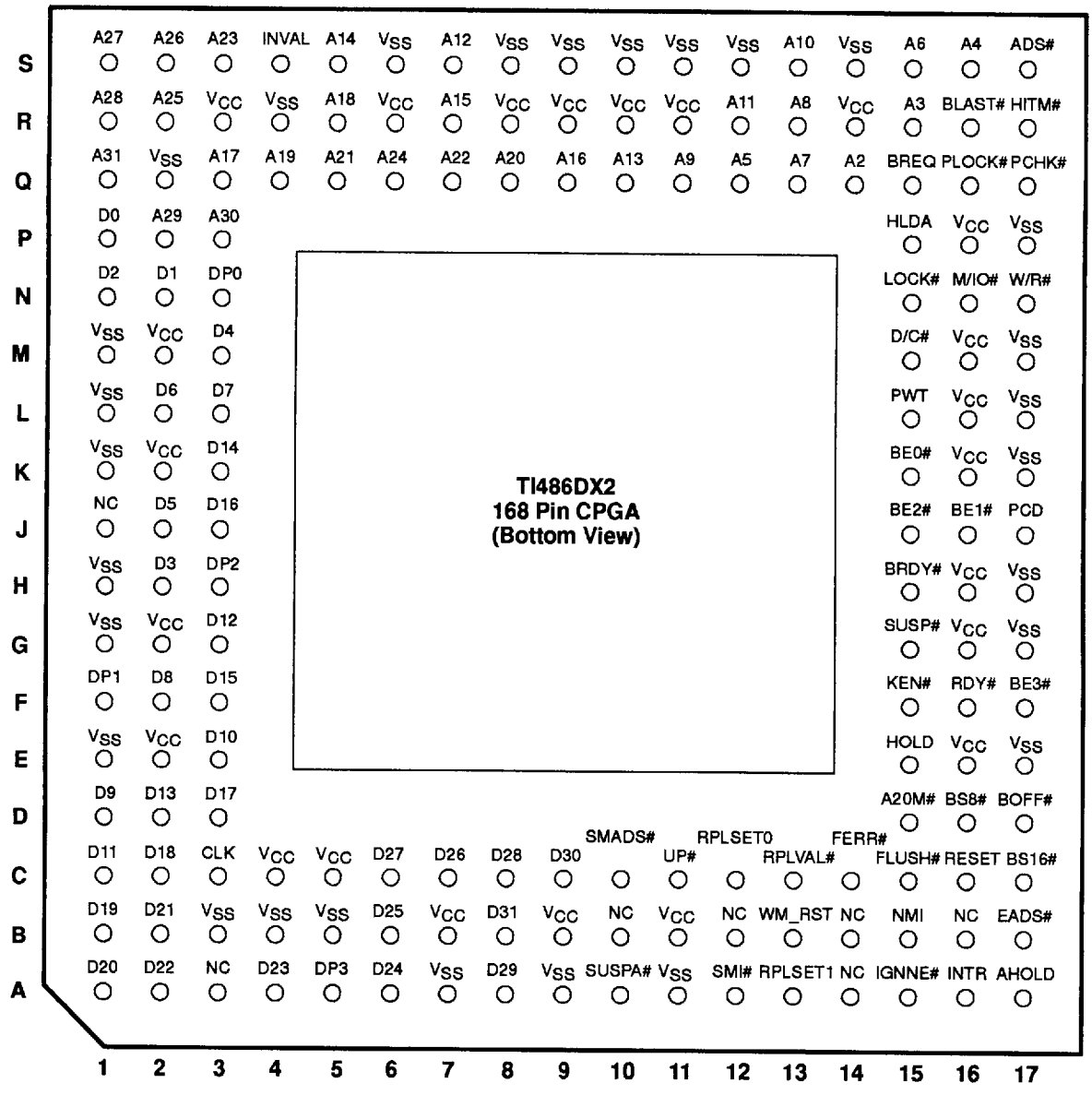


† This symbol is in accordance with ANSI/IEEE Std 91-1991 and IEC Publication 617-12.
‡ 168-pin CPGA only

terminal assignments

The terminal assignments for the 168-pin, CPGA TI486DX2 microprocessors are shown as viewed from the terminal side (bottom) in Figure 1. The signal names are listed in Table 1 and Table 2 sorted by terminal number and signal name, respectively.

Figure 1. 168-Pin CPGA Terminal Assignments



NC — Make no external connection

NOTE A: Connecting or terminating (high or low) any NC terminal(s) may cause unpredictable results or nonperformance of the microprocessor.

Table 1. 168-Pin PGA Signal Names Sorted by Terminal Number

Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name
A1	D20	B12	NC	D17	BOFF#	J15	BE2#	P2	A29	R7	A15
A2	D22	B13	WM_RST	E1	V_{SS}	J16	BE1#	P3	A30	R8	V_{CC}
A3	NC	B14	NC	E2	V_{CC}	J17	PCD	P15	HLDA	R9	V_{CC}
A4	D23	B15	NMI	E3	D10	K1	V_{SS}	P16	V_{CC}	R10	V_{CC}
A5	DP3	B16	NC	E15	HOLD	K2	V_{CC}	P17	V_{SS}	R11	V_{CC}
A6	D24	B17	EADS#	E16	V_{CC}	K3	D14	Q1	A31	R12	A11
A7	V_{SS}	C1	D11	E17	V_{SS}	K15	BE0#	Q2	V_{SS}	R13	A8
A8	D29	C2	D18	F1	DP1	K16	V_{CC}	Q3	A17	R14	V_{CC}
A9	V_{SS}	C3	CLK	F2	D8	K17	V_{SS}	Q4	A19	R15	A3
A10	SUSPA#	C4	V_{CC}	F3	D15	L1	V_{SS}	Q5	A21	R16	BLAST#
A11	V_{SS}	C5	V_{CC}	F15	KEN#	L2	D6	Q6	A24	R17	HITM#
A12	SMI#	C6	D27	F16	RDY#	L3	D7	Q7	A22	S1	A27
A13	RPLSET1	C7	D26	F17	BE3#	L15	PWT	Q8	A20	S2	A26
A14	NC	C8	D28	G1	V_{SS}	L16	V_{CC}	Q9	A16	S3	A23
A15	IGNNE#	C9	D30	G2	V_{CC}	L17	V_{SS}	Q10	A13	S4	INVAL
A16	INTR	C10	SMADS#	G3	D12	M1	V_{SS}	Q11	A9	S5	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M2	V_{CC}	Q12	A5	S6	V_{SS}
B1	D19	C12	RPLSET0	G16	V_{CC}	M3	D4	Q13	A7	S7	A12
B2	D21	C13	RPLVAL#	G17	V_{SS}	M15	D/C#	Q14	A2	S8	V_{SS}
B3	V_{SS}	C14	FERR#	H1	V_{SS}	M16	V_{CC}	Q15	BREQ	S9	V_{SS}
B4	V_{SS}	C15	FLUSH#	H2	D3	M17	V_{SS}	Q16	PLOCK#	S10	V_{SS}
B5	V_{SS}	C16	RESET	H3	DP2	N1	D2	Q17	PCHK#	S11	V_{SS}
B6	D25	C17	BS16#	H15	BRDY#	N2	D1	R1	A28	S12	V_{SS}
B7	V_{CC}	D1	D9	H16	V_{CC}	N3	DP0	R2	A25	S13	A10
B8	D31	D2	D13	H17	V_{SS}	N15	LOCK#	R3	V_{CC}	S14	V_{SS}
B9	V_{CC}	D3	D17	J1	NC	N16	M/IO#	R4	V_{SS}	S15	A6
B10	NC	D15	A20M#	J2	D5	N17	W/R#	R5	A18	S16	A4
B11	V_{CC}	D16	BS8#	J3	D16	P1	D0	R6	V_{CC}	S17	ADS#

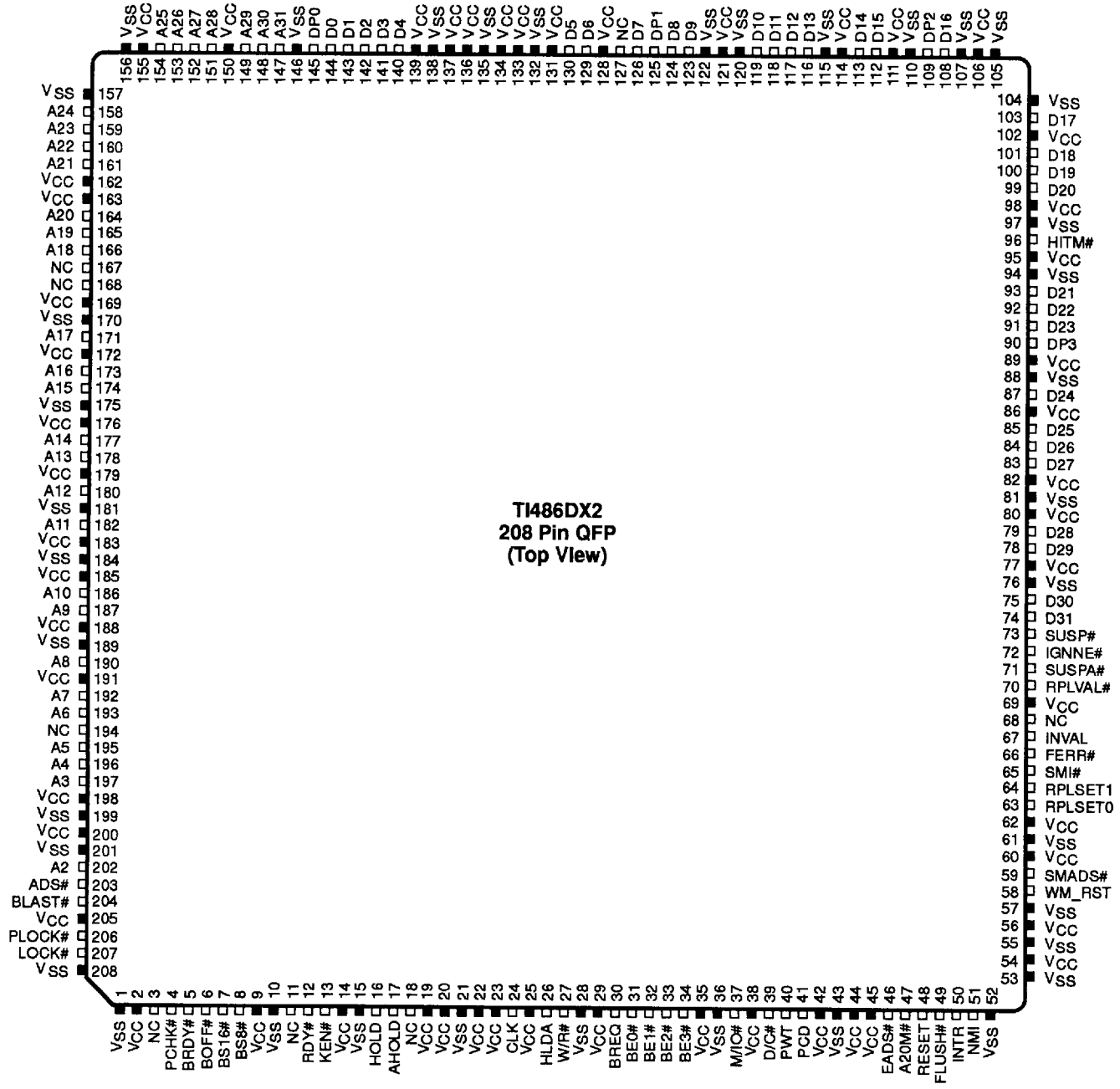
Table 2. 168-Pin PGA Terminal Numbers Sorted by Signal Name

Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.
A2	Q14	A29	P2	D11	C1	HITM#	R17	SUSP#	G15	V_{SS}	A11
A3	R15	A30	P3	D12	G3	HLDA	P15	SUSPA#	A10	V_{SS}	B3
A4	S16	A31	Q1	D13	D2	HOLD	E15	UP#	C11	V_{SS}	B4
A5	Q12	ADS#	S17	D14	K3	IGNNE#	A15	V_{CC}	B7	V_{SS}	B5
A6	S15	AHOLD	A17	D15	F3	INTR	A16	V_{CC}	B9	V_{SS}	E1
A7	Q13	BE0#	K15	D16	J3	INVAL	S4	V_{CC}	B11	V_{SS}	E17
A8	R13	BE1#	J16	D17	D3	KEN#	F15	V_{CC}	C4	V_{SS}	G1
A9	Q11	BE2#	J15	D18	C2	LOCK#	N15	V_{CC}	C5	V_{SS}	G17
A10	S13	BE3#	F17	D19	B1	M/IO#	N16	V_{CC}	E2	V_{SS}	H1
A11	R12	BLAST#	R16	D20	A1	NC	A3	V_{CC}	E16	V_{SS}	H17
A12	S7	BOFF#	D17	D21	B2	NC	A14	V_{CC}	G2	V_{SS}	K1
A13	Q10	BRDY#	H15	D22	A2	NC	B10	V_{CC}	G16	V_{SS}	K17
A14	S5	BREQ	Q15	D23	A4	NC	B12	V_{CC}	H16	V_{SS}	L1
A15	R7	BS8#	D16	D24	A6	NC	B14	V_{CC}	K2	V_{SS}	L17
A16	Q9	BS16#	C17	D25	B6	NC	B16	V_{CC}	K16	V_{SS}	M1
A17	Q3	CLK	C3	D26	C7	NC	J1	V_{CC}	L16	V_{SS}	M17
A18	R5	D/C#	M15	D27	C6	NMI	B15	V_{CC}	M2	V_{SS}	P17
A19	Q4	D0	P1	D28	C8	PCD	J17	V_{CC}	M16	V_{SS}	Q2
A20	Q8	D1	N2	D29	A8	PCHK#	Q17	V_{CC}	P16	V_{SS}	R4
A20M#	D15	D2	N1	D30	C9	PLOCK#	Q16	V_{CC}	R3	V_{SS}	S6
A21	Q5	D3	H2	D31	B8	PWT	L15	V_{CC}	R6	V_{SS}	S8
A22	Q7	D4	M3	DP0	N3	RDY#	F16	V_{CC}	R8	V_{SS}	S9
A23	S3	D5	J2	DP1	F1	RESET	C16	V_{CC}	R9	V_{SS}	S10
A24	Q6	D6	L2	DP2	H3	RPLSET0	C12	V_{CC}	R10	V_{SS}	S11
A25	R2	D7	L3	DP3	A5	RPLSET1	A13	V_{CC}	R11	V_{SS}	S12
A26	S2	D8	F2	EADS#	B17	RPLVAL#	C13	V_{CC}	R14	V_{SS}	S14
A27	S1	D9	D1	FERR#	C14	SMADS#	C10	V_{SS}	A7	W/R#	N17
A28	R1	D10	E3	FLUSH#	C15	SMI#	A12	V_{SS}	A9	WM_RST	B13

NC — Make no external connection

The terminal assignments for the 208-pin, QFP TI486DX2 microprocessors are shown as viewed from the top side in Figure 2. The signal names are listed in Table 3 and Table 4 sorted by terminal number and signal name, respectively.

Figure 2. 208-Pin QFP Terminal Assignments



NC — Make no external connection

NOTE A: Connecting or terminating (high or low) any NC terminal(s) may cause unpredictable results or nonperformance of the microprocessor.

Table 3. 208-Pin QFP Signal Names Sorted by Terminal Number

Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name
1	V_{SS}	53	V_{SS}	105	V_{SS}	157	V_{SS}
2	V_{CC}	54	V_{CC}	106	V_{CC}	158	A24
3	NC	55	V_{SS}	107	V_{SS}	159	A23
4	PCHK#	56	V_{CC}	108	D16	160	A22
5	BRDY#	57	V_{SS}	109	DP2	161	A21
6	BOFF#	58	WM_RST	110	V_{SS}	162	V_{CC}
7	BS16#	59	SMADS#	111	V_{CC}	163	V_{CC}
8	BS8#	60	V_{CC}	112	D15	164	A20
9	V_{CC}	61	V_{SS}	113	D14	165	A19
10	V_{SS}	62	V_{CC}	114	V_{CC}	166	A18
11	NC	63	RPLSET0	115	V_{SS}	167	NC
12	RDY#	64	RPLSET1	116	D13	168	NC
13	KEN#	65	SMI#	117	D12	169	V_{CC}
14	V_{CC}	66	FERR#	118	D11	170	V_{SS}
15	V_{SS}	67	INVAL	119	D10	171	A17
16	HOLD	68	NC	120	V_{SS}	172	V_{CC}
17	AHOLD	69	V_{CC}	121	V_{CC}	173	A16
18	NC	70	RPLVAL#	122	V_{SS}	174	A15
19	V_{CC}	71	SUSPA#	123	D9	175	V_{SS}
20	V_{CC}	72	IGNNE#	124	D8	176	V_{CC}
21	V_{SS}	73	SUSP#	125	DP1	177	A14
22	V_{CC}	74	D31	126	D7	178	A13
23	V_{CC}	75	D30	127	NC	179	V_{CC}
24	CLK	76	V_{SS}	128	V_{CC}	180	A12
25	V_{CC}	77	V_{CC}	129	D6	181	V_{SS}
26	HLDA	78	D29	130	D5	182	A11
27	W/R#	79	D28	131	V_{CC}	183	V_{CC}
28	V_{SS}	80	V_{CC}	132	V_{SS}	184	V_{SS}
29	V_{CC}	81	V_{SS}	133	V_{CC}	185	V_{CC}
30	BREQ	82	V_{CC}	134	V_{CC}	186	A10
31	BE0#	83	D27	135	V_{SS}	187	A9
32	BE1#	84	D26	136	V_{CC}	188	V_{CC}
33	BE2#	85	D25	137	V_{CC}	189	V_{SS}
34	BE3#	86	V_{CC}	138	V_{SS}	190	A8
35	V_{CC}	87	D24	139	V_{CC}	191	V_{CC}
36	V_{SS}	88	V_{SS}	140	D4	192	A7
37	M/IO#	89	V_{CC}	141	D3	193	A6
38	V_{CC}	90	DP3	142	D2	194	NC
39	D/C#	91	D23	143	D1	195	A5
40	PWT	92	D22	144	D0	196	A4
41	PCD	93	D21	145	DP0	197	A3
42	V_{CC}	94	V_{SS}	146	V_{SS}	198	V_{CC}
43	V_{SS}	95	V_{CC}	147	A31	199	V_{SS}
44	V_{CC}	96	HITM#	148	A30	200	V_{CC}
45	V_{CC}	97	V_{SS}	149	A29	201	V_{SS}
46	EADS#	98	V_{CC}	150	V_{CC}	202	A2
47	A20M#	99	D20	151	A28	203	ADS#
48	RESET	100	D19	152	A27	204	BLAST#
49	FLUSH#	101	D18	153	A26	205	V_{CC}
50	INTR	102	V_{CC}	154	A25	206	PLOCK#
51	NMI	103	D17	155	V_{CC}	207	LOCK#
52	V_{SS}	104	V_{SS}	156	V_{SS}	208	V_{SS}

NC — Make no external connection

Table 4. 208-Pin QFP Terminal Numbers Sorted by Signal Name

Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.	Signal Name	Term. No.
A2	202	D8	124	PLOCK#	206	V_{CC}	163
A3	197	D9	123	PWT	40	V_{CC}	169
A4	196	D10	119	RDY#	12	V_{CC}	172
A5	195	D11	118	RESET	48	V_{CC}	176
A6	193	D12	117	RPLSET0	63	V_{CC}	179
A7	192	D13	116	RPLSET1	64	V_{CC}	183
A8	190	D14	113	RPLVAL#	70	V_{CC}	185
A9	187	D15	112	SMADS#	59	V_{CC}	188
A10	186	D16	108	SMI#	65	V_{CC}	191
A11	182	D17	103	SUSP#	73	V_{CC}	198
A12	180	D18	101	SUSPA#	71	V_{CC}	200
A13	178	D19	100	V_{CC}	2	V_{CC}	205
A14	177	D20	99	V_{CC}	9	V_{SS}	1
A15	174	D21	93	V_{CC}	14	V_{SS}	10
A16	173	D22	92	V_{CC}	19	V_{SS}	15
A17	171	D23	91	V_{CC}	20	V_{SS}	21
A18	166	D24	87	V_{CC}	22	V_{SS}	28
A19	165	D25	85	V_{CC}	23	V_{SS}	36
A20	164	D26	84	V_{CC}	25	V_{SS}	43
A20M#	47	D27	83	V_{CC}	29	V_{SS}	52
A21	161	D28	79	V_{CC}	35	V_{SS}	53
A22	160	D29	78	V_{CC}	38	V_{SS}	55
A23	159	D30	75	V_{CC}	42	V_{SS}	57
A24	158	D31	74	V_{CC}	44	V_{SS}	61
A25	154	D/C#	39	V_{CC}	45	V_{SS}	76
A26	153	DP0	145	V_{CC}	54	V_{SS}	81
A27	152	DP1	125	V_{CC}	56	V_{SS}	88
A28	151	DP2	109	V_{CC}	60	V_{SS}	94
A29	149	DP3	90	V_{CC}	62	V_{SS}	97
A30	148	EADS#	46	V_{CC}	69	V_{SS}	104
A31	147	FERR#	66	V_{CC}	77	V_{SS}	105
ADS#	203	FLUSH#	49	V_{CC}	80	V_{SS}	107
AHOLD	17	HITM#	96	V_{CC}	82	V_{SS}	110
BE0#	31	HLDA	26	V_{CC}	86	V_{SS}	115
BE1#	32	HOLD	16	V_{CC}	89	V_{SS}	120
BE2#	33	IGNNE#	72	V_{CC}	95	V_{SS}	122
BE3#	34	INTR	50	V_{CC}	98	V_{SS}	132
BLAST#	204	INVAL	67	V_{CC}	102	V_{SS}	135
BOFF#	6	KEN#	13	V_{CC}	106	V_{SS}	138
BRDY#	5	LOCK#	207	V_{CC}	111	V_{SS}	146
BREQ	30	M/IO#	37	V_{CC}	114	V_{SS}	156
BS16#	7	NC	3	V_{CC}	121	V_{SS}	157
BS8#	8	NC	11	V_{CC}	128	V_{SS}	170
CLK	24	NC	18	V_{CC}	131	V_{SS}	175
D0	144	NC	68	V_{CC}	133	V_{SS}	181
D1	143	NC	127	V_{CC}	134	V_{SS}	184
D2	142	NC	167	V_{CC}	136	V_{SS}	189
D3	141	NC	168	V_{CC}	137	V_{SS}	199
D4	140	NC	194	V_{CC}	139	V_{SS}	201
D5	130	NMI	51	V_{CC}	150	V_{SS}	208
D6	129	PCD	41	V_{CC}	155	WM_RST	58
D7	126	PCHK#	4	V_{CC}	162	W/R#	27

NC — Make no external connection

Terminal Functions

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
A2	Q14	202	Address Bus (active high). The address bus (A31–A2) signals provide addresses for physical memory and I/O ports. Address lines A31–A4 are bidirectional signals used by the TI486DX2 to drive addresses to memory and I/O devices and are also used by the system logic to drive cache inquiry addresses into the processor. Address lines A3–A2 are output signals only and are ignored during cache inquiry cycles. All address lines can be used for addressing physical memory allowing a 4G-byte address space (0000 0000h to FFFF FFFFh). During I/O port accesses, A31–A16 are driven low (except for coprocessor accesses). This permits a 64-Kbyte I/O address space (0000 0000h to 0000 FFFFh).
A3	R15	197	
A4	S16	196	
A5	Q12	195	
A6	S15	193	
A7	Q13	192	
A8	R13	190	
A9	Q11	187	
A10	S13	186	
A11	R12	182	
A12	S7	180	
A13	Q10	178	
A14	S5	177	
A15	R7	174	
A16	Q9	173	
A17	Q3	171	
A18	R5	166	
A19	Q4	165	
A20	Q8	164	
A21	Q5	161	
A22	Q7	160	
A23	S3	159	
A24	Q6	158	
A25	R2	154	
A26	S2	153	
A27	S1	152	
A28	R1	151	
A29	P2	149	
A30	P3	148	
A31	Q1	147	
ADS#	S17	203	Address Strobe (active low). This 3-state output indicates that the TI486DX2 microprocessor has driven a valid address (A31–A2, BE3#–BE0#) and bus-cycle definition (M/IO#, D/C#, W/R#) on the appropriate output pins. If the current cycle is a memory access, ADS# also indicates that the current bus cycle is intended for normal memory space rather than system management memory. ADS# floats while the microprocessor is in a hold-acknowledge or float state. An external pullup resistor is recommended to ensure negation during hold-acknowledge states.
AHOLD	A17	17	Address Hold Request (active high). This input forces the microprocessor to float A31–2 in the next clock cycle. While AHOLD is asserted, only the address bus is disabled. The current bus cycle remains active and completes in the normal fashion. No additional bus cycles are generated while AHOLD is asserted, except cache line write-back cycles in response to a cache inquiry. The microprocessor samples AHOLD during RESET. If AHOLD is asserted at the clock edge prior to the falling edge of RESET, built-in self test is executed prior to issuing any bus cycles. AHOLD is internally connected to a pulldown resistor to prevent it from floating active when left unconnected.

Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
A20M#	D15	47	Address Bit-20 Mask (active low). This input causes the microprocessor to mask (force low) physical address bit 20 when driving the external address bus or performing an internal cache access. Asserting A20M# emulates the 1M-byte address wraparound that occurs on the 8086. A20 masking should not be done by external logic. The A20M# input is ignored during three conditions: • While paging is enabled • While writing back dirty cache data to system memory. (This occurs only if the data was loaded into the cache when A20M# was inactive.) • During system management address space accesses. A20M# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
BE3# BE2# BE1# BE0#	F17 J15 J16 K15	34 33 32 31	Byte Enables BE3# – BE0# (active low). These 3-state outputs determine which bytes within the 32-bit data bus are transferred during a memory or I/O access. During the first cycle of a cache line fill, the microprocessor expects data to be returned as if all data bytes are enabled regardless of the state of the byte enable outputs. BE3#–BE0# float during bus hold states.
BLAST#	R16	204	Burst Last (active low). This output indicates that the current 32-bit data transfer is either the last transfer of a multiple transfer cycle or a single transfer cycle. BLAST# is valid for the second and subsequent clock cycles within both burstable and nonburstable cycles. BLAST# floats during bus hold states.
BOFF#	D17	6	Back Off (active low). This input forces the microprocessor to abort the current bus cycle and relinquish control of the CPU local bus in the next clock. When asserted, the microprocessor enters the bus hold state but the HLDA output is not asserted. The bus hold state persists until BOFF# is negated. Once BOFF# is negated, the aborted bus cycle is restarted. While BOFF# is asserted, the microprocessor ignores any data returned. BOFF# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
BRDY#	H15	5	Burst Ready (active low). This input is generated by the system hardware to indicate that the current transfer within a bus cycle can be terminated. The microprocessor samples BRDY# in the second and subsequent clocks of a multiple transfer cycle. If BRDY# is returned instead of RDY# for the first transfer of a multiple transfer cycle, the microprocessor completes the remaining transfers as a burst cycle. BRDY# must be returned instead of RDY# for each transfer except the final transfer to maintain the burst cycle. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is aborted. BRDY# is active during address hold states. The microprocessor is capable of bursting code fetches, memory data reads, memory data writes (also with BS16# or BS8# active), or cache line write-back cycles if the BWRT bit in CCR2 is set. The microprocessor bursts cache write-back cycles resulting from a cache inquiry only when all four doublewords within the cache line have been modified and need to be written back. When less than three doublewords are modified, the microprocessor issues the write-back cycles as nonburst 32-bit write cycles. BRDY# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
BREQ	Q15	30	Bus Request (active high). This output is asserted when a bus cycle is pending internally. BREQ is asserted in the first clock of a bus cycle as well as during bus hold and address hold states if a bus cycle is pending. If no other bus cycles are pending, BREQ is negated prior to termination of the current cycle.
BS16# BS8#	C17 D16	7 8	Bus Size 16 and Bus Size 8 (active low). These inputs allow connection of the 32-bit microprocessor data bus to an external bus of either 16 or 8 bits. When these inputs are asserted, the microprocessor performs multiple bus cycles to complete a single 32-bit transfer. BS16# and BS8# are sampled each clock. The state of these pins during the clock before RDY# goes low is used to determine the bus size for the current cycle. If both BS8# and BS16# are asserted, BS8# is used. During write cycles, valid data is driven only on the data pins corresponding to the active byte enables. BS16# and BS8# are each connected internally to a pullup resistor to prevent them from floating active when left unconnected.

Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
CLK	C3	24	Clock Input (active high). This input signal is the basic timing reference for the TI486DX2 microprocessors. This signal is also used as an input to time the microprocessor, but the signal is first doubled within the TI486DX2 to provide an internal 2X CPU clock. The CLK signal controls external CPU bus timing. The rising edge of the CLK signal defines the starting point for measurement of external ac specifications for the microprocessor.
D/C#	M15	39	Data Control. This 3-state, bus-cycle-definition signal distinguishes between data and control operations. When high, this signal indicates that the current bus cycle is a data transfer to or from memory. When low, D/C# indicates that the current bus cycle involves a control function such as a halt, interrupt acknowledge, or code fetch.
D0	P1	144	Data Bus (active high). The data bus (D31–D0) signals are 3-state bidirectional signals that provide the data path between the microprocessor and external memory and I/O devices. The data bus inputs data during memory read, I/O read, and interrupt-acknowledge cycles and outputs data during memory and I/O write cycles. Data read operations require that specified data setup and hold times be met for correct operation. The data bus signals float while the CPU is in a hold-acknowledge state.
D1	N2	143	
D2	N1	142	
D3	H2	141	
D4	M3	140	
D5	J2	130	
D6	L2	129	
D7	L3	126	
D8	F2	124	
D9	D1	123	
D10	E3	119	
D11	C1	118	
D12	G3	117	
D13	D2	116	
D14	K3	113	
D15	F3	112	
D16	J3	108	
D17	D3	103	
D18	C2	101	
D19	B1	100	
D20	A1	99	
D21	B2	93	
D22	A2	92	
D23	A4	91	
D24	A6	87	
D25	B6	85	
D26	C7	84	
D27	C6	83	
D28	C8	79	
D29	A8	78	
D30	C9	75	
D31	B8	74	
DP3	A5	90	Data Parity bus (active high). The data parity bus signals are four 3-state bidirectional signals that provide the parity associated with the four-byte data bus. There is one data parity bit for each data byte. Even parity is driven on the data parity bus for all data write cycles. During read cycles, the data parity bus is read by the microprocessor and is used with the corresponding data bus byte to check for even parity.
DP2	H3	109	
DP1	F1	125	
DP0	N3	145	

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
EADS#	B17	46	External Address Strobe (active low). This input indicates that a valid cache inquiry address is being driven on the address bus (A31–2). The microprocessor checks the on-chip cache for this address. If the cache is operating in write-through mode and has no dirty-bit location, the cache line corresponding to the specified address is invalidated if it is present. If the cache is operating in write-back mode or contains dirty data from a previous write-back operation, the cache line corresponding to the specified address is checked for dirty data. If dirty data exists, the dirty data is written to external memory. The state of the INVAL pin at the time EADS# is sampled active determines the final state of the cache line. A cache inquiry cycle using EADS# may be run with the microprocessor in either an address hold or bus hold state and the inquiry address driven by an external device. Additionally, an inquiry cycle can be run while the microprocessor is driving the address bus. In this case, the current address is used as the inquiry address. EADS# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
FERR#	C14	66	Floating-Point Error (active low). This output is asserted when an unmasked floating point error occurs. FERR# is asserted during execution of the FPU instruction that caused the error. FERR# does not float during bus hold states.
FLUSH#	C15	49	Cache Flush (active low). This input invalidates (flushes) the entire cache while in write-through cache mode. If the cache is operating in write-back mode, FLUSH# forces the microprocessor to write back all dirty data in the cache. If the INVAL pin is asserted when FLUSH# is sampled, the microprocessor invalidates the cache contents following the write back of dirty data. FLUSH# needs to be asserted only for a single clock but must meet specified setup and hold times to ensure recognition at a particular clock edge. FLUSH# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
HITM#	R17	96	Hit on Modified Data (active low). This output indicates that the current cache inquiry address has been found in the cache and that dirty data exists in the cache line. HITM# is asserted one clock after EADS# is sampled active and remains asserted until all dirty data has been written to external memory. The microprocessor does not accept additional cache inquiry cycles while HITM# is asserted. HITM# is disabled (floats) following RESET and is enabled by setting the WBAK bit in CCR2.
HLDA	P15	26	Hold Acknowledge (active high). This output indicates that the microprocessor is in a hold-acknowledge state and has relinquished control of its local bus. While in the hold-acknowledge state, the microprocessor drives HLDA active. The microprocessor simultaneously drives the bus and deactivates HLDA when the HOLD request is driven inactive.
HOLD	E15	16	Hold Request (active high). This input indicates that another bus master requests control of the local bus. After recognizing the HOLD request and completing the current bus cycle, burst cycle, cache line fill, sequence of locked bus cycles, or cache line write back, the microprocessor responds by floating the local bus and asserting the hold acknowledge (HLDA) output. Once HLDA is asserted, the bus remains granted to the requesting bus master until HOLD becomes inactive. When the microprocessor recognizes HOLD is inactive, it simultaneously drives the local bus and drives HLDA inactive.

Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION

IGNNE#	A15	72	Ignore Numeric Error (active low). This input forces the microprocessor to ignore any pending unmasked FPU errors and allows continued execution of floating point instructions. When IGNNE# is not asserted and an unmasked FPU error is pending, only these floating point instructions can be executed:
			
			FNCLEX, FNINIT, FNSAVE, FNSTCW, FNSTENV, and FNSTSW.
			
			IGNNE# is ignored when the NE bit in CR0 is set to a 1. This and related actions are detailed using this pseudo-code:
			
			if FERR# = 0 then
			{
			if NE = 1 then
			generate interrupt 16 at next FPU or WAIT instruction
			else
			{
			If IGNNE# = 0 then continue execution
			else
			while IGNNE# AND (FPU instruction OR WAIT instruction).
			wait until IGNNE# goes active. CPU stalls on a FPU instruction or WAIT instruction. CPU continues to service interrupts
			}
			}
			
			IGNNE# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.

INTR	A16	50	Maskable Interrupt Request. This level-sensitive input causes the processor to suspend execution of the current instruction stream and begin execution of an interrupt service routine. The INTR input can be masked (ignored) through the Flag Word register IF bit. When unmasked, the microprocessor responds to the INTR input by issuing two locked interrupt-acknowledge cycles. During the second interrupt acknowledge cycle, the microprocessor reads an 8-bit value, the interrupt vector from an external interrupt controller. The 8-bit interrupt vector indicates the interrupt level that caused generation of the INTR and is used by the CPU to determine the beginning address of the interrupt service routine. To assure recognition of the INTR request, INTR must remain active until the start of the first interrupt-acknowledge cycle.
INVAL	S4	67	Invalidate Request (active high). This input can be driven by the system during a cache inquiry cycle to indicate the final state of the cache line if an inquiry hit occurs. INVAL is sampled with EADS# and is required only when operating the on-chip cache in write-back mode. Assertion of INVAL indicates that the final state of the cache line is invalid. Deassertion indicates that the final state of the cache line is valid and clean. The state of the INVAL input is also sampled with the FLUSH# input to determine the final state of the entire cache. INVAL is ignored following RESET and is enabled by setting the WBAK bit in CCR2. INVAL is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
KEN#	F15	13	Cache Enable (active low). This input indicates that the data being returned during the current cycle is cacheable. When KEN# is active one clock before the first BRDY# or RDY# and the microprocessor is performing a cacheable code fetch or memory data read cycle, the cycle is transformed into a 16-byte cache line fill. Returning KEN# active one clock before ready is returned during the last read in the cache line fill causes the line to be written to the on-chip cache. I/O accesses, locked reads, SMM address space accesses, and interrupt-acknowledge cycles are never cached. KEN# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.

Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
LOCK#	N15	207	Lock (active low). This 3-state, bus-cycle-definition signal is asserted to deny access to the CPU bus by other bus masters. The LOCK# signal may be explicitly activated during bus operations by including the lock prefix on certain instructions. LOCK# is always asserted during descriptor and page table updates, interrupt-acknowledge sequences, and when executing the XCHG instruction. The microprocessor does not enter the hold-acknowledge state in response to HOLD while the LOCK# output is active. An external pullup resistor is recommended to ensure negation during hold-acknowledge states.
M/IO#	N16	37	Memory/IO. This 3-state, bus-cycle-definition signal distinguishes between memory and I/O operations. When high, this signal indicates that the current bus cycle is a memory read or write. When low, M/IO# indicates that the current bus cycle is an I/O read, I/O write, interrupt acknowledge cycle, or a special bus cycle.
NC†	A3 A14 B10 B12 B14 B16 J1	3 11 18 68 127 167 168 194	Make no external connection.
NMI	B15	51	Nonmaskable Interrupt Request. This rising-edge-sensitive input causes the processor to suspend execution of the current instruction stream and begin execution of an NMI interrupt service routine. The NMI interrupt service request cannot be masked by software. Asserting NMI causes an interrupt which internally supplies interrupt vector 2h to the CPU core. External interrupt-acknowledge cycles are not necessary since the NMI interrupt vector is supplied internally.
PCD	J17	41	Page Cache Disable (active high). This output reflects the state of the PCD page attribute bit in the page table entry or the page directory entry. When paging is disabled or during cycles that are not paged, the PCD output is driven low. PCD is masked by the cache disable (CD) bit in CR0 and floats during bus hold states.
PCHK#	Q17	4	Parity Check (active low). This output is used to indicate that a parity error has occurred on a read operation. Parity is checked for all reads except interrupt acknowledge cycles and coprocessor I/O cycles, and it is only checked for valid bytes as indicated by the byte enable outputs and the bus size inputs. PCHK# is valid only during the clock immediately after read data is returned to the microprocessor and is inactive otherwise. Parity errors signaled by a logic low on PCHK# have no effect on processor execution.
PLOCK#	Q16	206	Pseudo Lock (active low). This output is asserted during reads and writes to/from memory that are greater that 32 bits meaning that multiple bus cycles are required to complete the read/write. PLOCK# is asserted during segment descriptor reads (64 bits), cache line fills (128 bits), and noncacheable prefetches (128 bits). The microprocessor does not enter a hold acknowledge state in response to HOLD while PLOCK# is active, except during noncacheable, nonburstable code prefetches. Under these conditions, the microprocessor acknowledges HOLD on bus-cycle boundaries even though PLOCK# is asserted.
PWT	L15	40	Page Write Through (active high). This output reflects the state of the PWT page attribute bit in the page table entry or the page directory entry. When paging is disabled or during cycles that are not paged, the PCD output is driven low. PWT floats during bus hold states.
RDY#	F16	12	Ready (active low). This input is generated by the system hardware to indicate that the current bus cycle can be terminated. During a read cycle, assertion of RDY# indicates that the system hardware has presented valid data to the CPU. When RDY# is sampled active, the microprocessor latches the input data and terminates the cycle. During a write cycle, RDY# assertion indicates that the system hardware has accepted the microprocessor output data. RDY# is active during address hold states. RDY# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.

† Connecting or terminating (high or low) any NC terminal(s) may cuase unpredictable results or nonperformance of the microprocessor.

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Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
RESET	C16	48	Reset (active high). When asserted, RESET suspends all operations in progress and places the microprocessor into a reset state. RESET is an asynchronous input but must meet specified setup and hold times to be properly recognized by the microprocessor at a particular clock edge. While RESET is active, only the HOLD input signal is recognized. The microprocessor output signals are initialized to their reset state during the internal reset sequence. Neither RESET nor WM_RST should be asserted during SMM as system hardware may not be returned to a known state if the SMI handler is not allowed to complete its routine.
RPLSET1 RPLSET0	A13 C12	64 63	Replacement Set 1 – 0 (active high). These 3-state outputs indicate which set in the cache is currently undergoing a line replacement. The RPLSET1 – 0 outputs are disabled (floated) following reset and can be enabled using the RPL bit in the CCR1 Configuration Control register.
RPLVAL#	C13	70	Replacement Set Valid (active low). This three-state output is asserted during a cache line fill cycle indicating that RPLSET1 – 0 are valid for the current cycle. This output and the RPLSET1 – 0 outputs are provided so that external hardware can implement the capability for monitoring the cache LRU replacement algorithm. The RPLVAL output is disabled (floated) following reset and can be enabled using the RPL bit in the CCR1 Configuration Control register.
SMADS#	C10	59	SMM Address Strobe (active low). SMADS#, a three-state output, is asserted instead of the ADS# during SMM bus cycles and indicates that SMM memory is being accessed. SMADS# floats while the CPU is in a hold-acknowledge or float state. The SMADS# output is disabled (floated) following reset and can be enabled using the SMI bit in the CCR1 Configuration Control register. If bit 3 of CCR3 is set, this signal becomes SMIACT#, which indicates that SMI is active.
SMI#	A12	65	System Management Interrupt (active low). This 3-state, bidirectional, level-sensitive, input/output signal is an interrupt with higher priority than the NMI interrupt. SMI# must be active for at least one clock period to be recognized by the microprocessor. After the SMI is acknowledged, the SMI# pin is driven low by the microprocessor for the duration of the SMI service routine. The SMI# input is ignored following reset and can be enabled using the SMI bit in the CCR1 Configuration register. If bit 3 of CCR3 is set, this signal becomes an input only. An external pullup resistor is recommended to ensure negation during hold-acknowledge states.
SUSP#	G15	73	Suspend Request (active low). This input requests the microprocessor to enter suspend mode. After recognizing SUSP# active, the processor completes execution of the current instruction, any pending decoded instructions, and associated bus cycles. During suspend mode, internal clocks are stopped. With SUSPA# asserted, the external CLK input can be stopped in either phase. Stopping the CLK input reduces power consumption. To resume operation, the CLK input is restarted (if stopped), followed by negation of the SUSP# input. The microprocessor resumes instruction fetching and begins execution in the instruction stream at the point it stopped. SUSP# is a level-sensitive input but must meet specified setup and hold times to be properly recognized by the microprocessor at a particular clock edge. The SUSP# input is ignored following reset and can be enabled by setting the SUSP bit in the CCR2 Configuration Control register. SUSP# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
SUSPA#	A10	71	Suspend Acknowledge (active low). This output indicates that the microprocessor has entered the low-power suspend mode as a result of SUSP# assertion or execution of a HLT instruction. SUSPA# remains asserted until SUSP# is negated or until an interrupt is serviced if suspend mode was entered from a HLT instruction. The CLK input can be stopped after SUSPA# has been asserted to reduce power consumption. The SUSPA# output is disabled (floated) after reset and can be enabled by setting the SUSP bit in the CCR2 Configuration Control register.

Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
UP#†	C11	—	Upgrade Present (active low). This input forces the TI486DX2 to float (3-state) all outputs and enter a power-down state. UP# is internally connected to a pullup resistor to prevent it from floating active when left unconnected.
V_{CC}		2, 9 14, 19	Power Supply. All pins must be connected and used.
	B7	20, 22	
	B9	23, 25	
	B11	29, 35	
	C4	38, 42	
	C5	44, 45	
	E2	54, 56	
	E16	60, 62	
	G2	69, 77	
	G16	80, 82	
	H16	86, 89	
	K2	95, 98	
	K16	102, 106	
	L16	111, 114	
	M2	121, 128	
	M16	131, 133	
	P16	134, 136	
	R3	137, 139	
	R6	150, 155	
	R8	162, 163	
	R9	169, 172	
	R10	176, 179	
	R11	183, 185	
	R14	188, 191	
		198, 200	
		205	

† 168-pin CPGA only

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Terminal Functions (continued)

NAME	TERMINAL NO. 168-PIN	TERMINAL NO. 208-PIN	DESCRIPTION
V_{SS}	A7 A9 A11 B3 B4 B5 E1 E17 G1 G17 H1 H17 K1 K17 L1 L17 M1 M17 P17 Q2 R4 S6 S8 S9 S10 S11 S12 S14	1, 10 15, 21 28, 36 43, 52 53, 55 57, 61 76, 81 88, 94 97, 104 105, 107 110, 115 120, 122 132, 135 138, 146 156, 157 170, 175 181, 184 189, 199 201, 208	Ground Pins. All pins must be connected and used.
WM_RST	B13	58	Warm Reset (active high). When asserted, WM_RST suspends all operations in progress and places the microprocessor into a reset state. WM_RST is an asynchronous input but must meet specified setup and hold times to be properly recognized by the microprocessor at a particular clock edge. WM_RST differs from RESET in that the valid and dirty bits in the on-chip cache and the system control bits in the Configuration registers remain unchanged. When RESET and WM_RST are asserted simultaneously, WM_RST is ignored and RESET takes priority. WM_RST is ignored following RESET but can be enabled using the WBAK bit in CCR2. WM_RST has the same timing and duration specifications as RESET. Neither RESET nor WM_RST should be asserted during SMM as system hardware may not be returned to a known state if the SMI handler is not allowed to complete its routine. WM_RST is internally connected to a pulldown resistor to prevent it from floating active when left unconnected.
W/R#	N17	27	Write/Read. This 3-state, bus-cycle-definition signal is low during read cycles (data is read from memory, I/O, or interrupt acknowledge cycle) and is high during write bus cycles (data is written to memory, I/O, or a special bus cycle).

execution pipeline

The execution path in the TI486DX2 microprocessor consists of five pipelined stages optimized for minimal instruction-cycle times. These five stages are:

- Code fetch
- Instruction decode
- Microcode ROM access
- Execution
- Memory/register file write-back

These stages have hardware interlocks that permit execution overlap for successive instructions.

The 16-byte instruction-prefetch queue fetches code in advance and prepares it for decode, helping to minimize overall execution time. The instruction decoder then decodes four bytes of instructions per clock, eliminating the need for a queue of decoded instructions. Sequential instructions are decoded quickly and provided to the microcode. Nonsequential operations do not have to wait for a queue of decoded instructions to be flushed and refilled before execution continues. As a result, both sequential and nonsequential instruction execution times are minimized.

The execution stage uses a RISC-like, single-cycle execution unit and a 16-bit hardware multiplier. The write-back stage provides single-cycle, 32-bit access to the on-chip cache and posts all writes to the cache and system bus using a two-deep write buffer. Posted writes allow the execution unit to proceed with program execution while the bus-interface unit completes the write cycle.

on-chip write-back cache

The on-chip cache is an 8K-byte unified instruction and data cache implemented using a four-way set associative architecture and a least recently used (LRU) replacement algorithm. The cache is designed for optimum performance in write-back mode; however, the cache can be operated in write-through mode. The cache line size is 16 bytes and new lines are allocated only during memory read cycles. Valid status is maintained on a 16-byte cache line basis, but modified or dirty status for write-back mode is maintained on a 4-byte (double-word) basis. Therefore, only the double words that have been modified are written back to external memory when a line is replaced in the cache. The CPU can access the cache in a single internal clock cycle for both reads and writes.

The TI486DX2 on-chip cache can be configured to run in write-through or in write-back mode. By using the write-back cache configuration, performance increases due to a reduction in the number of external memory write cycles. The write-back mode optimizes performance of the CPU core as external memory writes are required only when a cache miss occurs, a modified line is replaced in the cache, or an external bus master requires access to the data. The write-back architecture is especially effective in improving performance of the TI486DX2 devices.

Write-through cache architectures require that all writes to the cache simultaneously update external memory. These updates are unnecessary as long as the cache contains the updated instruction/data necessary to perform the operations. The write-back architecture allows the data to be written to the cache without updating external memory, thereby eliminating unnecessary external writes that can reduce system performance.

floating-point unit (FPU) operations

The TI486DX2 FPU high-performance coprocessor is an integrated part of the microprocessor, thereby eliminating the overhead associated with an external math coprocessor. When the FPU is not in use it is automatically powered down to reduce power consumption. The external system is supported by two terminals, FERR# and IGNNE#. FERR# output reports that an unmasked floating point error has occurred. The input IGNNE# is provided so that the system can signal the processor to ignore numeric error.

clock-doubling

The TI486DX2 microprocessor is designed with an on-chip clock-doubler feature. Upon power-up, the microprocessor's internal core operates at twice the input clock frequency, while the external bus interface remains the same as the input clock frequency. This increases the speed of the on-chip cache, FPU, instruction decode, and instruction execution while the external interface remains the same.

The TI486DX2 provides up to 1.8 times the performance of a 486DX at the same external clock frequency. This performance is achieved by doubling the frequency of the input clock to drive the CPU core. To further enhance this architecture, the TI486DX2 on-chip cache avoids unnecessary external memory accesses by taking advantage of cache write-back and the support of eight write buffers.

In addition to the clock-doubler feature, the TI486DX2 microprocessor supports stopping the CLK input.

power management

The TI486DX2 microprocessors incorporate advanced power-management features such as suspend mode, static operation, and operation at 3.45 V. These capabilities are attractive for battery-powered notebook and energy-efficient desktop PC systems.

system-management mode (SMM)

System-management mode (SMM) provides an additional interrupt and a separate address space that can be used for system power management or software-transparent emulation of I/O peripherals. SMM is entered using the system-management interrupt (SMI#) input or the SMINT instruction. SMI# has a higher priority than any other interrupt. While running in protected SMM address space, the SMI interrupt routine can execute without interfering with the operating system or application programs.

After receiving an SMI# interrupt, portions of the CPU state are automatically saved, SMM is entered, and program execution begins at the base of SMM address space. The location and size of the SMM memory is programmable in the TI486DX2 microprocessors. Eight SMM instructions have been added to the 486 instruction set that permit software entry into SMM and saving and restoring the total CPU state when in SMM mode.

suspend mode and static operation

The power-management feature in the TI486DX2 microprocessors allows a dramatic reduction in the current required when the microprocessor is in suspend mode (typically using less than one percent of the operating current). Suspend mode is entered either by a hardware- or software-initiated action. Using hardware to initiate suspend mode involves a two-pin handshake using the SUSP# and SUSPA# signals.

The software initiates suspend mode with execution of the HLT instruction. Once the microprocessor is in suspend mode, power consumption can be reduced further by stopping the external clock input. The resulting current draw is typically 200 μA.

Since these microprocessors are static devices, no internal CPU data is lost when the clock input is stopped.

mixed 3.45-V and 5-V operation

The TI486DX2 devices operate from a 3.45-V supply. The microprocessors feature 5-V-tolerant inputs and outputs meaning that they can be incorporated in system designs that use both 3.45-V and 5-V devices.

electrical specifications

Electrical specifications include electrical connection requirements for all package pins, maximum ratings, recommended operating conditions, dc electrical characteristics, and ac characteristics.

electrical connections

Requirements are given for power and ground connections, decoupling, termination of inputs with internal pullup/pulldown resistors, termination of system functional inputs requiring external pullup resistors, termination of unused inputs, and connection to terminals designated NC.

power and ground connections and decoupling

The TI486DX2 microprocessors must be installed and tested using standard high-frequency techniques. The high clock frequencies used in the microprocessors and their output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the dc power leads with low-inductance decoupling capacitors, by using low-impedance wiring, and by making connection to all of the V_{CC} and V_{SS} (GND) terminals.

pullup/pulldown resistors

Table 5 lists the terminals that are internally connected to pullup or pulldown resistors. The pullup resistors are connected to V_{CC} and the pulldown resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pullup or pulldown resistors. The SUSP# terminal is unique because it is connected to a pullup resistor only when it is not asserted.

The internal pullup and pulldown resistors are designed to tie-off the individual internal signal associated with that pin. External signals should not be terminated to any of these pins.

Table 5. Terminals Connected to Internal Pullup and Pulldown Resistors

SIGNAL	168-TERMINAL	208-TERMINAL	RESISTOR
A20M#	D15	47	Pullup
AHOLD	A17	17	Pulldown
BOFF#	D17	6	Pullup
BS16#	C17	7	Pullup
BS8#	D16	8	Pullup
BRDY#	H15	5	Pullup
EADS#	B17	46	Pullup
FLUSH#	C15	49	Pullup
IGNNE#	A15	72	Pullup
INVAL	S4	67	Pullup
KEN#	F15	13	Pullup
RDY#	F16	12	Pullup
UP#†	C11	194	Pullup
SUSP#	G15	73	Pullup
WM_RST	B13	58	Pulldown

† 168-pin CPGA only

TI recommends that the ADS#, LOCK#, and SMI# output terminals be connected to pullup resistors, as indicated in Table 6. The external pullups ensure that the signals remain negated during hold-acknowledge states.

Table 6. Terminals Requiring External Pullup Resistors

SIGNAL	168-TERMINAL	208-TERMINAL	EXTERNAL RESISTOR
ADS#	S17	203	20-kΩ pullup
LOCK#	N15	207	20-kΩ pullup
SMI#	A12	65	20-kΩ pullup

NC designated terminals

Terminals designated NC must be left disconnected. Connecting or terminating any NC terminal(s) to a pullup resistor, pulldown resistor, or an active signal can cause unpredictable results or nonperformance of the microprocessor.

unused signal input terminals

All signal inputs not used by the system designer and not listed in Table 5 should be connected either to V_{SS} or to V_{CC}. Connect active-high inputs to V_{SS} through a 20-kΩ (±10%) pulldown resistor and active-low inputs to V_{CC} through a 20-kΩ (±10%) pullup resistor to prevent possible spurious operation.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 to 4 V
Voltage on any terminal ..... −0.5 to 6 V
Input clamp current, I_{IK} ..... 10 mA
Output clamp current, I_{OK} ..... 25 mA
Case temperature, T_C ..... −65°C to 110°C
Storage temperature, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to V_{SS}		3.3	3.6	V
V_{IH}	High-level input voltage			2	5.5	V
V_{IL}	Low-level input voltage			−0.3	0.6	V
I_{OH}	High-level output current	$V_{OH} = V_{OH}$(min)			−1	mA
I_{OL}	Low-level output current	$V_{OL} = V_{OL}$(max)			3	mA
T_C	Case temperature	Power applied	GA 168-pin PGA	0	85	°C
			WR 208-pin QFP	0	75	

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electrical characteristics at recommended operating conditions

PARAMETER			TEST CONDITIONS		168-PIN PACKAGE			208-PIN PACKAGE			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OL}	Low-level output voltage		I_{OL} = 5 mA				0.35			0.35	V
V_{OH}	High-level output voltage		I_{OH} = −1 mA		2.4			2.4			V
I_I	Input current (leakage)		V_{IN} = 0, $V_{IN} \geq V_{CC}$,	See Note 1			±15			±15	µA
I_{IH}	High-level input current		V_{IH} = 2.4 V,	See Note 2			200			200	µA
I_{IL}	Low-level input current		V_{IL} = 0.45 V,	See Note 1			−400			−400	µA
I_{CC}	Supply current (active mode)	TI486DX2-G66	CLK = 66 MHz,	See Note 3		400	850		400	850	mA
		TI486DX2-G80	CLK = 80 MHz,	See Note 3		450	950		450	950	mA
I_{CCSM}	Supply current (suspend mode)	TI486DX2-66	CLK = 66 MHz,	See Notes 3 and 4		14	46		14	46	mA
		TI486DX2-80	CLK = 80 MHz,	See Notes 3 and 4		16	48		16	48	mA
I_{CCSS}	Supply current (standby)		0 MHz, Suspended, CLK stopped	See Note 5		0.2	15		0.2	1	mA
C_i	Input capacitance		f = 1 MHz,	See Note 5			20			20	pF
C_o	Output or I/O capacitance		f = 1 MHz,	See Note 6			20			20	pF
C_{clk}	Clock input capacitance		f = 1 MHz,	See Note 6			20			20	pF

† Typical values are at V_{CC} = 3.45 V and T_A = 25°C.

NOTES: 1. Applicable for all input terminals except those with an internal pullup resistor. See Table 5.
2. Applicable for all inputs that have an internal pulldown resistor. See Table 5.
3. Refers to the internal frequency
4. All inputs at 0.4 V or $V_{CC-0.4}$. All inputs held static, (except CLK as indicated). All outputs unloaded (static I_{OUT} = 0). Valid for UP# = 0 (168-pin CPGA only).
5. All inputs at 0.4 V or $V_{CC-0.4}$. All inputs held static,. All outputs unloaded (static I_{OUT} = 0).
6. Not 100% tested

switching characteristics

The switching characteristics provide detailed information regarding measurement points, specific timing requirements for setup and hold times, and propagation delay times of the TI486DX2 microprocessors.

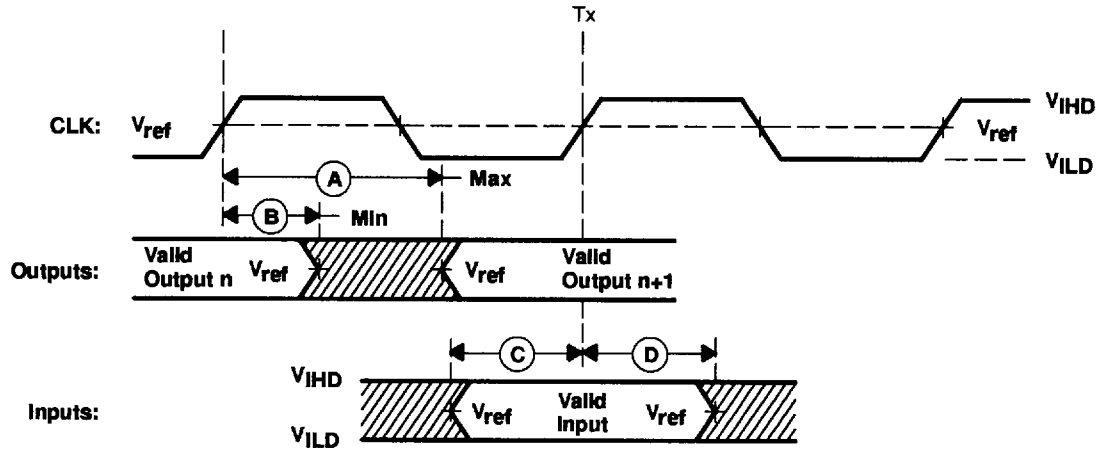
measurement points for switching characteristics

The rising-clock-edge reference level, V_{ref}, and other reference levels are specified in Table 7. Input or output signals must cross these levels during testing.

Table 7. Measurement Levels for Switching Characteristics

SYMBOL	MEASUREMENT LEVEL	UNIT
V_{ref}	1.5	V
V_{IHD}	2.3	V
V_{ILD}	0	V

Figure 3 shows delays (A and B) and input setup and hold times (C and D). Input setup and hold times are specified minimums, defining the smallest acceptable sampling window during which a synchronous input signal must be stable for correct operation.



LEGEND: A – Maximum Output Delay Specification
B – Minimum Output Delay Specification
C – Minimum Input Setup Specification
D – Minimum Input Hold Specificaton

Figure 3. Measurement Points for Delay, Setup, and Hold Times

switching characteristics and timing requirements for TI486DX2-G66 over recommended supply voltage and operating case temperature ranges

PARAMETER		ALT. SYMBOL	FIGURES	NOTES	TI486DX2-G66		UNIT
					MIN	MAX	
f_{clock}	CLK frequency (internal)	f_{CLK}		see Note 7		66	MHz
t_c	CLK period	T1	Figure 4	see Note 8	30		ns
t_{wH}	Pulse duration, CLK high	T2			11		
t_{wL}	Pulse duration, CLK low	T3			11		
t_f	CLK fall time	T4				3	
t_r	CLK rise time	T5				3	
t_{pd}	A31–A2, ADS#, BE3#–BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# valid delay	T6	Figure 6	C_L = 50 pF	2	16	ns
t_{pd}	SMADS#, SMI# valid delay	T6a	Figure 6	C_L = 50 pF	2	16	
t_{dis}	A31–A2 ADS#, BE3#–BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# float delay	T7	Figure 7	see Note 9		20	
t_{dis}	SMADS#, SMI# float delay	T7a	Figure 7	see Note 9		20	
t_{pd}	PCHK# valid delay	T8	Figure 5	C_L = 50 pF	2	22	ns
t_{pd}	BLAST#, PLOCK# valid delay	T8a	Figure 6		2	20	
t_{pd}	HITM#, RPLSET1–0, RPLVAL#, SUSPA# valid delay	T8b	Figure 6		2	20	
t_{dis}	BLAST#, PLOCK# float delay	T9	Figure 7	see Note 9		20	
t_{dis}	RPLSET1–0, RPLVAL# Float delay	T9a	Figure 7	see Note 9		22	
t_{pd}	D31–0, DP3–0 write valid delay	T10	Figure 6	C_L = 50 pF see Note 10	2	19	ns
t_{pd}	D31–0, DP3–0 write float delay	T11	Figure 7	C_L = 50 pF see Note 9		20	
t_{su}	EADS# setup time	T12	Figure 8		6		ns
t_{su}	INVAL setup time	T12a			6		
t_h	EADS# hold time	T13			3		
th	INVAL hold time	T13a			3		
t_{su}	BS16#, BS8#, KEN# setup time	T14	Figure 8		6		ns
t_h	BS16#, BS8#, KEN# hold time	T15			3		
t_{su}	BRDY#, RDY# setup time	T16	Figure 8		6		ns
t_{su}	BRDY#, RDY# setup time	T17			3		
t_{su}	AHOLD, HOLD setup time	T18	Figure 8		6		ns
t_{su}	BOFF# setup time	T18a			9		
t_h	AHOLD, HOLD, BOFF# hold time	T19			3		
t_{su}	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET setup time	T20	Figure 8	see Note 11	6		ns
t_{su}	SMI#, SUSP#, WM_RST setup time	T20a			6		
t_h	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET hold time	T21	Figure 8	see Notes 10 and 11	3		ns
th	SMI#, SUSP#, WM_RST hold time	T21a			3		
t_{su}	A31–4, D31–0, DP3–0 read setup time	T22	Figure 8		6		ns
t_h	A31–4, D31–0, DP3–0 read hold time	T23			3		

NOTES: 7. Input clock can be stopped; therefore, minimum CLK frequency is 0 MHz.
8. These parameters are not tested. They are determined by design characterization.
9. Float condition occurs when maximum output current becomes less than I_I in magnitude. Float is not 100% tested.
10. Not 100% tested.
11. These inputs are allowed to be asynchronous to CLK. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK period.

switching characteristics and timing requirements for TI486DX2-G80 over recommended supply voltage and operating case temperature ranges

PARAMETER		ALT. SYMBOL	FIGURES	NOTES	TI486DX2-G80		UNIT
					MIN	MAX	
f_{clock}	CLK frequency (internal)	f_{CLK}		see Note 7		80	MHz
t_c	CLK period	T1	Figure 4	see Note 8	25		ns
t_{wH}	Pulse duration, CLK high	T2			9		
t_{wL}	Pulse duration, CLK low	T3			9		
t_f	CLK fall time	T4				3	
t_r	CLK rise time	T5				3	
t_{pd}	A31–A2, ADS#, BE3#–BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# valid delay	T6	Figure 6	C_L = 50 pF	3	14	ns
t_{pd}	SMADS#, SMI# valid delay	T6a	Figure 6	C_L = 50 pF	3	14	
t_{dis}	A31–A2 ADS#, BE3#–BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# float delay	T7	Figure 7	see Note 9		19	
t_{dis}	SMADS#, SMI# float delay	T7a	Figure 7	see Note 9		19	
t_{pd}	PCHK# valid delay	T8	Figure 5	C_L = 50 pF	3	18	ns
t_{pd}	BLAST#, PLOCK# valid delay	T8a	Figure 6		3	16	
t_{pd}	HITM#, RPLSET1–0, RPLVAL#, SUSPA# valid delay	T8b	Figure 6		3	16	
t_{dis}	BLAST#, PLOCK# float delay	T9	Figure 7	see Note 9		16	
t_{dis}	RPLSET1–0, RPLVAL# Float delay	T9a	Figure 7	see Note 9		16	
t_{pd}	D31–0, DP3–0 write valid delay	T10	Figure 6	C_L = 50 pF see Note 10	3	17	ns
t_{pd}	D31–0, DP3–0 write float delay	T11	Figure 7	C_L = 50 pF see Note 9		19	
t_{su}	EADS# setup time	T12	Figure 8		6		ns
t_{su}	INVAL setup time	T12a			6		
t_h	EADS# hold time	T13			3		
th	INVAL hold time	T13a			3		
t_{su}	BS16#, BS8#, KEN# setup time	T14	Figure 8		6		ns
t_h	BS16#, BS8#, KEN# hold time	T15			3		
t_{su}	BRDY#, RDY# setup time	T16	Figure 8		6		ns
t_{su}	BRDY#, RDY# setup time	T17			3		
t_{su}	AHOLD, HOLD setup time	T18	Figure 8		6		ns
t_{su}	BOFF# setup time	T18a			8		
t_h	AHOLD, HOLD, BOFF# hold time	T19			3		
t_{su}	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET setup time	T20	Figure 8	see Note 11	6		ns
t_{su}	SMI#, SUSP#, WM_RST setup time	T20a			6		
t_h	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET hold time	T21	Figure 8	see Notes 10 and 11	3		ns
th	SMI#, SUSP#, WM_RST hold time	T21a			3		
t_{su}	A31–4, D31–0, DP3–0 read setup time	T22	Figure 8		6		ns
t_h	A31–4, D31–0, DP3–0 read hold time	T23			3		

NOTES: 7. Input clock can be stopped; therefore, minimum CLK frequency is 0 MHz.
8. These parameters are not tested. They are determined by design characterization.
9. Float condition occurs when maximum output current becomes less than I_I in magnitude. Float is not 100% tested.
10. Not 100% tested.
11. These inputs are allowed to be asynchronous to CLK. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK period.

switching waveforms

Switching waveforms for the TI486DX2 microprocessor are illustrated in Figure 4 through Figure 8.

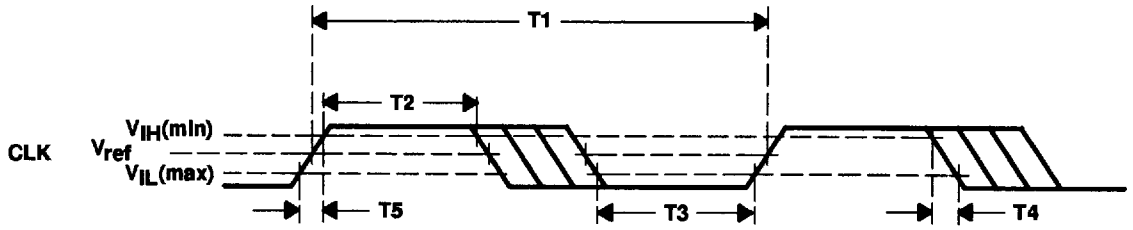


Figure 4. CLK Timing Measurement Points

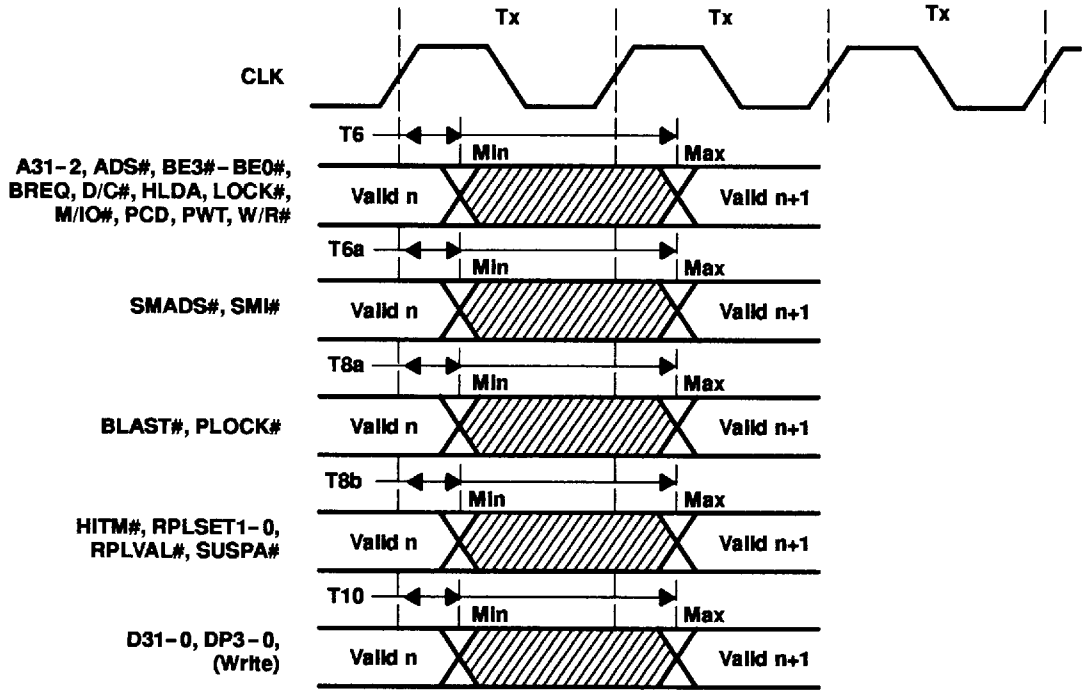


Figure 5. PCHK# Valid Delay Timing

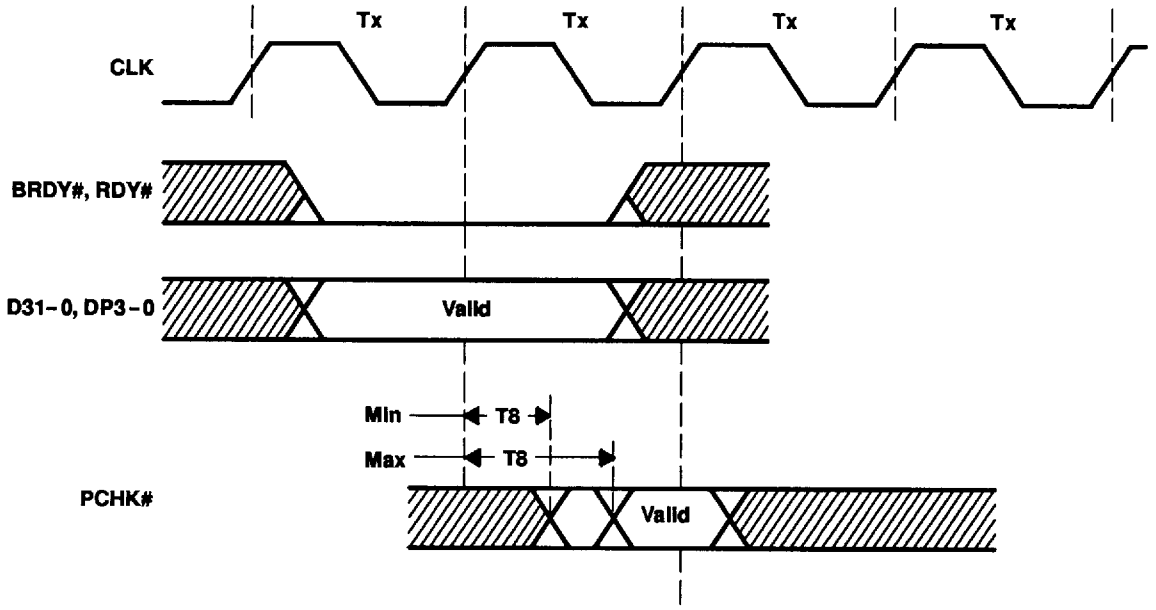


Figure 6. Output Signal Valid Delay Timing

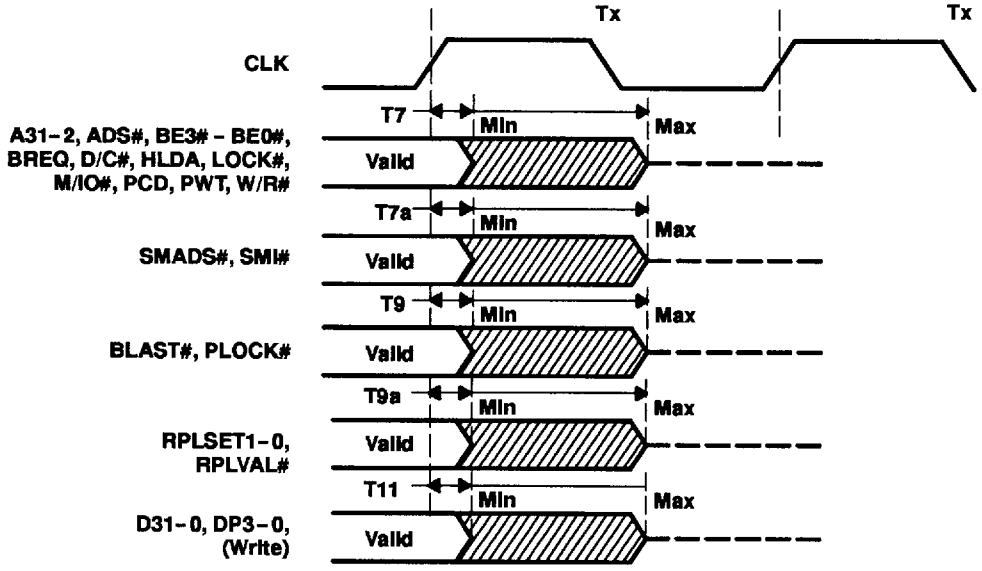


Figure 7. Output Signal Float Delay Timing

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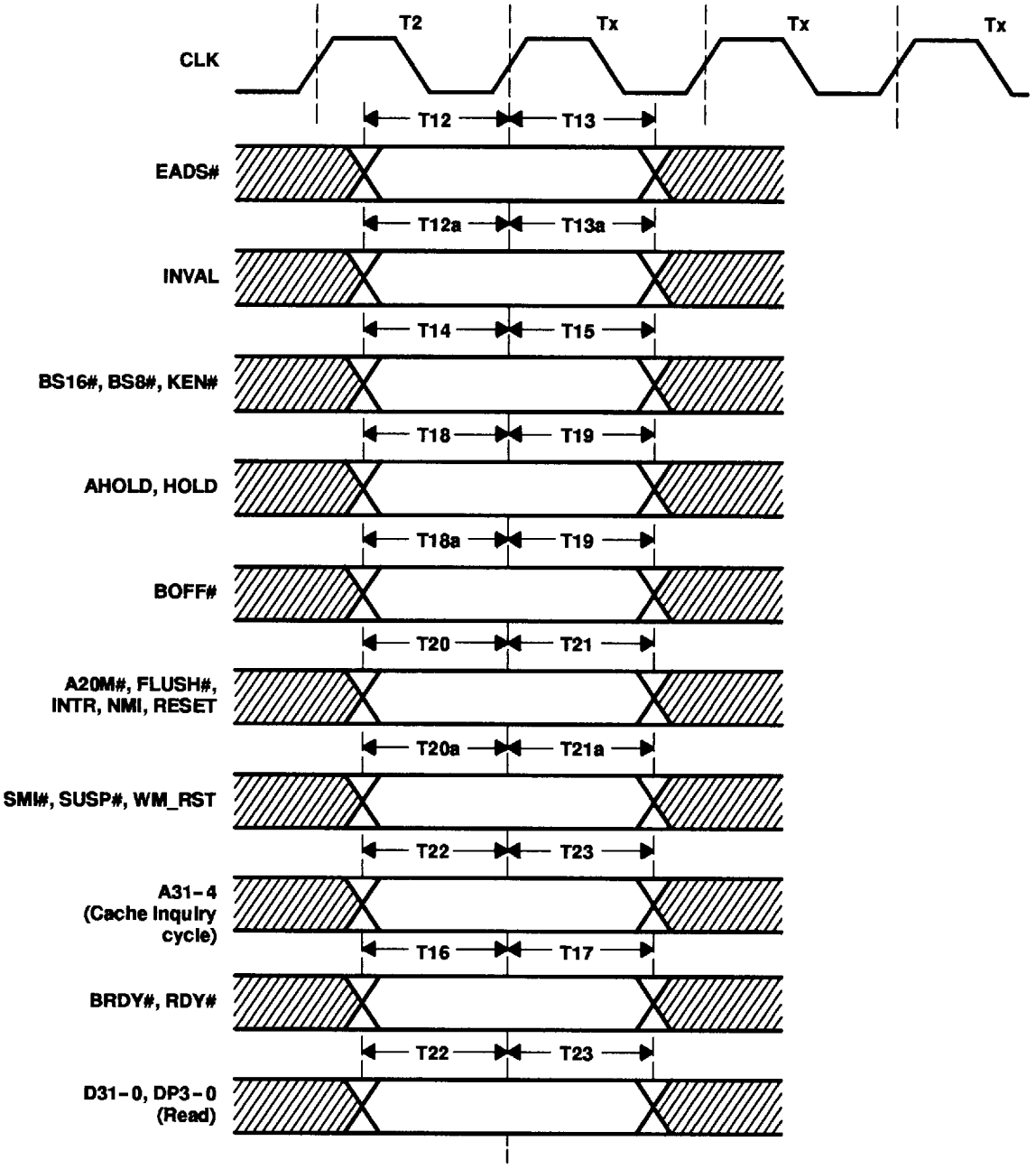

Figure 8. Input Signal Setup and Hold Timing

thermal characteristics

The junction-to-ambient (typical) values vary for individual applications depending on factors relating to how the device is mounted and the surrounding environment such as:

- Circuit trace density of the printed circuit board (PCB) and/or the presence or absence of ground or power planes internal to the PCB that affect the ability of the board to conduct heat away from the device
- Whether the device is soldered to the PCB or is inserted into a socket
- Orientation of the PCB on which device is mounted and the proximity of adjacent PCBs or system enclosure features that impede natural convection air circulation around the device
- Ambient-air temperature in close proximity to the device and the proximity of other high-power devices in the system

The final responsibility for verifying designs incorporating any version of a TI microprocessor rests with the customer originating the design. Recommended case temperature extremes are specified in recommended operating conditions.

airflow measurement setup

The wind tunnel used for airflow measurements is represented schematically in Figure 9.

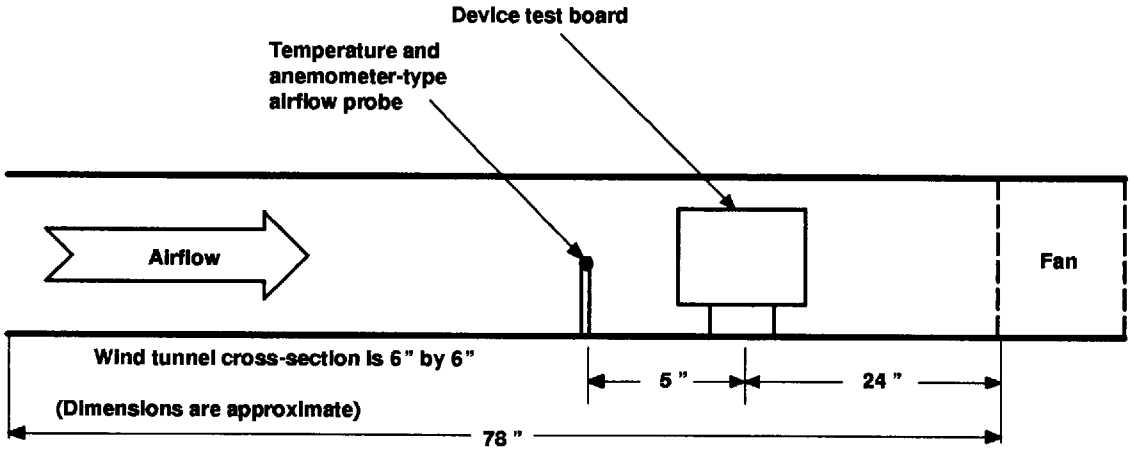

Figure 9. Wind Tunnel Schematic Diagram

Typically, the devices undergoing thermal test are mounted on a test board consisting of 0.062-inch thick FR4 printed circuit board material with one-ounce copper etch. Surface-mount devices are soldered to the test board using matching footprints with the minimal circuit-trace density required to electrically interconnect the device to the board. PGA devices are typically inserted in a socket that is soldered to the test board.

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thermal parameter definitions

The maximum average junction temperature ($T_J$max) and the maximum ambient temperature ($T_A$max) can be calculated using the following equations:

$$T_J\text{max} = T_C + (P_{max} \times R_{\theta JC})$$
$$T_A\text{max} = T_J - (P_{max} \times R_{\theta JA})$$

where:

$T_J$max = Maximum average junction temperature (°C)
T_C = Case temperature at top center of package (°C)
Pmax = Maximum device power dissipation (W)
$R_{\theta JC}$ = Junction-to-case thermal resistance (°C/W)
$T_A$max = Maximum ambient temperature (°C)
T_J = Average junction temperature (°C)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

Values for $R_{\theta JA}$ and $R_{\theta JC}$ are given in Table 8 and Table 9 for various airflows.

Table 8. 168-Pin CPGA Thermal Resistance and Airflow

AIRFLOW (FT/MIN)	THERMAL RESISTANCE (°C/W) 168-PIN CERAMIC PGA PACKAGE	
	$R_{\theta JC}$	$R_{\theta JA}$
0	3	19
100	3	16
200	3	14
400	3	11
600	3	10

Thermal resistance values shown are based on measurements made on similar ceramic PGA packages.

Table 9. 208-Pin CQFP Thermal Resistance and Airflow

AIRFLOW (FT/MIN)	THERMAL RESISTANCE (°C/W) 208-PIN CERAMIC QUAD FLAT PACKAGE	
	$R_{\theta JC}$	$R_{\theta JA}$
0	4	29
100	4	25
200	4	22
400	4	19
600	4	16

Thermal resistance values shown are based on measurements made on similar ceramic PGA packages.

mechanical specifications

The TI486DX2 microprocessor is supplied in the following packages:

- 168-pin, ceramic pin grid array package
- 208-pin, ceramic quad flat package

Mechanical specifications provide physical dimensions for the 168-pin and 208-pin packages.

Industry-standard dimensioned drawings are supplied for each package.

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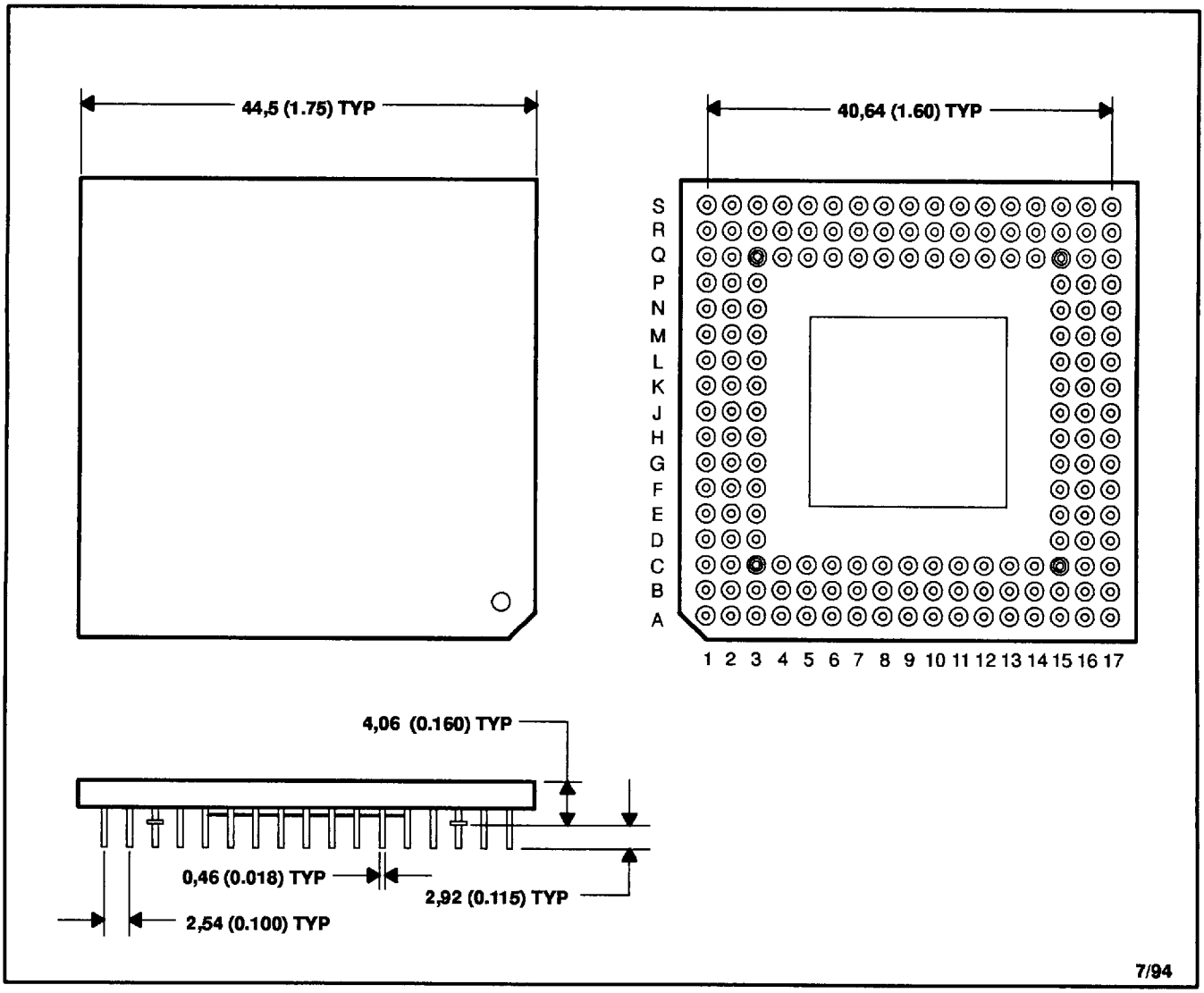
MECHANICAL DATA

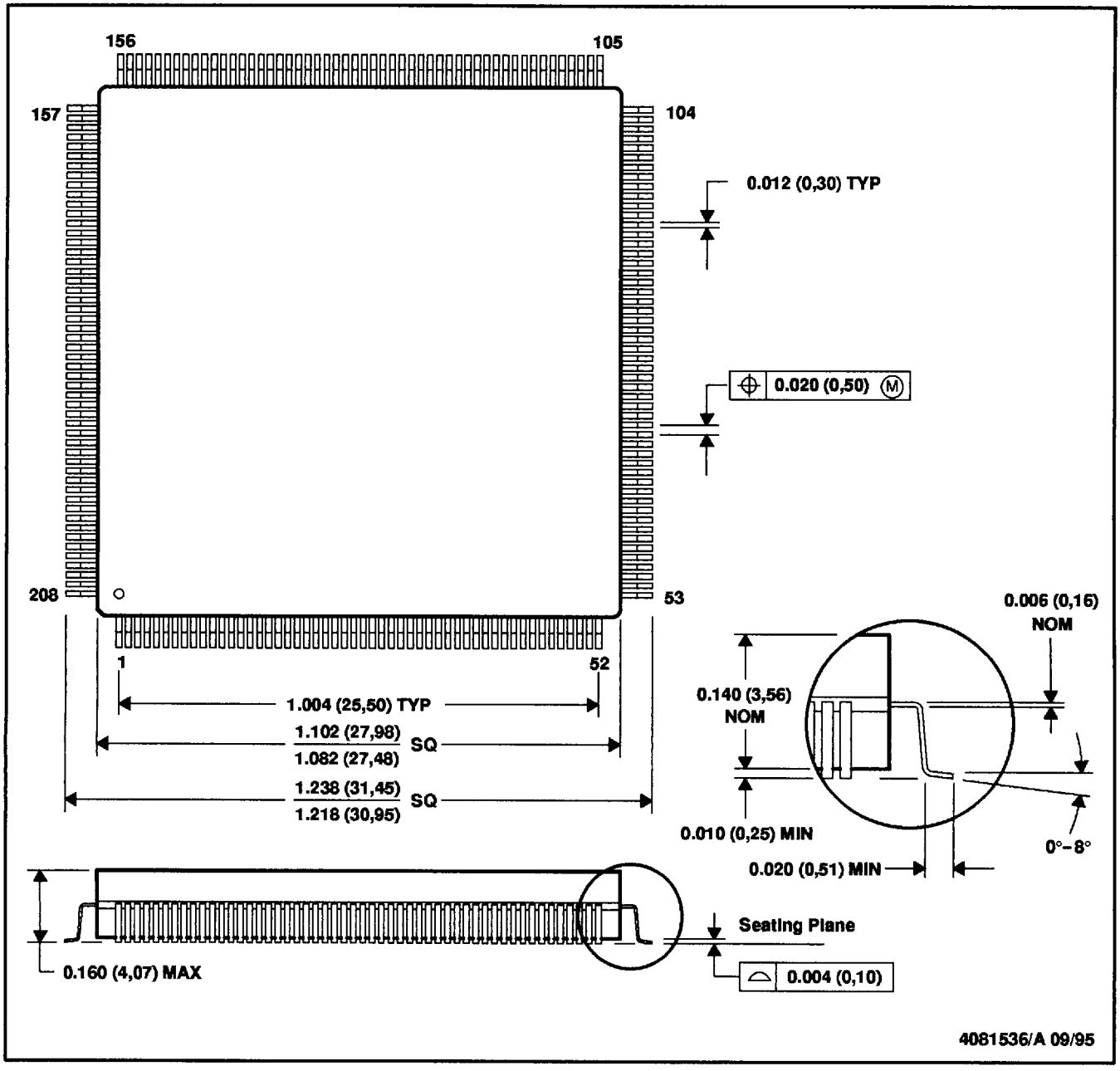
CPGA-168 PIN **CERAMIC PIN GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.

MECHANICAL DATA

WR (S-GQFP-G208) **CERAMIC QUAD FLATPACK (DIE-DOWN)**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.