September 1990
Edition 2.0

FUJITSU

DATA SHEET

MB84256A-70/70L/70LL/-10/10L/10LL/-12/12L/12LL/-15/15L/15LL
CMOS 256K-BIT LOW POWER SRAM

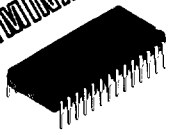
32K Words x 8 Bits CMOS Static Random Access Memory with Data Retention

The Fujitsu MB84256A is a 32,768 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

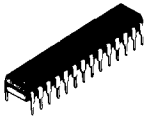
The MB84256A has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 32,768 words x 8 bits
- Access time: 70 ns max. (MB84256A-70/-70L/-70LL)
  100 ns max. (MB84256A-10/-10L/-10LL)
  120 ns max. (MB84256A-12/-12L/-12LL)
  150 ns max. (MB84256A-15/-15L/-15LL)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V power supply ±10% tolerance
- Low power standby:
  CMOS level 5.5 mW max. (MB84256A-70/-10/-12/-15)
  0.55 mW max. (MB84256A-70L/-70LL/-10LL, -12L/-12LL/-15LL)
  TTL level 16.5 mW max. (MB84256A-70/-70L/-70LL/-10L/-10LL, -12/-12L/-12LL/-15L/-15LL)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
  DIP (600 mil) MB84256A-xx(L/LL)P
  Skinny DIP (300 mil) MB84256A-xx(L/LL)PSK
  SOP MB84256A-xx(L/LL)PF
  TSOP (normal bend) MB84256A-xx(L/LL)PFTN
  TSOP (reverse bend) MB84256A-xx(L/LL)PFTR

PRELIMINARY



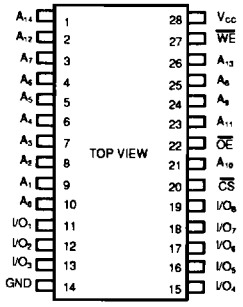
PLASTIC PACKAGE
DIP-28P-M02



PLASTIC PACKAGE
DIP-28P-M04

PLASTIC PACKAGE
FPT-28P-M02
*TSOP packages: PFTN/PFTR

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	−40 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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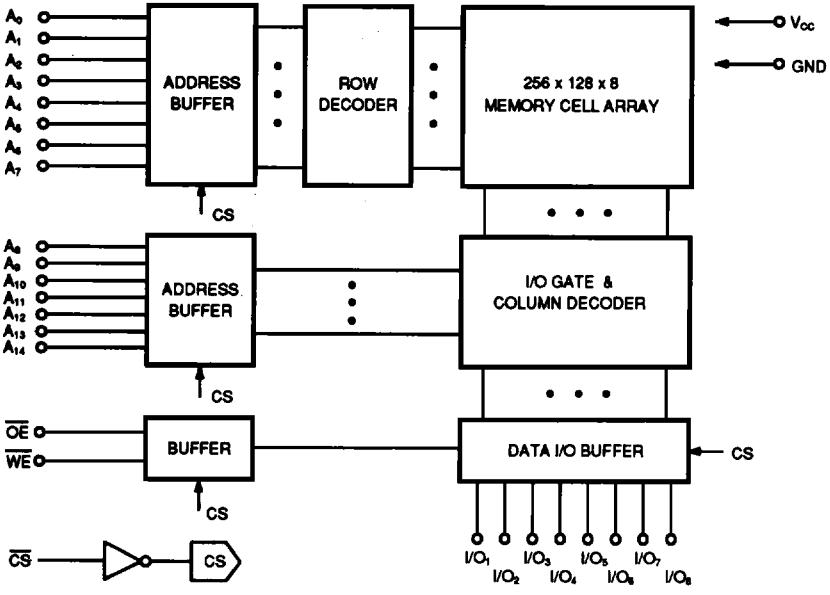
Fig. 1 – MB84256A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High–Z
L	H	H	D_{OUT} Disable	I_{CC}	High–Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

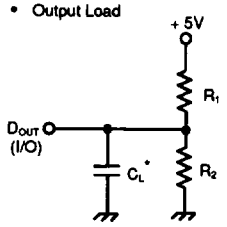
(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Condition	MB84256A-70/10/12/15		MB84256A-70L/70LL/10L/10LL/12L/12LL/15L/15LL		Unit
				Min	Max	Min	Max	
Standby Supply Current		I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$		1		0.1	mA
		I_{SB2}	$\overline{CS} = V_{IH}$		3		3	mA
Active Supply Current		I_{CC1}	$V_{IN} = V_{IH}$ or V_{IL}, $\overline{CS} = V_{IL}$, I_{OUT} = 0mA		60		60	mA
Operating Supply Current	-70	I_{CC2}	Cycle = Min. Duty = 100% I_{OUT} = 0mA		80		80	mA
	-10/12/15				70		70	
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	−1	1	−1	1	µA
Output Leakage Current		I_{LO}	$V_{I/O}$ = 0V to V_{CC}, $\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	−1	1	−1	1	µA
Input High Voltage		V_{IH}		2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
Input Low Voltage		V_{IL}		−3.0 *	0.8	−3.0 *	0.8	V
Output High Voltage		V_{OH}	I_{OH} = −1.0mA	2.4		2.4		V
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA		0.4		0.4	V

Note: All voltages are referenced to GND.
*: −3.0V min. for pulse width less than 20 ns.(V_{IL} min. = −0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS

- Output Load



* Including Jig and stray capacitance

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.0V

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		150		ns
Address Access Time *2	t_{AA}		70		100		120		150	ns
$\overline{CS}$ Access Time *3	t_{ACS}		70		100		120		150	ns
Output Enable to Output Valid	t_{OE}		35		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		ns
Chip Select to Output Low-Z *4	t_{CLZ}	10		10		10		10		ns
Output Enable to Output Low-Z *4	t_{OLZ}	5		5		5		5		ns
Chip Select to Output High-Z *4	t_{CHZ}		25		40		40		50	ns
Output Enable to Output High-Z *4	t_{OHZ}		25		40		40		50	ns

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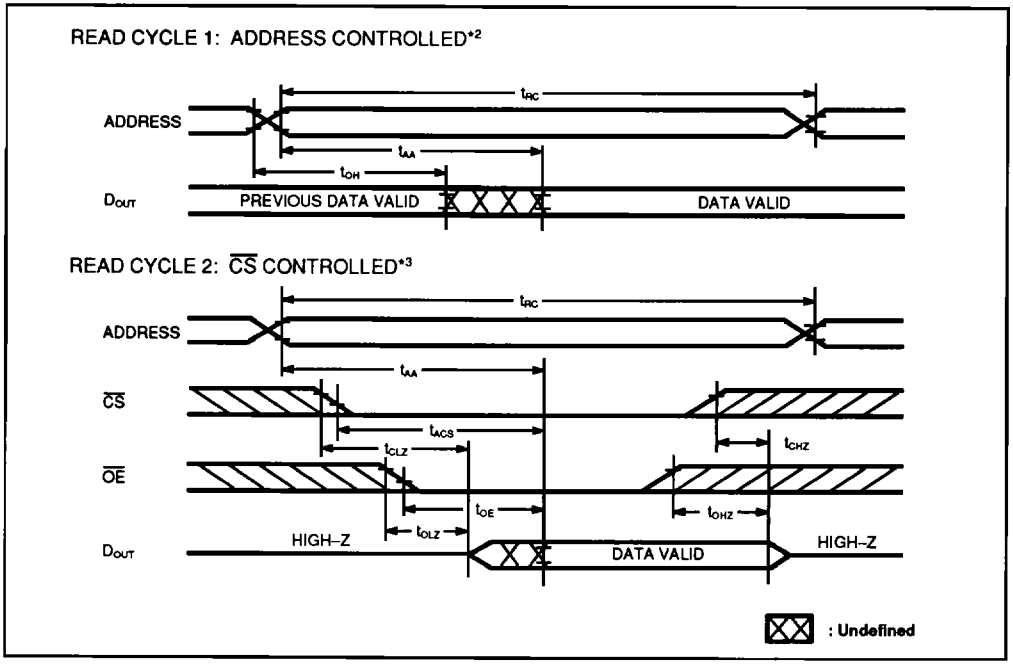
READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$ = $\overline{OE}$ = V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE *1*2

Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	70		100		120		150		ns
Address Valid to End of Write	t_{AW}	50		80		85		100		ns
Chip Select to End of Write	t_{CW}	50		80		85		100		ns
Data Valid to End of Write	t_{DW}	25		40		45		50		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Pulse Width	t_{WP}	50		60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Write Recovery Time *4	t_{WR}	5		5		5		5		ns
$\overline{WE}$ to Output Low-Z *5	t_{WLZ}	5		5		5		5		ns
$\overline{WE}$ to Output High-Z *5	t_{WHZ}		25		40		40		50	ns

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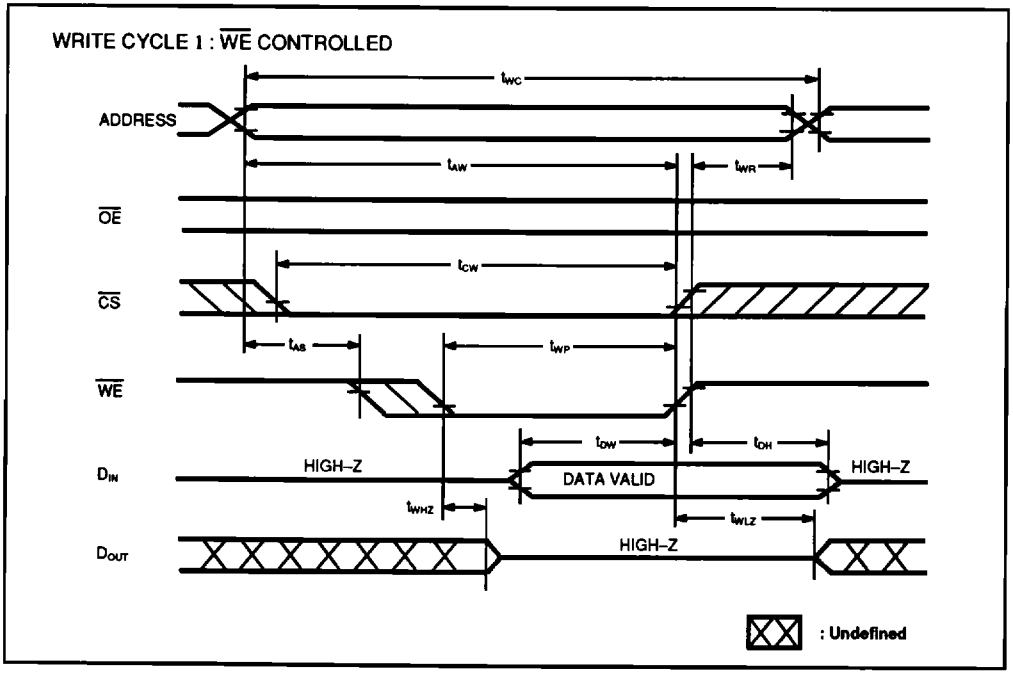
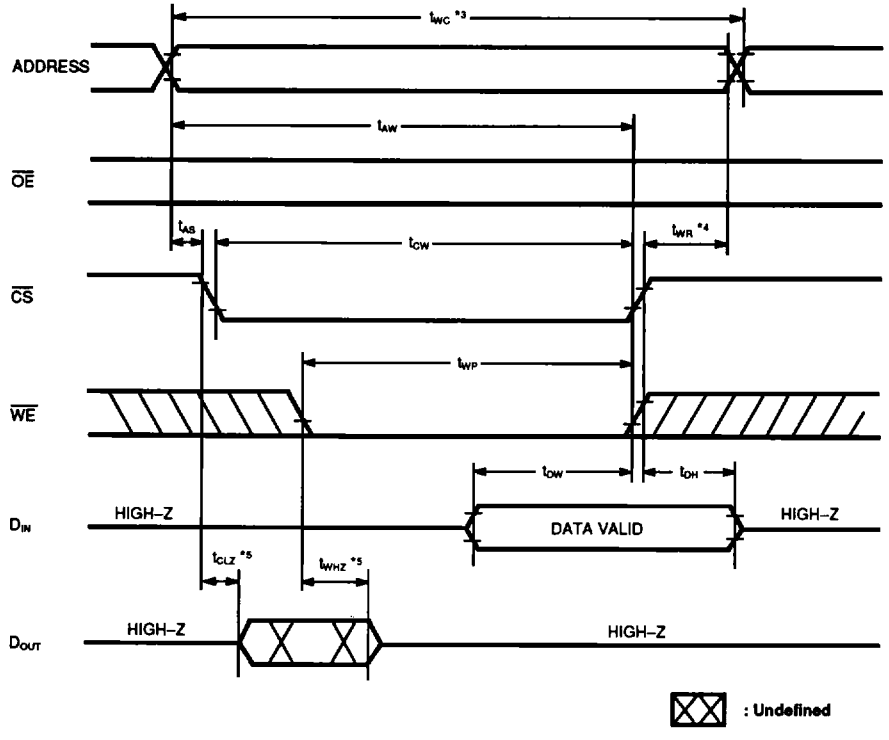
WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode..
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load I in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1 *2

WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode..

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1		V_{DR}	2.0		5.5	V
Data Retention Supply Current *2	Standard	I_{DR}			1.0	mA
	L-Version			1.0	50	µA
	LL-Version *3			1.0	5.0	
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $\overline{CS} \geq V_{DR} - 0.2V$
*2 $V_{DR} = 3.0V$, $\overline{CS} \geq V_{DR} - 0.2V$
*3 $V_{DR} = 3.0V$, $T_A = 40°C$

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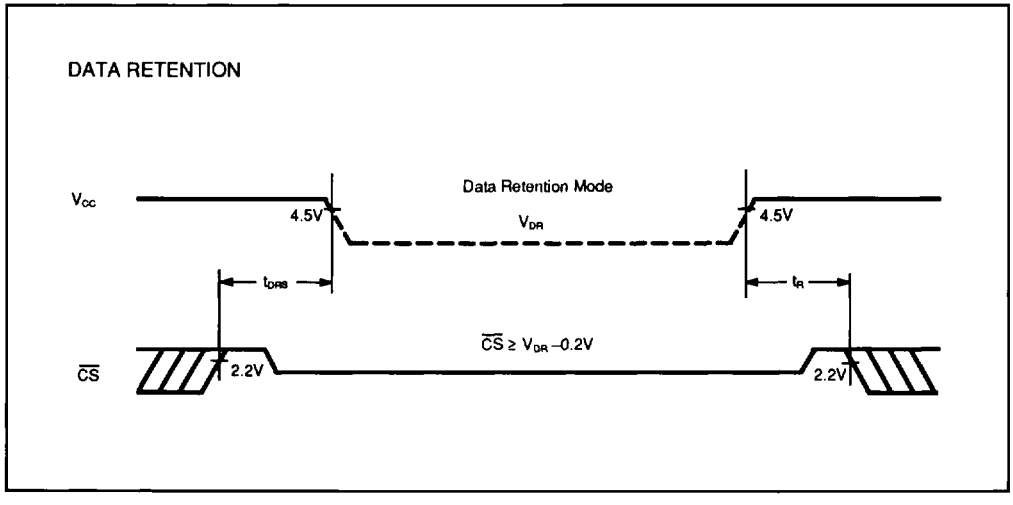
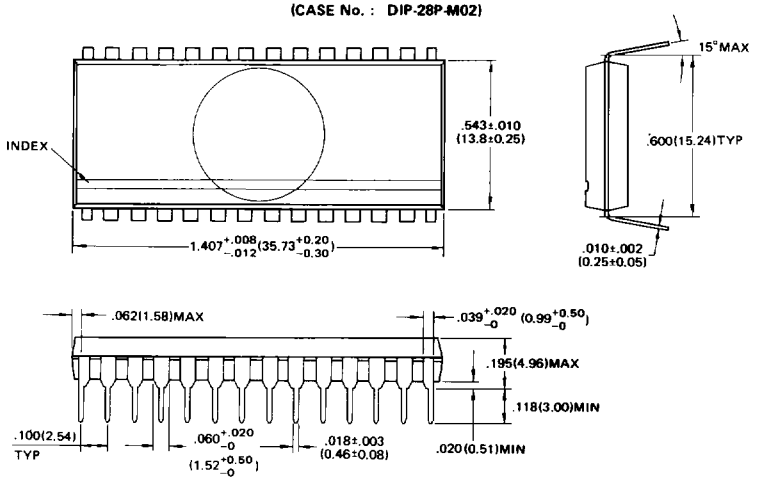
DATA RETENTION TIMING



PACKAGE DIMENSIONS

(Suffix: P)

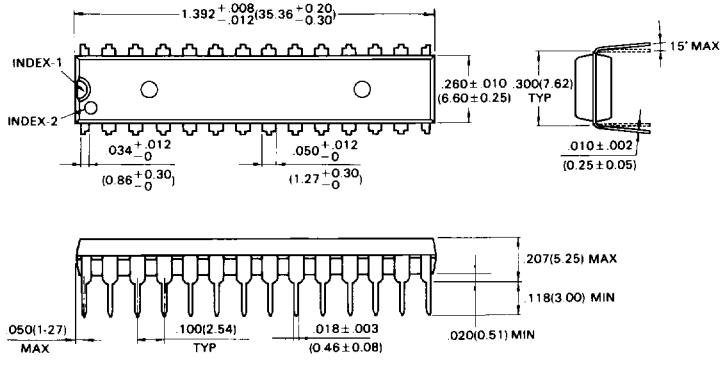
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in inches (millimeters)

(Suffix: P-SK)

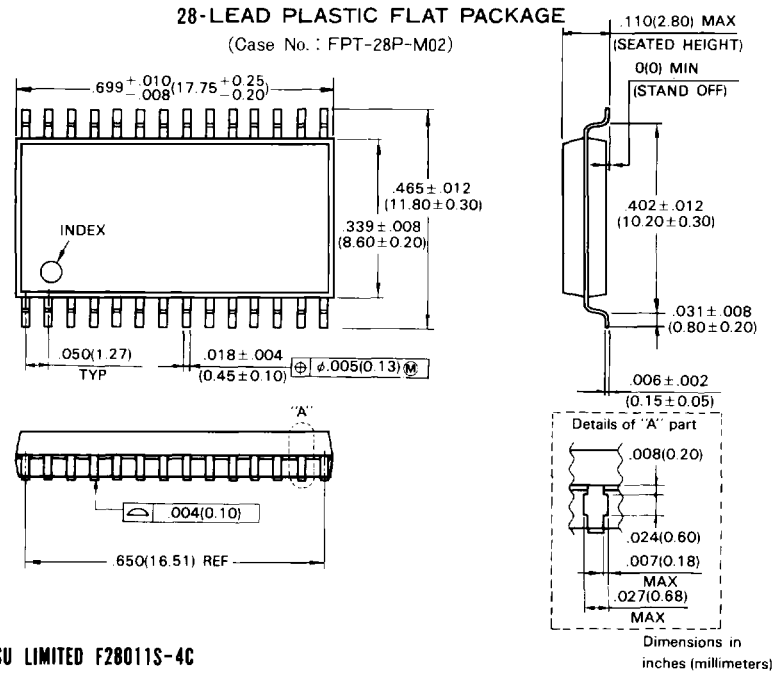
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-28P-M04)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

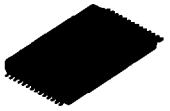
(Suffix: PF)



3

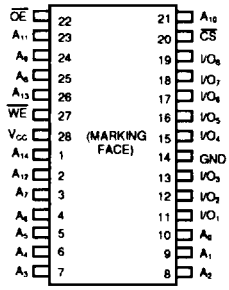
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



FPT-28P-M03

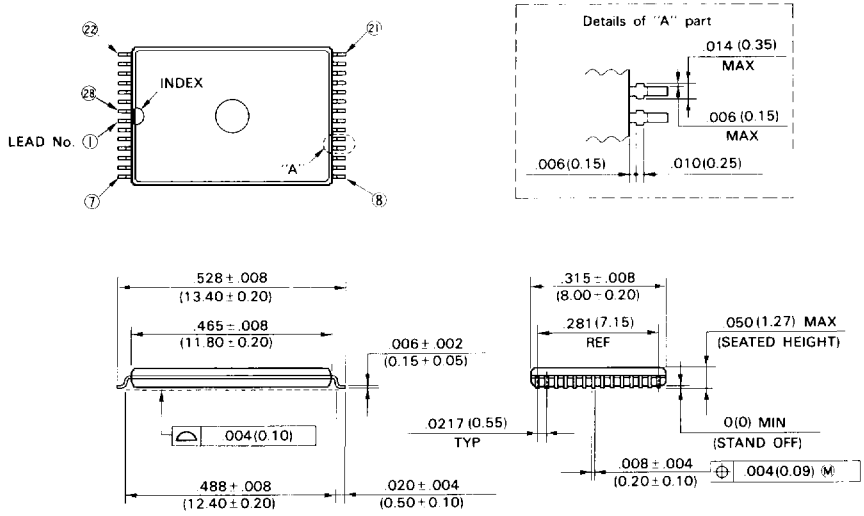
PIN ASSIGNMENT
(NORMAL BEND)



TOP VIEW

28-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-28P-M03)



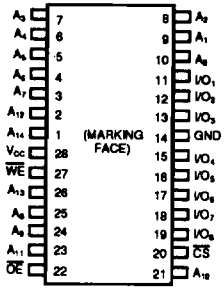
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)

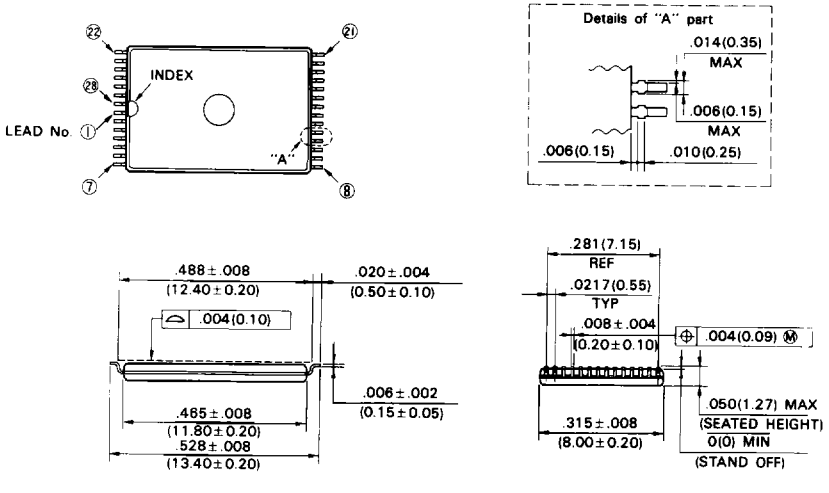
FPT-28P-M04

PIN ASSIGNMENT
(REVERSE BEND)



BOTTOM VIEW

28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M04)



Dimensions in inches (millimeters)

3