

## 4M × 32 -Bit Dynamic RAM Module SMALL OUTLINE MEMORY MODULE

**HYM32V4040GD(L)-50/-60**

### Advanced Information

- 72-Pin Small Outline Dual-in-Line Memory Module
- 1 bank 4M x 32-bit organization
- Fast Page Mode Operation
- Performance:

		-50	-60	
t <sub>RC</sub>	Read / Write Cycle Time	90	110	ns
t <sub>RAC</sub>	RAS Access Time	50	60	ns
t <sub>CAC</sub>	CAS Access Time	13	15	ns
t <sub>AA</sub>	Access Time From Address	25	30	ns
t <sub>PC</sub>	Fast Page Mode Cycle Time	35	40	ns

- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation  
max. 936 mW active (-50 version)  
max. 756 mW active (-60 version)  
  
LVTTL – 14.4 mW standby  
LVCMOS– 6.5 mW standby  
LVCMOS– 2.88 mW standby (L-version)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only-refresh
- Self Refresh on HYM32V4040GDL versions
- 2 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully LV-TTL compatible
- Card size 59.69 mm x 25.40 mm x 2.30 mm
- Utilizes two 4M × 16 -DRAMs (HYB 3165160AT(L)) in 400mil wide TSOPII-50 packages
- 12R / 10C addressing
- 4096 refresh cycles / 64 ms for HYM32V4040GD  
4096 refresh cycles / 128 ms for HYM32V4040GDL
- Gold contact pad

The HYM 32V4040GD(L) are 16 MByte DRAM 72 pin small outline dual-in-line memory modules organized as 4M x 32, comprising two 4M x 16 DRAMs (HYB 3165160AT) in 400mil wide TSOPII packages mounted together with ceramic decoupling capacitors on a PC board. Each HYB 3165160AT is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed. The HYM32V4040GD(L) parts (L-versions) have a very lower power „sleep mode“ supported by Self Refresh.

The density and speed of the module can be detected by the use of presence detect pins.

These modules are ideal for portable systems applications where high memory capacity is needed.

### Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 32V4040GD -50	Q67100-	L-DIM-72-4	50 ns DRAM module
HYM 32V4040GD -60	Q67100-	L-DIM-72-4	60 ns DRAM module
HYM 32V4040GDL -50	Q67100-	L-DIM-72-4	50 ns Low Power DRAM module with Self Refresh
HYM 32V4040GDL -60	Q67100-	L-DIM-72-4	60 ns Low Power DRAM module with Self Refresh

### Pin Names

A0-A11	Row Address Input
A0-A9	Column Address Inputs
DQ0 - DQ31	Data Input/Output
RAS0, RAS2	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
WE	Read / Write Input
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD7	Presence Detect Pins
N.C.	No Connection

### Presence-Detect Truth Table \*):

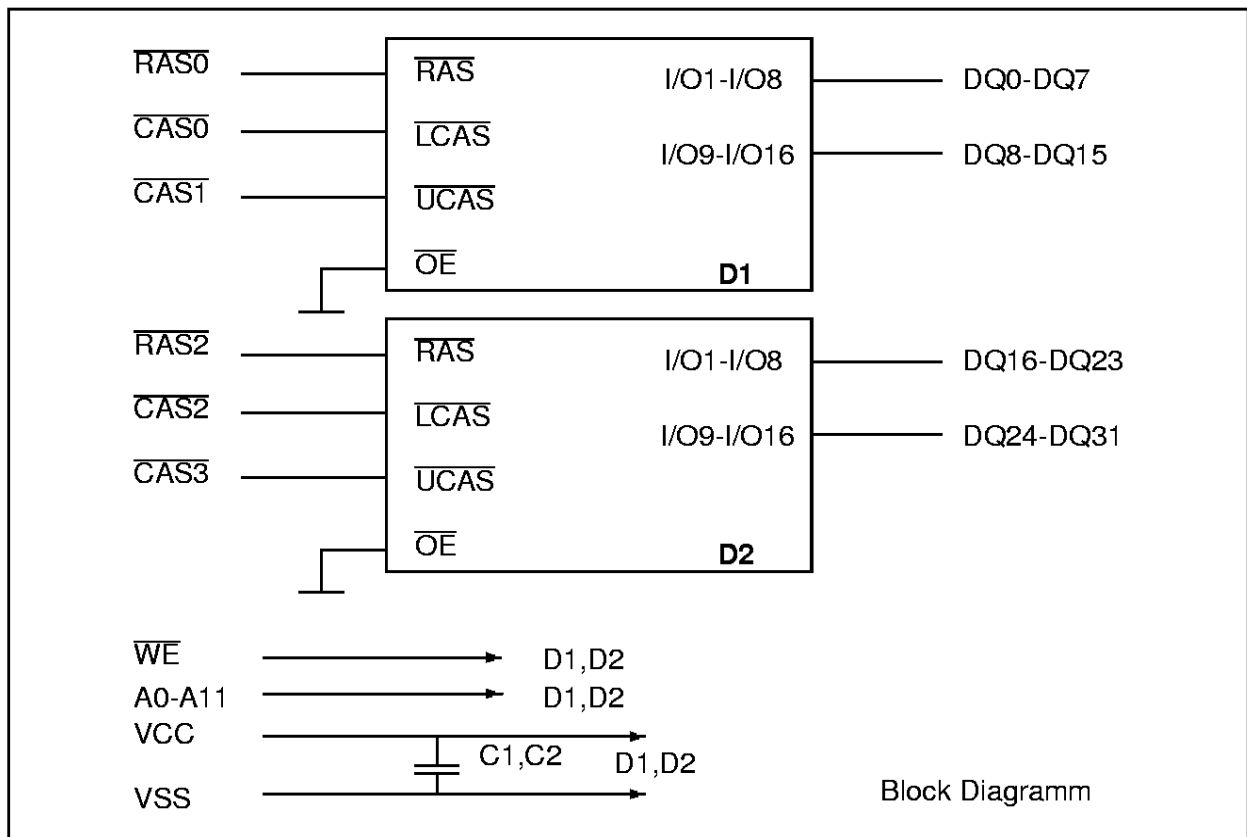
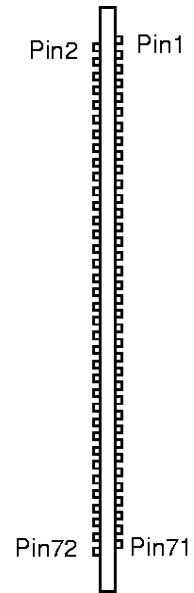
Module	PD1	PD2	PD3	PD4	PD5	PD6	PD7
HYM 32V4040GD -50	NC	NC	VSS	NC	VSS	VSS	NC
HYM 32V4040GD -60	NC	NC	VSS	NC	NC	NC	NC
HYM 32V4040GDL -50	NC	NC	VSS	NC	VSS	VSS	VSS
HYM 32V4040GDL -60	NC	NC	VSS	NC	NC	NC	VSS

### Pin Configuration

PIN	Name	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	37	DQ16	2	DQ0	38	DQ17
3	DQ1	39	VSS	4	DQ2	40	CAS0
5	DQ3	41	CAS2	6	DQ4	42	CAS3
7	DQ5	43	CAS1	8	DQ6	44	RAS0
9	DQ7	45	NC	10	VCC	46	NC
11	PD1	47	WRITE	12	A0	48	NC
13	A1	49	DQ18	14	A2	50	DQ19
15	A3	51	DQ20	16	A4	52	DQ21
17	A5	53	DQ22	18	A6	54	DQ23
19	A10	55	NC	20	NC	56	DQ24
21	DQ8	57	DQ25	22	DQ9	58	DQ26
23	DQ10	59	DQ28	24	DQ11	60	DQ27
25	DQ12	61	VCC	26	DQ13	62	DQ29
27	DQ14	63	DQ30	28	A7	64	DQ31
29	A11	65	NC	30	VCC	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	RAS2	70	PD6
35	DQ15	71	PD7	36	NC	72	VSS

Front Side

Back Side



### Absolute Maximum Ratings

Operating temperature range.....	0 to 70 °C
Storage temperature range.....	- 55 to 150 °C
Input/output voltage.....	-0.5 to min (V <sub>CC</sub> +0.5,4.6) V
Power supply voltage.....	-0.5V to 4.6 V
Power dissipation.....	1.2 W
Data out current (short circuit).....	50 mA

### DC Characteristics

$T_A = 0$  to 70 °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	$V_{IH}$	2.0	$V_{CC}+0.3$	V	1)
Input low voltage	$V_{IL}$	- 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage (I <sub>out</sub> = -2mA)	$V_{OH}$	2.4	-	V	1)
Output low voltage (LVTTL) Output „L“ level voltage (I <sub>out</sub> = +2mA)	$V_{OL}$	-	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ level voltage (I <sub>out</sub> = -100uA)	$V_{OH}$	$V_{CC}-0.2$	-	V	1)
Output low voltage (LVCMOS) Output „L“ level voltage (I <sub>out</sub> = +100uA)	$V_{OL}$	-	0.2	V	1)
Input leakage current, any input (0 V < $V_{in}$ < $V_{CC}$ , all other pins = 0 V)	$I_{I(L)}$	- 10	10	μA	
Output leakage current (DO is disabled, 0 V < $V_{out}$ < $V_{CC}$ )	$I_{O(L)}$	- 10	10	μA	
Average $V_{CC}$ supply current: -50 ns version -60 ns version ( $\overline{RAS}$ , $\overline{CAS}$ , address cycling: t <sub>RC</sub> = t <sub>RC</sub> min.)	$I_{CC1}$	-	260 210	mA mA	2) 3) 4)
Standby $V_{CC}$ supply current ( $\overline{RAS}=\overline{CAS}= V_{IH}$ )	$I_{CC2}$	-	4	mA	-
Average $V_{CC}$ supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: $\overline{CAS} = V_{IH}$ ; t <sub>RC</sub> = t <sub>RC</sub> min.)	$I_{CC3}$	-	260 210	mA mA	2) 3)

**DC Characteristics** (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average $V_{CC}$ supply current, during fast page mode: -50 ns version -60 ns version ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: $t_{PC}=t_{PC}$ min.)	$I_{CC4}$	–	120 100	mA mA	2) 3) 4)
Standby $V_{CC}$ supply current ( $\overline{RAS}=\overline{CAS}= V_{CC}-0.2V$ )	$I_{CC5}$	–	1.8 0.4	mA mA	– L-version
Average $V_{CC}$ supply current, during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode: -50 ns version -60 ns version ( $\overline{RAS}$ , $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ min.)	$I_{CC6}$	–	260 210	mA mA	2) 4)
Self Refresh Current (L-version only)  (CBR cycle with $t_{RAS}>t_{RASSmin}$ , $\overline{CAS}$ held low, $\overline{WE}=V_{CC}-0.2V$ , Address and $\overline{Din}=V_{CC}-0.2V$ or 0.2V)	$I_{CC7}$	–	0.8	mA	

**Capacitance**

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance ( $A0$ to $A11$ , $\overline{WE}$ )	$C_{I1}$	–	25	pF
Input capacitance ( $\overline{RAS0}$ , $\overline{RAS2}$ )	$C_{I2}$	–	20	pF
Input capacitance ( $\overline{CAS0}$ - $\overline{CAS3}$ )	$C_{I3}$	–	20	pF
I/O capacitance ( $DQ0$ - $DQ31$ )	$C_{I0}$	–	15	pF

### AC Characteristics <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

#### *common parameters*

Random read or write cycle time	$t_{RC}$	90	–	110	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	30	–	40	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	13	10k	15	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	18	37	20	45		
$\overline{RAS}$ to column address delay time	$t_{RAD}$	13	25	15	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	13		15	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	50		60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	3	30	3	30	ns	7
Refresh period	$t_{REF}$	–	64	–	64	ms	
Refresh period for L- version	$t_{REF}$	–	128	–	128	ms	

#### *Read Cycle*

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	ns	8,10
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	$t_{RRH}$	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	$t_{CLZ}$	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	ns	12

**AC Characteristics** (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

**Early Write Cycle**

Write command hold time	$t_{WCH}$	8	–	10	–	ns	
Write command pulse width	$t_{WP}$	8	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	ns	13
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	13	–	15	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	ns	14
Data hold time	$t_{DH}$	10	–	10	–	ns	14

**Fast Page Mode Cycle**

Fast page mode cycle time	$t_{PC}$	35	–	40	–	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	–	30	–	35	ns	7
$\overline{RAS}$ pulse width	$t_{RAS}$	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	$t_{RHCP}$	30	–	35	–	ns	

**$\overline{CAS}$ -before- $\overline{RAS}$  Refresh Cycle**

$\overline{CAS}$ setup time	$t_{CSR}$	5	–	5	–	ns	
$\overline{CAS}$ hold time	$t_{CHR}$	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	$t_{WRP}$	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	$t_{WRH}$	10	–	10	–	ns	

**Self Refresh Cycle (L-version only)**

$\overline{RAS}$ pulse width	$t_{RASS}$	100k	–	100k	–	ns	15
$\overline{RAS}$ precharge time	$t_{RPS}$	95	–	110	–	ns	15
$\overline{CAS}$ hold time	$t_{CHS}$	-50	–	-50	–	ns	15

### Notes:

- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{RAS} = VIL$ . In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).
- 5) An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 5$  ns.
- 7)  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with a load equivalent to 2 TTL loads and 100 pF.
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels
- 13) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If  $tWCS > tWCS$  (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle.
- 14) These parameters are referenced to the  $\overline{CAS}$  leading edge.
- 15) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
 If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
 If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediately after exit from Self Refresh.

SO-DIMM PACKAGE OUTLINES

